A CMOS 5.37-mW 10-Bit 200-MS/s Dual-Path Pipelined ADC

Yun Chai, *Student Member, IEEE*, and Jieh-Tsorng Wu, *Senior Member, IEEE*

***Abstract*—A 10-bit 200-MS/s pipelined ADC was fabricated using a standard 65 nm CMOS technology. We propose a dual-path amplification technique for residue generation. We split the pipeline stage into a coarse-stage multiplying digital-to-analog converter (MDAC) and a fine-stage MDAC. The opamps for these two MDACs require different specifications. They can be designed and optimized separately. They are turned off when not in use to save power. We modify the operation of a pipeline stage to accommodate the dual-path scheme by using time-interleaving capacitor sets. Operating at 200 MS/s sampling rate, this ADC consumes 5.37 mW from a 1 V supply. It achieves a signal-to-noise-plus-distortion ratio (SNDR) better than 55 dB SNDR over the entire Nyquist band. The chip active area is 0.19 mm^2.**

***Index Terms*—Analog-to-digital conversion, pipeline processing, switched-capacitor amplification, switching circuits.**

I. Introduction

PIPELINED analog-to-digital converters (ADCs) can simultaneously achieve high resolution and high sampling rate. Previous published high-performance pipelined ADCs include 10-bit ADCs with higher than 100 MS/s sampling rate [1]–[7], 12-bit ADCs with larger than 100 MS/s sampling rate [8], [9], and 14-bit ADCs with larger 100 MS/s sampling rate [10]–[12].

A pipelined ADC consists of a cascade of pipeline stages. Each pipeline stage uses the quantized-feedforward conversion operation to resolve its input into a digital code and an analog residue. The residue then serves as the input for the next stage. In most cases, it is the accuracy and speed of this residue generation that determines the overall performance of a pipeline ADC. In CMOS technologies, the residue generation is realized using a multiplying digital-to-analog converter (MDAC) [13], consisting of an opamp, switches, and capacitors. It is the opamp that determines the performance of an MDAC. Key opamp specifications are dc gain, frequency response, noise, output signal range, and power consumption. A high-performance opamp consumes large power.

The overall ADC power consumption can be reduced by stage scaling [14], i.e., shrinking both capacitors and opamps along the pipeline. The average power of an opamp can be reduced by turning it off when it is not in use [15]–[18]. The dc gain requirement of the opamps can be relaxed by using the dual-residue architecture [9], [19], but the scheme demands matching between two signal paths. The dc gain requirement of the opamp can also be relaxed by digital calibration [20]–[25].

This paper describes a CMOS low-power 10-bit 200-MS/s pipelined ADC. Resolution is achieved by the inherent capacitor matching of the technology. We avoided digital calibration to keep design simple. We employed a dual-path amplification technique for residue generation. An MDAC is split into two different paths. One path generates a large-swing signal that may not be accurate due to the non-ideal opamp. The other path provides signal accuracy but needs only to generate a small-swing signal. This amplification technique uses two different types of opamps, which have different requirements and can be designed and optimized separately. To save power, the opamps are turned off when not in use. The opamps must be able to wake up quickly for high-speed operation. In the dual-path configuration, opamps can be designed with fast turn-on time. We also redesigned the pipeline stages to accommodate the dual-path techniques. We use time-interleaving capacitor sets to increase the amplification time for the opamps, leading to further power reduction. This ADC was fabricated using a standard 65 nm CMOS technology. Operating at 200 MS/s sampling rate, it consumes 5.37 mW from a 1 V supply. It achieves a signal-to-noise-plus-distortion ratio (SNDR) better than 55 dB SNDR over the entire Nyquist band.

The remainder of this paper is organized as follows. Section II introduces the dual-path amplification technique and reviews several residue generation schemes for comparison. Section III describes the dual-path pipelined ADC architecture. Section IV provides detailed description of the circuits used in the ADC, including opamps and comparators. Section V shows the experimental results. Section VI draws conclusions.

II. Residue Generation Techniques

Fig. 1 shows the architecture of a conventional 10-bit pipelined ADC. There are eight pipeline stages. Each stage includes an analog processor (AP). Each AP resolves one bit with redundancy. The final stage is a 3-bit flash ADC consisting of 7 comparators. An encoder combines the stage digital outputs D_1 to D_9 to generate the final ADC digital output D_o. The pipelined ADC operates with two-phase non-overlapping clocks, ϕ_1 and ϕ_2. The neighboring stages operate with clocks of opposite clock phases. Consider the first stage AP1. Its input V_1 is available during ϕ_1. Voltage V_1 is sampled by AP1 and digitized into a digital code D_1. AP1 is enabled during ϕ_2. Its output V_2 is sampled by the 2nd stage, AP2.

Fig. 2 shows the AP1 block diagram. It performs the quantized-feedforward operation [26], [27]. Two comparators compare analog input V_1 with references $\pm V_r/4$ respectively. A

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The authors are with the Department of Electronics Engineering, National Chiao-Tung University, Hsin-Chu, 300, Taiwan (e-mail: angelia.ee99g@nctu.edu.tw; jt.wu@g2.nctu.edu.tw).

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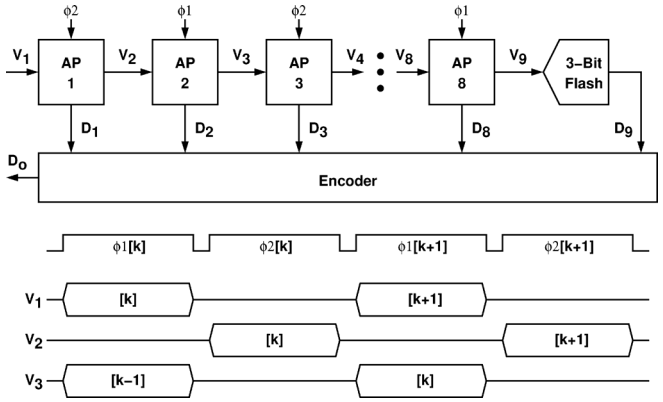

Fig. 1. A conventional 10-bit pipelined ADC.

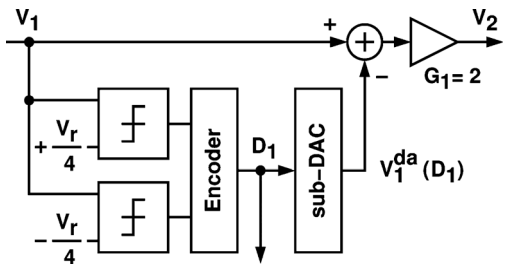

Fig. 2. A quantized-feedforward analog processor (AP).

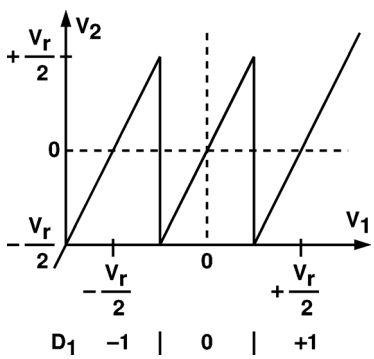

Fig. 3. Transfer function of an analog processor (AP).

local encoder generates $D_1 \in \{-1, 0, +1\}$ based on the comparison results. The digital code D_1 drives a sub-DAC, whose output, $V_1^{da}(D_1) = (V_r/2) \times D_1$, is an estimate of V_1. The difference $V_1 - V_1^{da}$ is amplified by a gain factor of $G_1 = 2$ to generate the residue V_2. The ideal V_2 is

$$V_{2,\text{ideal}} = 2 \times \left(V_1 - \frac{V_r}{2} \times D_1 \right) \tag{1}$$

Fig. 3 shows the transfer function of the pipeline stage.

Fig. 4 shows a switched-capacitor multiplying digital-to-analog converter (MDAC) and its operation. This MDAC performs the functions of sub-DAC, analog subtraction, and residue amplification shown in Fig. 2. The MDAC consists of an opamp A_1 and two capacitors C_1 and C_2. The superscript on the capacitor name marks its pipeline stage. During ϕ_1, input V_1 is sampled onto the two capacitors in the 1st stage, C_1^1 and C_2^1. During ϕ_2, these two capacitors and

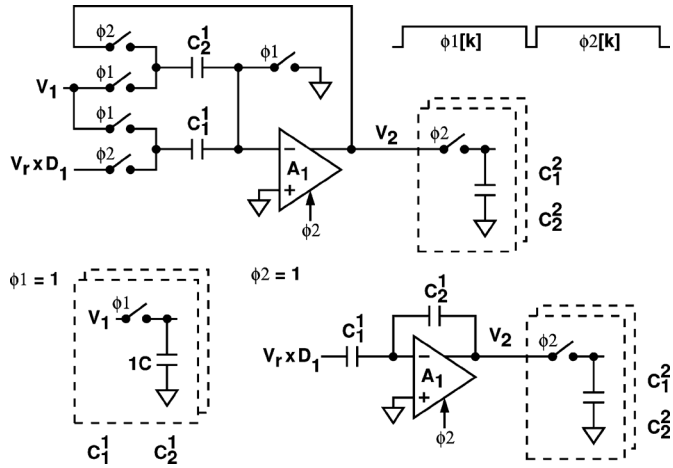

Fig. 4. A switched-capacitor MDAC.

opamp A_1 form a feedback amplifier. Its input is connected to a reference $V_r \times D_1$, which represents the sub-DAC function and can be easily realized with an analog demultiplexer. During ϕ_2, the opamp's output V_2 is sampled by C_1^2 and C_2^2 of the 2nd stage. If the opamp is ideal and $C_1^1 = C_2^1$, then V_2 is expressed by (1). This MDAC exhibits a residue gain of 2.

Any deviation of V_2 from (1) causes ADC conversion errors. The accuracy of the MDAC depends on the opamp as well as the capacitor ratio C_1^1/C_2^1. This paper does not cover the issue of capacitor matching. We assume all capacitors are large enough to satisfy a resolution requirement of at least 10 bits. There are several design considerations for the opamps, including dc gain, speed, noise, and power consumption. In addition, we want the opamps to provide a large output voltage range to relax the requirement for the sub-ADC and improve the signal-to-noise ratio (SNR) of the analog signal path.

In the following subsections, we will review several low-voltage amplification techniques that can be used to realize the MDAC function.

A. Cascaded Amplification

Under a low supply voltage, the opamp in Fig. 4 is usually a cascaded amplifier to provide enough dc gain. Fig. 5 shows a two-stage opamp in the MDAC configuration. The 1st stage of the opamp is modeled as a transconductance G_{m1} with an output resistance R_1. The 2nd stage is transconductance G_{m2} with an output resistance R_2. The G_{m2} stage needs a large output signal swing, while the output signal swing of stage G_{m1} is small. The dc gain of stage G_{m1} can be enhanced by using cascode. The Miller capacitor C_c is added to improve phase margin. This opamp is active during ϕ_2. Its allocated amplification time is T_a.

Due to the finite dc gain of the opamp, the output V_2 of the MDAC shown in Fig. 5 becomes

$$V_2 \approx V_{2,\text{ideal}} \times \left(1 - \frac{1}{L} \right) \tag{2}$$

where $L = G_{m1}R_1G_{m2}R_2 \times C_2/(C_1 + C_2)$ is the MDAC's dc loop gain. The product $G_{m1}R_1G_{m2}R_2$ is the opamp's dc gain and the ratio $C_2/(C_1+C_2)$ is the feedback factor of the MDAC.

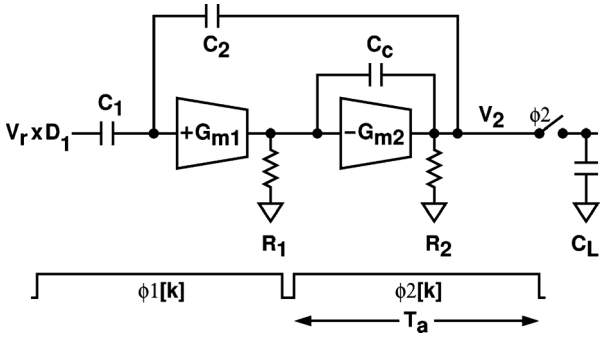

Fig. 5. Two-stage cascaded amplification.

The 1st stage G_{m1} is the major noise source of the opamp. The input-referred noises for G_{m1} can be expressed as $\overline{v_n^2}/\Delta f = 4kT(n_f/G_{m1})$ where n_f is a constant depending on circuit configuration. If $C_1 = C_2 = C_L = C$, $C_c = 0.5C$, then the total noise in V_2 is

$$\overline{V_{n,\mathrm{ca}}^2} = \frac{kT}{C} \times (2 + 4n_f)\,. \tag{3}$$

Consider a 10-bit 200-MS/s ADC design. Let the circuit shown in Fig. 5 be the first pipeline stage. The amplification time T_a is 2 nsec. Let $C_1 = C_2 = 300$ fF for 10-bit matching. Capacitor $C_L = 300$ fF is the combination of the C_1 and C_2 capacitors in 2nd stage. The compensation capacitor C_c is chosen to be 150 fF. To make the opamp settle during T_a time and meet the MDAC accuracy requirement, we want $G_{m1} = 1.04$ m℧ and $G_{m2} = 9.35$ m℧. Assume the power consumption of this opamp is proportional to G_{m1} and G_{m2}. The opamp can be turned off outside ϕ_2 to save power. Thus, its average power consumption can be expressed as

$$P_{avg,\mathrm{ca}} \propto G_{m,\mathrm{ca}} = \frac{G_{m1} + G_{m2}}{2} = 5.2\ \mathrm{m}\mho. \tag{4}$$

B. CDS Amplification

The correlated double sampling (CDS) technique has been used to relax the dc gain requirement for the opamp [28], [29]. Fig. 6 shows an MDAC using the CDS technique. It includes a single-stage opamp modeled as a transconductor G_m with an output resistor R. The opamp has a dc gain of $A_0 = G_m R$. During ϕ_1, input V_1 is sampled onto capacitors C_1 to C_4. The ϕ_2 amplification phase is split into ϕ_{2a} and ϕ_{2b}. During ϕ_{2a}, opamp G_m and capacitors C_3 and C_4 form an MDAC, generating V_{2c}. The opamp output V_{2c} can be expressed as

$$V_{2c} \approx V_{2,\mathrm{ideal}} \times \left(1 - \frac{1}{L_a}\right) \tag{5}$$

where $L_a = A_0 \times C_4/(C_3 + C_4 + C_5)$ is the loop gain of the MDAC during ϕ_{2a}. The opamp input, which is equal to $-V_{2c}/A_0$, is sampled onto C_5. During ϕ_{2b}, C_5 becomes an input-coupling capacitor with a voltage shift of V_{2c}/A_0. Neglect capacitor mismatch. The final V_2 is

$$\begin{aligned} V_2 &= V_{2,\mathrm{ideal}} - (V_2 - V_{2c}) \times \frac{1}{L_b} \\ &\approx V_{2,\mathrm{ideal}} \times \left(1 - \frac{1}{L_a L_b}\right) \end{aligned} \tag{6}$$

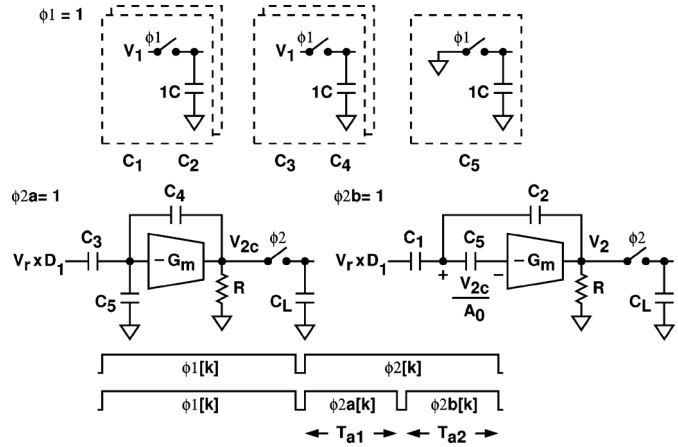

Fig. 6. A correlated-double-sampling (CDS) MDAC.

where $L_b = A_0 \times C_2/(C_1 + C_2)$ is the loop gain of the MDAC during ϕ_{2b}. Thus, this MDAC has an equivalent dc gain of $A_0^2 \times C_4/(C_3 + C_4 + C_5)$.

This CDS scheme is a coarse-fine two-step operation. During ϕ_{2a}, the MDAC makes a coarse estimation of $V_{2,\mathrm{ideal}}$, precharges the output capacitor C_L, and stores its estimation in C_5. During ϕ_{2b}, the MDAC needs only to make a fine adjustment from V_{2c} to its final output V_2.

One disadvantage of the CDS technique is that the same opamp must be used in both clock phases ϕ_{2a} and ϕ_{2b}. Thus, the opamp must satisfy both dc gain and output voltage range requirements, which may lead to a conventional 2-stage cascaded design. The other disadvantage is that the noise sampled on C_5 during ϕ_{2a} shows up in V_2 during ϕ_{2b} [30].

C. CLS Amplificatioin

The correlated-level-shifting (CLS) technique is also a coarse-fine two-step amplification scheme [30]–[34]. Fig. 7 shows an MDAC using the CLS technique. It includes two separate opamps. The coarse-stage opamp is modeled as a transconductor G_{mc} with an output resistor R_1. The fine-stage opamp is modeled as a transconductor G_{mf} with an output resistor R_2. During ϕ_1, input V_1 is sampled onto C_1 and C_2, and an additional capacitor C_3 is reset. During ϕ_{2a}, coarse-stage opamp G_{mc} and capacitors C_1 and C_2 form an MDAC. Its output V_{2c} is an estimate of $V_{2,\mathrm{ideal}}$ and can be expressed as (5) with a loop gain $L_a = G_{mc}R_1 \times C_2/(C_1 + C_2)$. The voltage V_{2c} is sampled onto C_3. During ϕ_{2b}, fine-stage opamp G_{mf} and capacitors C_1, C_2, and C_3 form an MDAC, generating output V_2. Opamp G_{mf} is coupled to V_2 through C_3. Its ouput V_{2f} is

$$V_{2f} = V_{2c} \times \frac{G_{mf}R_2}{G_{mc}R_1} \frac{1}{1 + L_b} \tag{7}$$

where

$$L_b = G_{mf}R_2 \times \frac{C_3}{(C_1 \| C_2) + C_3 + C_L} \times \frac{C_2}{C_1 + C_2} \tag{8}$$

is the MDAC's dc loop gain during ϕ_{2b}. The final V_2 can be expressed as

$$V_2 \approx V_{2,\mathrm{ideal}} \times \left(1 - \frac{1}{L_a L_a} - \frac{1}{L_a L_b}\right). \tag{9}$$

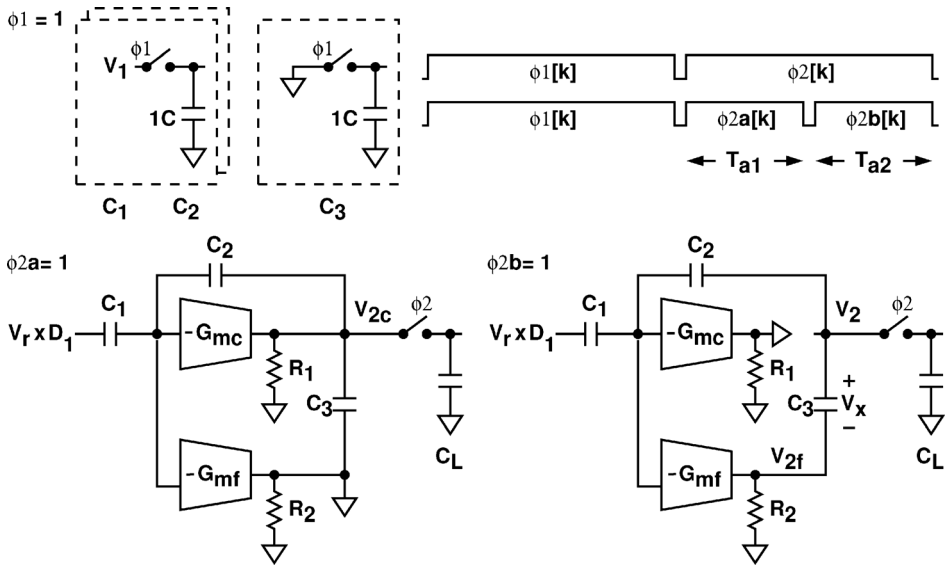

Fig. 7. A correlated-level-shifting (CLS) MDAC.

Comparing to (6), a CLS MDAC has an equivalent dc gain half of a value achieved by a CDS MDAC, if L_a approximates L_b.

During ϕ_{2a}, the MDAC using coarse-stage opamp G_{mc} makes a coarse estimation of $V_{2,\text{ideal}}$, precharges the output capacitor C_L, and stores its estimation V_{2c} on C_3. During ϕ_{2b}, the voltage across C_3, V_x, is added to the output V_2 directly. From (7), if $L_a \gg 1$ and $L_b \gg 1$, then V_x is close to V_{2c}, and the fine-stage opamp's output V_{2f} is small. Thus, opamp G_{mc} should be designed to have large output range and large slew rate, while opamp G_{mf} tolerates smaller output range and smaller slew rate and can be designed to possess larger dc gain. By optimizing opamps G_{mc} and G_{mf} separately, the CLS amplification can achieve better accuracy and speed performances than the CDS. Furthermore, the CLS amplification has a better noise performance than the CDS. In the CLS scheme, the noise sampled on C_3 during ϕ_{2a} is attenuated by the MDAC loop gain during ϕ_{2b} [30].

Note that, in the CLS scheme, both G_{mc} and G_{mf} opamps must remain active for the entire ϕ_2 period, leading to an overall power consumption similar to a cascaded 2-stage opamp design. As shown in Fig. 7, the inputs of G_{mc} and G_{mf} are tied together. During ϕ_2, any switching action on opamps G_{mc} and G_{mf} introduces kick-back charges injected to the input, resulting in errors in V_2. Thus, opamp G_{mf} cannot be turned off during ϕ_{2a} and opamp G_{mc} cannot be turned off during ϕ_{2b}.

D. Dual-Path Amplification

We propose a dual-path amplification technique for residue generation. Fig. 8 shows the 1st pipeline stage using the dual-path architecture. It includes a coarse-stage MDAC and a fine-stage MDAC. The coarse stage generates a residue V_{2c}, which may deviate from $V_{2,\text{ideal}}$ of (1) due to the non-ideal opamp in the MDAC. The fine stage also performs the normal MDAC function, but its output is subtracted by V_{2c}, yielding V_{2f}. The overall intended output V_2 is

$$V_2 = V_{2c} + V_{2f}. \tag{10}$$

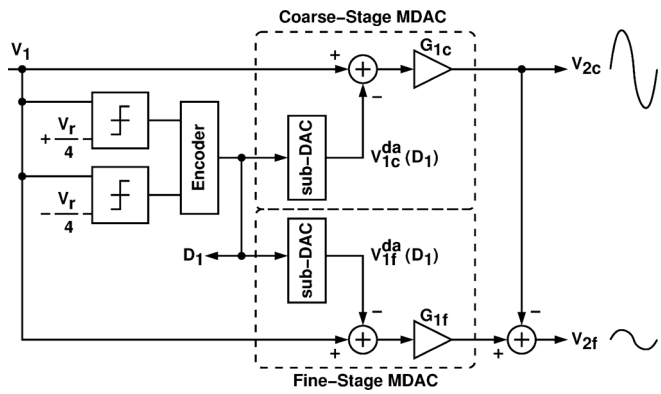

Fig. 8. A dual-path pipeline stage.

Voltage V_{2c} can be treated as an estimate of $V_{2,\text{ideal}}$. The difference between the ideal residue $V_{2,\text{ideal}}$ and V_{2c} is recovered by V_{2f}.

In this dual-path architecture, the coarse stage generates a large-swing signal to emulate $V_{2,\text{ideal}}$. The fine stage determines the accuracy and noise performances of the entire pipeline stage, but needs only to generate a small-swing signal. The opamps in these two stages have different requirements. They can be designed and optimized separately, leading to a better overall MDAC performance.

Fig. 9 shows a switched-capacitor dual-path MDAC. Similar to the CDS and CLS schemes, it also employs the coarse-fine two-step amplification technique. It includes a coarse-stage opamp G_{mc} and a fine-stage opamp G_{mf}. The ϕ_2 period is split into ϕ_{2a} and ϕ_{2b}. During ϕ_1, input V_1 is sampled onto capacitors C_1 to C_4, while C_5 is reset. During ϕ_{2a}, opamp G_{mc}, capacitors C_3 and C_4 are configured as a coarse-stage MDAC, generating output V_{2c}. Voltage $-V_{2c}$ is sampled onto capacitor C_5. A signal of negative polarity is easily available in a fully-differential circuit. During ϕ_{2b}, opamp G_{mf} and capacitors C_1 and C_2 are configured as a fine-stage MDAC, generating output V_{2f}. Voltage V_{2c} is subtracted from V_{2f} by connecting C_5 to the opamp's input, reducing the signal swing

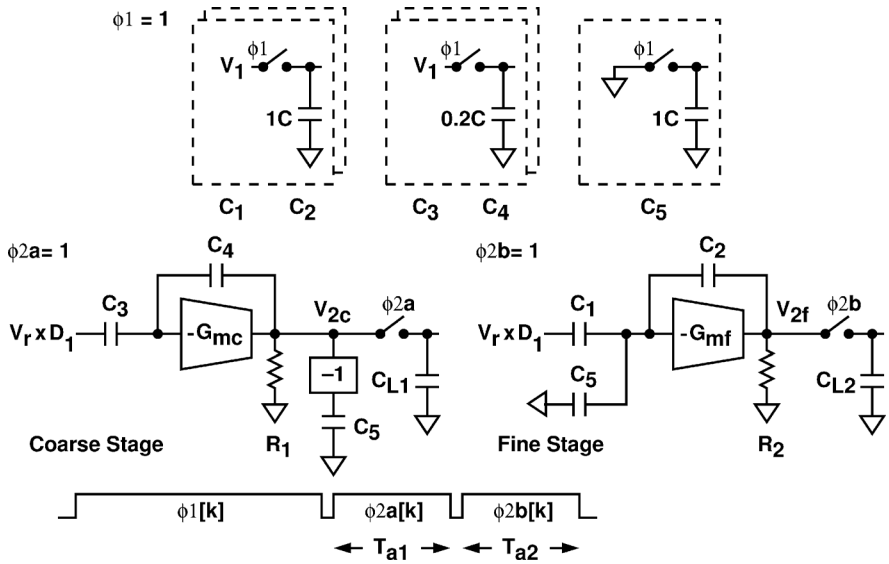

Fig. 9. A switched-capacitor dual-path MDAC.

of V_{2f}. Note that capacitors C_3 and C_4 can be much smaller than C_1, C_2, and C_5. This is because the coarse stage does not have stringent requirements for accuracy and SNR. Its error can be corrected by the fine stage.

Consider only the MDAC dc characteristic. Neglect capacitor mismatch. The coarse stage output V_{2c} can be expressed as (5) with a loop gain $L_a = G_{mc}R_1 \times C_4/(C_3 + C_4)$. The fine stage output can be expressed as

$$V_{2f} = (V_{2,\text{ideal}} - V_{2c}) \times \left(1 - \frac{1}{L_b}\right) \tag{11}$$

where the dc loop gain $L_b = G_{mf}R_2 \times C_2/(C_1 + C_2 + C_5)$. Then, the realized intended output is

$$V_2 = V_{2c} + V_{2f} \approx V_{2,\text{ideal}} \times \left(1 - \frac{1}{L_a L_b}\right). \tag{12}$$

Similar to the CDS and CLS cases, the effective gain error of the dual-path amplifier is $1/(L_a L_b)$. Comparing to (2), the dual-path amplifier has an equivalent dc gain similar to a 2-stage cascaded amplifier but reduced by a factor of $C_2/(C_1 + C_2 + C_5)$.

During ϕ_{2a}, the same thermal noise in V_{2c} is sampled onto capacitor C_5 and C_{L1}. During ϕ_{2b}, the voltage sampled on C_5 is subtracted from V_{2f}. In the next stage, the summation of V_{2c} and V_{2f} cancels most of the noise sampled on C_5 and C_{L1}, reducing the noise power from the coarse-stage MDAC by a factor of $1/L_b^2$. Thus, the fine-stage MDAC is the dominant noise source. The input-referred noises for G_{mf} is expressed as $\overline{v_n^2}/\Delta f = 4kT(n_f/G_{mf})$. If $C_1 = C_2 = C_5 = C$, $C_{L2} = 1.2C$, then the total noise in V_{2f} is

$$\overline{V_{n,\text{dp}}^2} = \frac{kT}{C} \times (1.6 + 1.6n_f). \tag{13}$$

Comparing (13) to (3), the dual-path amplifier has a better noise performance than a two-stage cascaded amplifier, unless the compensation capacitor C_c is increased. Note that the capacitance of C_{L2} is calculated based on the ADC architecture described in Section III. The capacitors in the following pipeline stage are scaled by half.

Assume clock phases ϕ_{2a} and ϕ_{2b} equally divide the ϕ_2 period, i.e., $T_{a1} = T_{a2} = T_a/2$ where T_a is the total amplification time in ϕ_2. At the end of ϕ_{2a}, the coarse stage output is

$$V_{2c}\left(\frac{T_a}{2}\right) \approx V_{2,\text{ideal}}\left[1 - e^{-(T_a/2)/\tau_c}\right] \tag{14}$$

where τ_c is the time constant of the coarse-stage MDAC. At the end of ϕ_{2b}, the fine stage output is

$$V_{2f}\left(\frac{T_a}{2}\right) \approx \left[V_{2,\text{ideal}} - V_{2c}\left(\frac{T_a}{2}\right)\right]\left[1 - e^{-(T_a/2)/\tau_f}\right] \tag{15}$$

where τ_f is the time constant of the fine-stage MDAC. Thus, the realized output V_2 at the end of ϕ_2 is

$$V_2 = V_{2c} + V_{2f} \approx V_{2,\text{ideal}}\left[1 - e^{-T_a/\tau_{eff}}\right] \tag{16}$$

where

$$\frac{1}{\tau_{eff}} = \frac{1}{2} \times \left(\frac{1}{\tau_c} + \frac{1}{\tau_f}\right). \tag{17}$$

The above equation illustrates that this dual-path amplifier has a settling accuracy similar to a single-path amplifier with an effective time constant of τ_{eff} and an amplification time of T_a. If $\tau_c = \tau_f$, then $\tau_{eff} = \tau_c = \tau_f$.

Consider a 10-bit 200-MS/s ADC design. Let the circuit shown in Fig. 9 be the first pipeline stage. The total amplification time T_a is 2 nsec. Both the coarse-stage amplification time T_{a1} and the fine-stage amplification time T_{a2} are equal to $T_a/2$. Let $C_1 = C_2 = C_5 = 300$ fF, $C_3 = C_4 = 60$ fF, and $C_{L1} = C_{L2} = 360$ fF. The pipeline architecture described in Section III requires larger capacitive loadings C_{L1} and C_{L2} than the C_L in the single-path amplifier. To make the dual-path

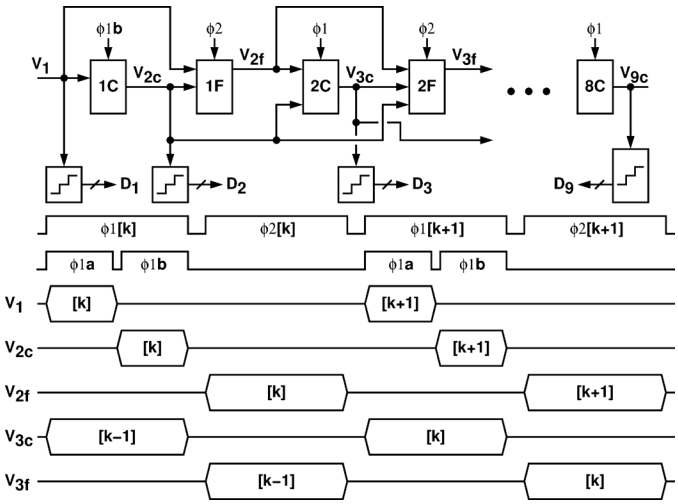

Fig. 10. Dual-path pipelined ADC architecture.

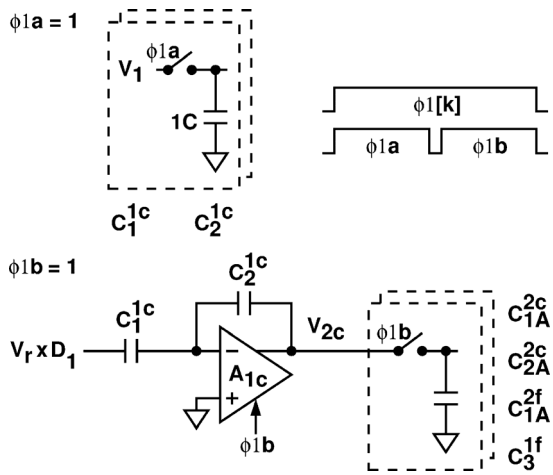

Fig. 11. Schematic and operation of stage 1C.

amplifier settle during overall T_a time and meet the accuracy requirement, we want $G_{mc} = 5.62\ \mathrm{m}\mho$ and $G_{mf} = 4.15\ \mathrm{m}\mho$. Assume the power consumption of the MDAC is proportional to G_{mc} and G_{mf}. The coarse stage needs to be turned on only during ϕ_{2a} and the fine stage needs to be turned on only during ϕ_{2b}. Thus, the average power consumption of the overall MDAC can be expressed as

$$P_{avg,\mathrm{dp}} \propto G_{m,\mathrm{dp}} = \frac{G_{mc} + G_{mf}}{4} = 2.4\ \mathrm{m}\mho. \qquad (18)$$

Comparing (18) to (4), the dual-path MDAC consumes only 50% of the power of a MDAC using a 2-stage opamp of similar settling accuracy.

Comparing to the CLS scheme, the dual-path amplification provides similar equivalent dc gain and noise performance. Opamps G_{mc} and G_{mf} demand similar specifications in both cases. The required G_{mc} and G_{mf} transconductances are similar for both cases to achieve the same settling accuracy. However, in the CLS scheme, both G_{mc} and G_{mf} must remain active during the entire ϕ_2 phase. Thus, a CLS MDAC consumes twice the power of a dual-path MDAC with similar performance.

III. Dual-Path Pipelined ADC Architecture

Fig. 10 shows a 10-bit pipelined ADC using the dual-path amplification technique described in Section II-D. Each conventional pipeline stage is split into a coarse stage and a fine stage. Consider the 1st pipeline stage. It is split into a coarse stage 1C and a fine stage 1F. Its input is V_1 and its two outputs are V_{2c} and V_{2f}. Clock ϕ_1 is split into ϕ_{1a} and ϕ_{1b}. Input V_1 is available during ϕ_{1a}. It is sampled by stages 1C and 1F, and is also quantized into code $D_1 \in \{-1, 0, +1\}$. Stage 1C is enabled during ϕ_{1b}. Its output V_{2c} is sampled by stage 1F and the 2nd stage. Stage 1F is enabled during the entire ϕ_2 period. Its output V_{2f} is sampled by the second stage.

Consider the 2nd pipeline stage, it is split into a coarse stage 2C and a fine stage 2F. Its two inputs are the coarse input V_{2c} and the fine input V_{2f}. Stage 2C samples $V_{2c}[k]$ during $\phi_{1b}[k]$ and $V_{2f}[k]$ during $\phi_2[k]$. Its output $V_{3c}[k]$ is generated during $\phi_1[k+1]$. Stage 2F samples $V_{2c}[k]$ during $\phi_{1b}[k]$, $V_{2f}[k]$ during $\phi_2[k]$, and $V_{3c}[k]$ during $\phi_1[k+1]$. Its output $V_{3f}[k]$ is generated during $\phi_2[k+1]$.

Excluding the 1st pipeline stage, all other pipeline stages employ the same architecture and the same timing scheme. Each stage has two inputs, a coarse input and a fine input. The effective input is the summation of the coarse input and the fine input. Each pipeline stage comprises a coarse stage and a fine stage. Both the coarse stage and the fine stage stage have an amplification time of half clock period in each clock cycle. Each pipeline stage includes a sub-ADC, which quantizes the coarse stage's output. The sub-ADC has the entire ϕ_2 period for quantization operation. Note that the design of the 1st pipeline stage is different. It receives only one input, V_1. Stage 1C has only the ϕ_{1b} period for amplification. The sub-ADC that quantizes V_1 has a quantizatioin time shorter than the ϕ_{1b} period.

Fig. 11 shows the stage 1C schematic and its operation. During ϕ_{1a}, input V_1 is sampled onto capacitors C_1^{1c} and C_2^{1c}. During ϕ_{1b}, it is configured as an MDAC using opamp A_{1c}. Its output V_{2c} is sampled by stage 1F and the second stage. To save power, the opamp A_{1c} is enabled only during ϕ_{1b}. Fig. 12 shows the stage 1F schematic and its operation. During ϕ_{1a}, input V_1 is sampled onto capacitors C_1^{1f} and C_2^{1f}. During ϕ_2, it is configured as an MDAC using opamp A_{1f}. Its output V_{2f} is sampled by the 2nd stage. The stage 1C output $-V_{2c}$ is sampled by capacitor C_3^{1f} during ϕ_{1b}. Capacitor C_3^{1f} is connected to opamp A_{1f} during ϕ_2 to subtract V_{2c} from the opamp's output. To save power, the opamp A_{1f} is enabled only during ϕ_2. The 10-bit resolution requirement of the 1st stage is segmented into a 6-bit requirement for opamp A_{1c} and a 4-bit requirement for opamp A_{1f}.

As shown in Fig. 10, stage 2C needs to generate V_{3c} during ϕ_1 while sampling V_{2c} during ϕ_{1b}. Two capacitor sets are required. Fig. 13 shows the schematic and operation of coarse stage 2C during cycle $[k]$. One capacitor set $(C_{1A}^{2c}, C_{2A}^{2c})$ samples $V_{2c}[k]$ during $\phi_{1b}[k]$, while the other capacitor set $(C_{1B}^{2c}, C_{2B}^{2c})$ is configured with opamp A_{2c} to form an MDAC during $\phi_1[k]$. During $\phi_2[k]$, the stage 2F output $V_{2f}[k]$ is sampled onto capacitor C_3^{2c}. Fig. 14 shows the stage 2C schematic and its operation during cycle $[k+1]$. During $\phi_1[k+1]$, capacitor set $(C_{1A}^{2c}, C_{2A}^{2c})$, capacitor C_3^{2c}, and opamp A_{2c} form an MDAC. The MDAC has

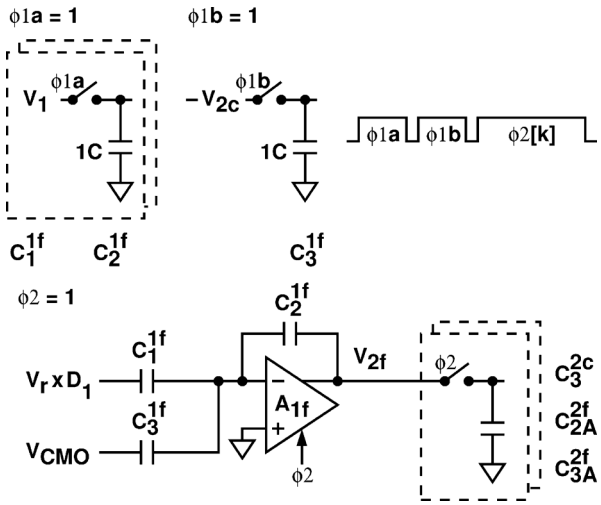

Fig. 12. Schematic and operation of stage 1F.

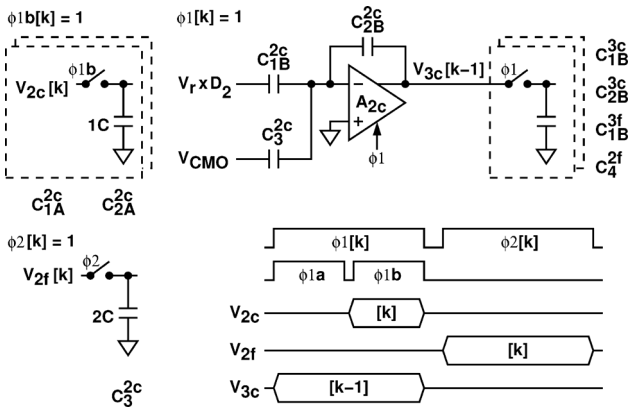

Fig. 13. Schematic and operation of stage 2C during clock cycle $[k]$.

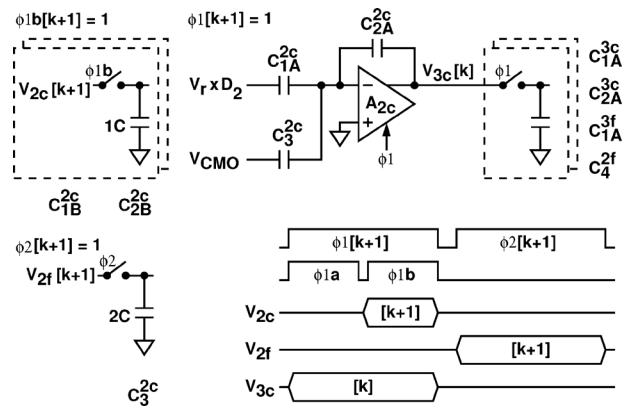

Fig. 14. Schematic and operation of stage 2C during clock cycle $[k+1]$.

an effective input of $V_{2c}[k] + V_{2f}[k] - (V_r/2)D_2$ and a corresponding output $V_{3c}[k]$. The other capacitor set $(C_{1B}^{2c}, C_{2B}^{2c})$ now samples $V_{2c}[k+1]$ during $\phi_{1b}[k+1]$. The MDAC output $V_{3c}[k]$ is sampled by stage 2F and the 3rd pipeline stage.

Stage 2F shares similar design principle with stage 2C. Stage 2F needs to generate V_{3f} during ϕ_2 while sampling V_{2f} at the same time. Furthermore, the V_{2c} sampled in clock cycle $[k]$ is used to generate the V_{3f} in clock cycle $[k+1]$. Two capacitor sets are required. Each capacitor set contains three capacitors.

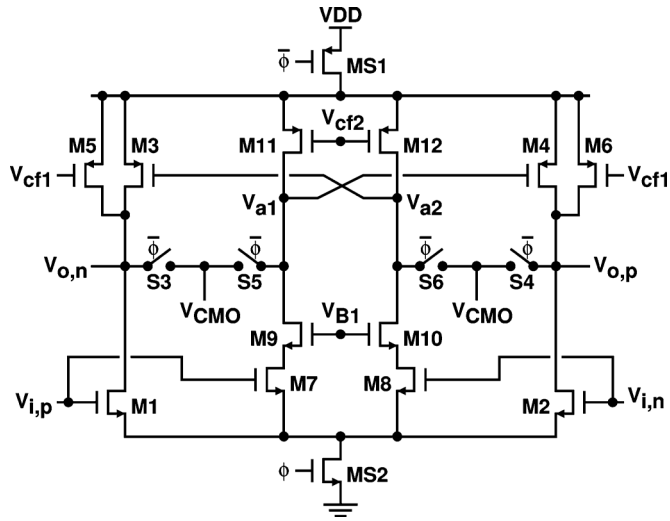

Fig. 15. Coarse-stage opamp schematic.

Within each clock cycle, one set samples V_{2c} and V_{2f}, while the other set is configured with opamp A_{2c} to form an MDAC. There is an additional capacitor, which samples $-V_{3c}$ during ϕ_1. It is also connected to opamp A_{2c} during ϕ_2 to complete the stage-2F MDAC.

IV. Circuit Details

The dual-path pipelined ADC described in Section III has been realized using 65 nm CMOS technology. It was designed to operate under a single 1 V supply. This section describes circuit details.

A. Coarse-Stage Opamp

Fig. 15 shows the coarse-stage opamp schematic. It consists of two parallel signal paths [35]. As shown in Fig. 16, A1 represents the common-source amplifiers M1 and M2, A2 represents the telescopic amplifiers M7 to M12, and A3 represents the common-source amplifiers M3 and M4. Path A has a higher dc gain than path B due to the additional amplification provided by A2. However, A2 contributes a dominant pole at frequency f_{p1}. Both A1 and A3 contribute poles at the same frequency f_{p2}, since their outputs are tied together. The signals from the two path are summed at the output V_o, creating a zero at frequency f_z. By careful placing the poles and zero, the compensation capacitor can be eliminated, results in a low power design.

Not shown in Fig. 15 are two continuous-time common-mode feedback (CMFB) circuits, generating biases V_{cf1} and V_{cf2}. To facilitate power control, this opamp is activated by ϕ through MOSFET switches MS1 and MS2, and CMOS switches S3 to S6. When ϕ is low, the opamp is turned off, nodes V_{a1}, V_{a2}, $V_{o,p}$, and $V_{o,n}$ are tied to a dc voltage V_{CMO} to eliminate the memory effect and improve turn-on time. When activated, this opamp takes only 0.17 nsec to turn on. To reduce glitches at outputs, S3 to S6 are turned off after MS1 and MS2 are turned on.

In stage 1C, this opamp consumes 0.87 mW when activated, among which the A2 telescopic amplifiers M7–M12 consume only 0.07 mW. The opamp has a dc gain of 49 dB. The frequencies of the poles and zero shown in Fig. 16 are $f_{p1} = 3.7$ MHz,

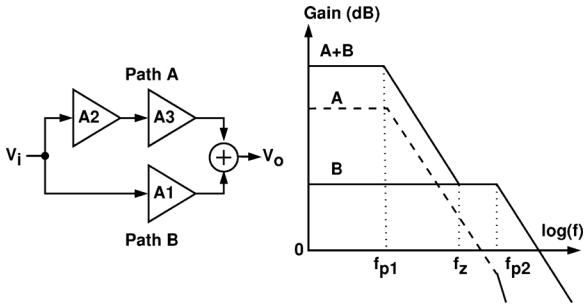

Fig. 16. Coarse-stage opamp architecture.

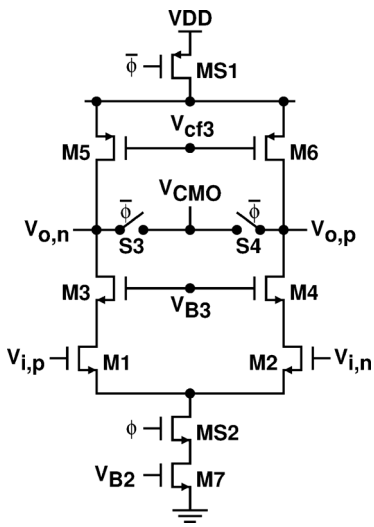

Fig. 17. Fine-stage opamp schematic.

$f_{p2} = 54.6$ MHz, and $f_z = 44.3$ MHz. When used in stage 1C, the resulting MDAC has a loop-gain unity frequency of 530 MHz and a phase margin of 67°.

This opamp exhibits several sources of errors. It is not completely settled at the end of its allocated amplification time. This is mainly due to the slow settling of the pole-zero doublet [36], [37]. There are extra noises introduced by the A2 telescopic amplifier. The opamp is not capable of input common-mode rejection. Input common-mode variation may lead to variation in the output. Most of the errors in the coarse stage are corrected by the corresponding fine stage.

B. Fine-Stage Opamp

Fig. 17 shows the fine-stage opamp. It is a single-stage differential telescopic amplifier. A large output voltage range is not required. A continuous-time CMFB circuit is used to generate V_{cf3}. To facilitate power control, this opamp is activated by ϕ using MOSFET switches MS1 and MS2. When ϕ is low, the opamp is turned off, nodes $V_{o,p}$ and $V_{o,n}$ are tied to a dc voltage V_{CMO} through CMOS switches S3 and S4. When activated, this opamp takes only 0.14 nsec to turn on. To reduce glitches at outputs, S3 and S4 are turned off after MS1 and MS2 are turned on.

In stage 1F, this opamp consumes 0.52 mW when activated. It has a dc gain of 29 dB. When used in stage 1F, the resulting MDAC has a loop-gain unity frequency of 510 MHz and a phase margin of 110°.

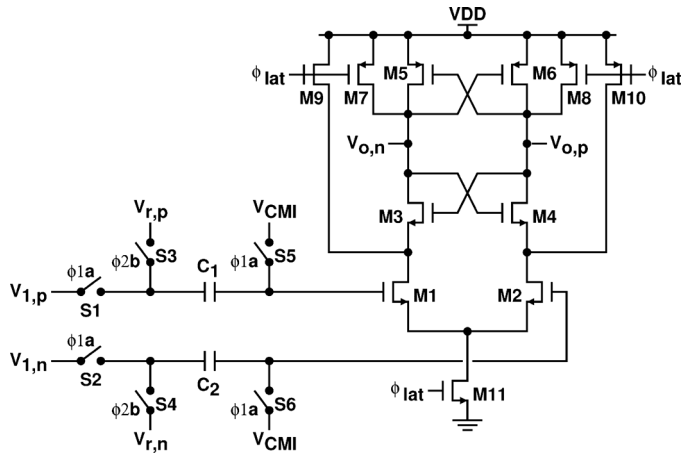

Fig. 18. Schematic of the comparators in the first sub-ADC.

The capacitances of the capacitors in the fine stages are chosen to meet the matching requirements. The resulting kT/C noise is much smaller than the ADC resolution.

C. Comparator

As shown Fig. 10, the ADC input V_1 and the outputs of the coarse stages are quantized by the corresponding sub-ADCs. Each sub-ADC consists of two comparators. Fig. 18 shows the schematic of the comparators in the 1st sub-ADC that quantizes V_1. The comparator comprises a switched-capacitor input sampling network and a regenerative latch. To save power, there is no amplifier or buffer between the sampling network and the latch. The latch offset is tolerated by the MDAC redundancy. The sampling capacitors C_1 and C_2 are both 30 fF. Each comparator consumes an average power of 5 μW at 200 MS/s sampling rate.

The analog input of this ADC is sampled directly by the first pipeline stage. No additional sample-and-hold amplifier is used. The sample-and-hold operations is synchronized for the sampling capacitors C_1^{1c} and C_2^{1c} in Fig. 11, the capacitors C_1^{1f} and C_2^{1f} in Fig. 12, and the capacitors C_1 and C_2 in Fig. 18. All the V_1 sampling switches controlled by clock ϕ_{1a} are bootstrapped n-channel MOSFET switches [38].

For the other sub-ADCs, the operation of the sampling network of the comparator is modified. The sampling capacitors C_1 and C_2 in Fig. 18 are first precharged to $V_{r,p}$ and $V_{r,n}$ respectively, then they become the input-coupling capacitors for the latch and connect to the outputs of a coarse-stage opamp. This arrangement can reduce the total input capacitance of a sub-ADC as seen by the coarse-stage opamp.

V. Experimental Results

The ADC was fabricated using a standard 65 nm CMOS process. Fig. 19 shows the chip micrograph. It has an active area of 0.19 mm^2, including clock generator and encoder. All capacitors are standard metal-oxide-metal (MOM) capacitors. The chip was mounted directly on a circuit board for testing. Voltage references are externally supplied.

Table I lists the power consumption of the opamps at 200 MS/s sampling rate. Also listed are the unit capacitances in different stages defined in Section III. Capacitors and opamps are

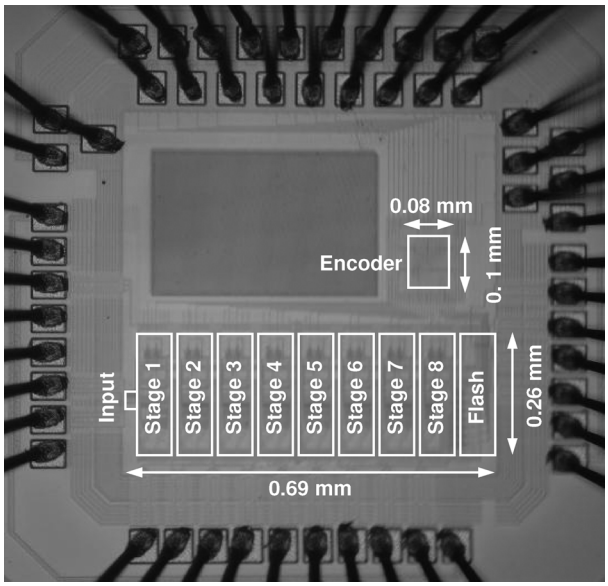

Fig. 19. ADC chip micrograph.

TABLE I
POWER CONSUMPTION OF OPAMPS.

Stage	1C	1F	2C	2F	3C–8C	3F–7F
C (fF)	60	300	40	200	30	130
Act. Power (mW)	0.87	0.52	0.55	0.43	0.39	0.29
Avg. Power (mW)	0.23	0.29	0.30	0.23	0.21	0.16

scaled along the ADC pipeline. Aggressive scaling was not pursued due to design time constraint. In Table I, the active power is the power consumption of the opamp when enabled, while the average power is the power consumption of the opamp averaged over the entire clock period. The opamp in stage 1C is enabled for 1/4 of a clock period, thus, its average power is about 1/4 of the active power. The opamps in other stages are enabled for 1/2 of a clock period, thus, their average power is about 1/2 of the active power. At 200 MS/s sampling rate, the total power consumption of the ADC is 5.37 mW, among which the opamps consume 3.11 mW, the comparators consume 0.11 mW, the digital encoder consumes 0.36 mW, and the clock drivers consume 1.55 mW.

Fig. 20 shows the measured differential nonlinearity (DNL) and integral nonlinearity (INL). The maximum DNL is $+0.08/-0.38$ LSB, and the maximum INL is $+1.36/-1.29$ LSB.

Fig. 21 shows the measured output spectra at 200 MS/s sampling rate. The upper plot is obtained with a 1-MHz 1.3-V_{pp} sinewave input. Digital output is collected off-chip with a down-sampling ratio of 8. The signal-to-noise-plus-distortion ratio (SNDR) is 57 dB and the spurious-free dynamic range (SFDR) is 64 dB. The lower plot is obtained with a 99-MHz 1.3-V_{pp} sinewave input. The measured SNDR and SFDR are 55 dB and 59 dB respectively. There are time-interleaving capacitor sets in all pipeline stages except the 1st stage. The mismatches between the capacitor sets can introduce spurious tone at $f_s/2 - f_{in}$. In Fig. 21, this spurious tone is less than -75 dB, much less than the 3rd-order harmonic tone.

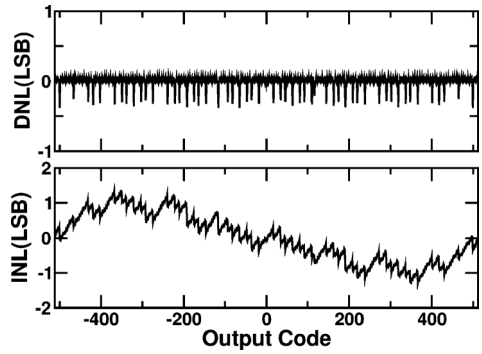

Fig. 20. Measured DNL and INL.

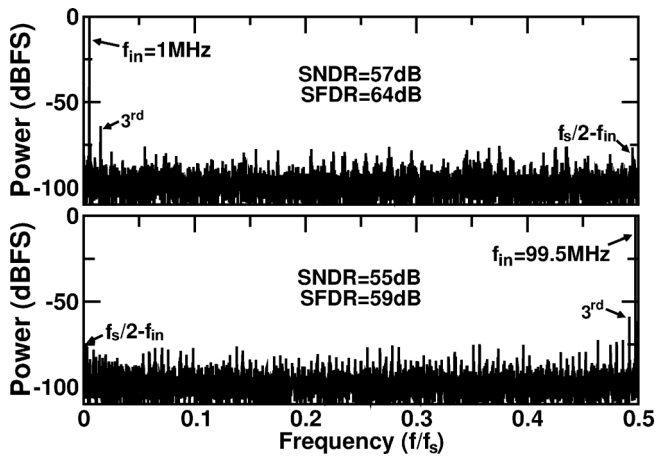

Fig. 21. Measured output spectra.

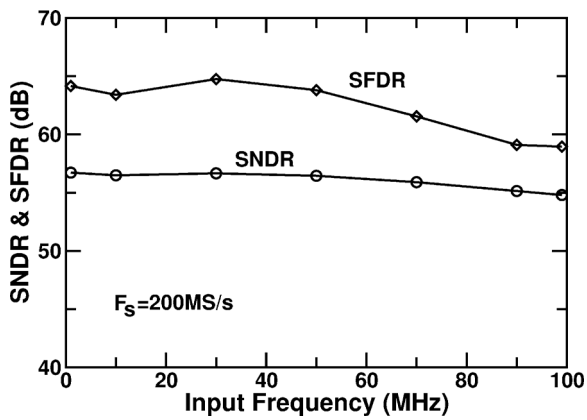

Fig. 22. Measured dynamic performance versus input frequency.

Fig. 22 shows the dynamic performance versus input frequency measured at 200 MS/s sampling rate. The measured effective resolution bandwidth (ERBW) is above 100 MHz.

Table II is the ADC performance summary. This ADC consumes 5.37 mW from a 1 V supply. The differential input signal range is 1.3 V_{pp}. The figure-of-merit (FOM) is defined as

$$\text{FOM} = \frac{\text{Power}}{2^{\text{ENOB}} \times \min\{2\text{ERBW}, f_s\}}. \tag{19}$$

TABLE II
ADC PERFORMANCE SUMMARY.

Technology	CMOS 65 nm
Power Supply	1 V
Differential Input Range	1.3 V_{pp}
Input Capacitance (Per Pin)	720 fF
Resolution	10 Bits
Sampling Rate f_s	200 MS/s
DNL	+0.08/-0.38 LSB
INL	+1.36/-1.29 LSB
SNDR @ f_{sig} = 1 MHz	57.1 dB
SNDR @ f_{sig} = 99 MHz	54.8 dB
Power Consumption	5.37 mW
Core Area	0.19 mm^2
FOM	48 fJ/conv.-step

TABLE III
ADC PERFORMANCE COMPARISON.

Reference	[6]	[7]	[39]	[9]	This Work
Architecture	Pipe	Pipe	SAR	TI-Pipe	Pipe
Technology (nm)	90	90	65	40	65
Supply (V)		1	1.2	1/2.5	1
f_s (MS/s)	500	100	100	800	200
SNDR (dB)	53	55	59	59	56.7
SFDR (dB)		67.4	76.5	70	64.2
ENOB (Bits)	8.51	8.84	9.51	9.51	9.13
ERBW (MHz)	233	50	50	400	100
Power (mW)	55	4.5	1.13	105	5.37
FOM (fJ/conv-step)	300	98	15.5	180	48
Active Area (mm^2)	0.49	0.058	0.026	0.88	0.19

where f_s is the sampling rate, and ENOB is the effective number of bits at low input frequency, defined as $\mathrm{ENOB} = [\mathrm{SNDR(dB)} - 1.76]/6.02$. Table III compares this ADC with other 10-bit ADCs that achieve $\geq 100\ \mathrm{MS/s}$ sampling rate. It shows that the pipelined ADCs can achieve a competitive FOM at high sampling rate.

VI. CONCLUSIONS

Signal amplification is a fundamental analog function. Accurate high-speed amplification becomes more difficult in nanoscale CMOS technologies and under a low supply voltage. The coarse-fine two-step amplification technique provides an alternative amplification scheme. It decomposes the intended signal into two separate signals of different properties. It facilitates the use of switching opamps with fast turn-on time to save power. In the pipeline stage design, the use of time-interleaving capacitor sets increases the amplification time for the opamps, leading to further power saving. We designed a 5.37-mW 10-bit 200-MS/s pipelined ADC to demonstrate the above techniques.

ACKNOWLEDGMENT

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Yun Chai (S'11) was born in Taipei, Taiwan. She received the B.S. degree from the department of electrical engineering, National Cheng-Kung University (NCKU), Tainan, Taiwan, and the M.S. degree from the department of electronics engineering, National Chiao-Tung University (NCTU), Hsin-Chu, Taiwan. Since then, she has been pursuing the Ph.D degree at the NCTU. She has been engaged in the design of mixed signal IC design, especially in the field of pipelined ADC. Her current research is low-power data converters.

Jieh-Tsorng Wu (S'83–M'87–SM'06) was born in Taipei, Taiwan. He received the B.S. degree in electronics engineering from National Chiao-Tung University, Hsin-Chu, Taiwan, in 1980, and the M.S. and Ph.D. degrees in electrical engineering from Stanford University, Stanford, CA, in 1983 and 1988, respectively.

From 1980 to 1982 he served in the Chinese Army as a Radar Technical Officer. From 1982 to 1988, at Stanford University, he focused his research on high-speed analog-to-digital conversion in CMOS VLSI. From 1988 to 1992 he was a Member of Technical Staff at Hewlett-Packard Microwave Semiconductor Division in San Jose, CA, and was responsible for several linear and digital giga-hertz IC designs. Since 1992, he has been with the Department of Electronics Engineering, National Chiao-Tung University, Hsin-Chu, Taiwan, where he is now a Professor. His current research interests are high-performance mixed-signal integrated circuits.

Dr. Wu is a member of Phi Tau Phi. He has served as an Associate Editor of the IEEE JOURNAL OF SOLID-STATE CIRCUITS.