On-Current Decrease After Erasing Operation in the Nonvolatile Memory Device With LDD Structure

Geng-Wei Chang, Ting-Chang Chang, Yong-En Syu, Ya-Hsiang Tai, and Fu-Yen Jian

***Abstract*—The on-current decrease phenomenon is observed after erasing operation in the silicon–oxide–nitride–oxide–silicon thin-film transistors (TFTs) with lightly doped drain (LDD) structure. As nonvolatile memory, when the TFT is programmed again, the on-current decrease phenomenon can be recovered. The on-current decrease and recovery are explained by the energy band diagrams at different drain biases. The explanation implies that this phenomenon only appears in the device with LDD structure, but not in the device without LDD structure, which is experimentally verified.**

***Index Terms*—Lightly doped drain (LDD), nonvolatile memory, on-current decrease, silicon–oxide–nitride–oxide–silicon thin-film transistor (SONOS TFT).**

I. Introduction

SILICON–oxide–nitride–oxide–silicon (SONOS) technology has been considered as a replacement for floating gate nonvolatile memory due to the simple structure and process, low voltage operation, and its immunity to extrinsic charge loss [1], [2]. Silicon nitride and its interface with silicon dioxide provide an alternative for this charge storage where the highly localized storage of charge at an increased number of sites may allow a further scaling of the insulator thickness [3]. The scaling of SONOS devices also offers improved performance with a small cell size. However, the short-channel effect owing to the scaling down arises from the high electric field in the channel region [4]–[7]. High electric fields cause undesired hot-carrier injection into the oxide, leading to oxide charging and subsequent threshold-voltage shift. The lightly doped drain (LDD) structure is a solution to avoid this effect, which not only increases breakdown voltage [8] but also reduces impact ionization (and thus hot-electron emission) by spreading the high electric field at the drain pinchoff region into the n-region [9], [10]. In addition, the SONOS memory and display switch devices can be integrated on the same glass substrate for a potential system-on-panel technology. This approach will make a display more compact and reduce both the fabrication and the assembly costs. However, conventional poly-Si thin-film transistors (TFTs) suffer from an anomalous OFF-state leakage current, namely, gate-induced drain leakage (GIDL), which increases with gate voltage [11], [12]. The leakage hinders poly-Si TFTs being used as switching devices in applications [13], [14]. Therefore, the poly-Si TFT with LDD structure is one of the most promising candidates for the switching elements in future high-performance large-area active matrix liquid crystal displays because the LDD structure can effectively suppress the leakage current to less than 1 pA/pixel [15], [16]. However, an on-current decrease phenomenon is observed after erasing operation in SONOS TFT memory devices with LDD structure. In this letter, we investigate the on-current decrease phenomenon and explain it with energy band diagrams. According to the explanation, this phenomenon only takes place in LDD devices, which is verified by the device without LDD structure subject to the same programming/erasing operation.

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II. Experimental Setup

The devices for this study are n-channel SONOS TFTs with the top gate and LDD structure. The detailed fabrication procedures are as follows. A silicon oxide buffer layer and a 50-nm-thick undoped amorphous-Si (a-Si) film were deposited sequentially by plasma-enhanced chemical vapor deposition at 380 °C, followed by dehydrogenation via a furnace annealing process at 450 °C. Then, the a-Si film was crystallized by a 308-nm XeCl excimer laser with a line-shaped beam power of 350 mJ/cm^2. After the active region was patterned by plasma dry etching, the source/drain regions as well as the LDD regions were defined by a mask and formed by a mass-separated ion implanter technique. The LDD implant was done with 60 keV$/10^{13}$ cm^{-2}, and the LDD length is 1.25 μm. The stack of ONO gate consists of 40-nm top oxide, 20-nm silicon nitride, and 10-nm bottom (tunneling) oxide, respectively. The electrical properties of SONOS TFTs with $L = 6$ μm and $W = 6$ μm were analyzed by using an Agilent 4156-C and Agilent B-1500 system. For comparison, the n-channel SONOS TFTs without LDD structure are also made and investigated.

III. Results and Discussion

Fig. 1(a) shows the evolution of the transfer characteristics (I_D–V_G) of a SONOS TFT for different erasing times. Before

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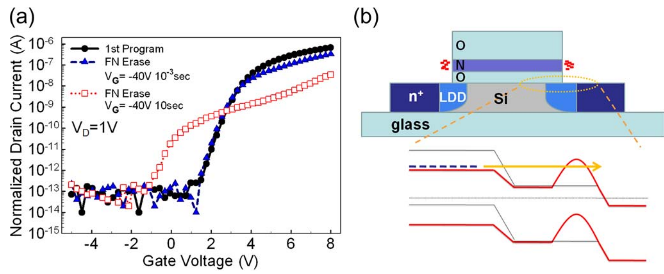

Fig. 1. (a) I_D–V_G curves of SONOS TFT with LDD structure for different erase times. (b) Corresponding electron distribution and the energy band diagram near the drain region after erase.

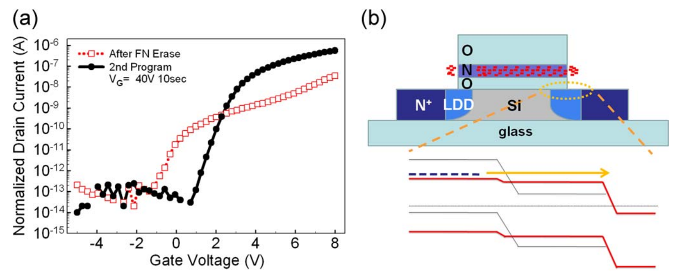

Fig. 2. (a) Transfer characteristics of SONOS TFT before and after the second program operation. (b) Energy band diagram after the second program operation.

the erasing operation, the memory device was programmed by a gate bias of 40 V for 10 s. Thus, electrons are injected from the channel through the tunnel oxide to the nitride layer by Fowler–Nordheim (FN) tunneling because of the gate-bias-induced high electron field [17]. After the erasing operation at a gate bias of -40 V for 10^{-3} s, it is found that the curve shifts left slightly and the on current decreases. For the FN erasing process, the mobility of holes is slower than that of electrons because the effective mass of holes is heavier than that of electrons [18], [19]. As short as 10^{-3} s of the erasing time, only very few carriers can tunnel through the oxide barrier. Extending the erasing time to 10 s, the transfer curve largely shifts from 2 to -0.2 V, and the on current significantly decreases from 6.61×10^{-7} to 3.47×10^{-8} A. The electrons trapped at the storage layer are uniformly distributed in the nitride layer above the channel as well as the LDD region after the FN programming operation. After the erasing operation, only the trapped electrons above the channel area are erased, but those above the LDD region still remain, as shown in Fig. 1(b). On the other hand, the trapped electrons, above the LDD region, are hardly erased because LDD greatly suppresses the electron field induced by the gate bias. The charge above the area of the LDD region results in the curvature in the energy bands, and thus the potential barriers, which impedes the movement of free carriers from source to drain. Even though the inversion channel region is still induced by the gate voltage, the electrons existing at the area above the LDD region in the nitride layer make carrier transport from source to drain more difficult. In addition, it can be seen that the device exhibits good retention for 10^4 s at 150 °C with no significant decline in the memory window. Therefore, the charge was mainly trapped in the nitride layer rather than in the bottom oxide.

The on-current decrease phenomenon can be recovered by the proceeding programming operation, as shown in Fig. 2(a). After the FN tunneling programming process at the gate bias of 40 V for 10 s, the curve shifts back, and the on current is restored. Electrons injected from the channel to the nitride layer by FN tunneling are distributed uniformly. The height of the potential barrier above the area of the LDD region is no more increased because of the locally trapped carriers in the storage layer, as shown in Fig. 2(b). Therefore, the programming operation restores the smoothness of the carrier transport, and the on-current decrease phenomenon is recovered.

To confirm the role of the potential barrier above the area of the LDD region, the transfer characteristics of the SONOS TFT

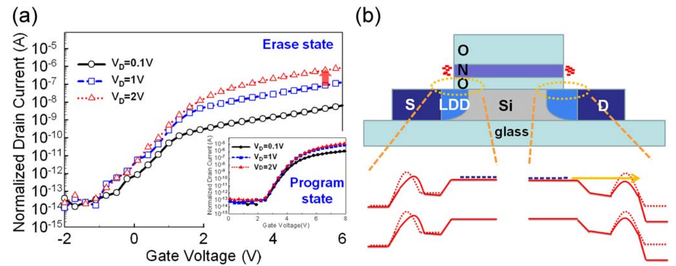

Fig. 3. (a) I_D–V_G curves of SONOS TFT at the different V_D's at the erase state. Inset shows those curves at program state. (b) Energy band diagram at the different V_D's at erasing state.

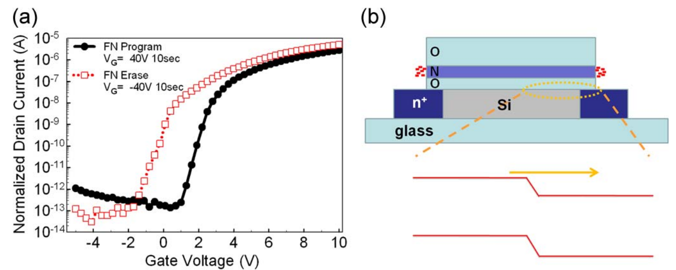

Fig. 4. (a) Transfer characteristics of SONOS TFT without LDD structure at program/erase states. (b) Energy band diagram at erasing state.

at the different V_D's are shown in Fig. 3(a). At the erasing state, the drain current rises with increasing V_D. In the saturation region, when V_D increases from 1 to 2 V, the drain current raises significantly. The potential barrier is lowered by the exerted drain bias, as shown by the energy band diagram in Fig. 3(b). It is attributed to the fact that the movement of electrons from source to drain is impeded in the area of the LDD region. As for the programming state, the band is flat above the area of the LDD region. The on current only raises a little, while V_D increases from 1 to 2 V, as shown in the inset in Fig. 3(a).

In order to confirm the effect of LDD, we measured the memory device without LDD structure. The results are shown in Fig. 4(a). At the programming state, the transfer curve is the same as that of the device with LDD structure. After the erasing operation, the transfer characteristic shifts left in the same way. However, the on-current decrease phenomenon does not appear. For the device without LDD structure, since electrons are gathered above the area of the drain terminal, the barrier has no effect on the carrier transportation from source to drain, as shown in Fig. 4(b).

IV. Conclusion

In conclusion, the on-current decrease phenomenon for SONOS TFTs with LDD structure has been discussed in this letter. After the next operation of programming, this on-current decrease can be recovered. The role of the potential barrier in the area of the LDD region has been explained. It is verified by varying V_D under both the programming and erasing states. It is further verified by comparing the results of the devices with and without LDD structure subject to the same programming/erasing operation. Even though the LDD device possesses the advantage of suppressing GIDL, the on-current decrease after the erasing operation becomes a drawback in the application.

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