Novel Dielectric-Engineered Trapping-Charge Poly-Si-TFT Memory With a TiN–Alumina–Nitride–Vacuum–Silicon Structure

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***Abstract*—High-performance poly-Si-TFT-based TiN–alumina–nitride–vacuum–silicon (TANVAS) trapping-charge memory has been demonstrated utilizing high-k blocking oxide and vacuum tunneling layer for the first time. In particular, the vacuum, lowest k in nature, was introduced to replace the traditional tunneling oxide. Furthermore, the alumina high-k blocking oxide was applied to upgrade the electric field across the tunneling layer. Based on the enlarged k-value difference between the blocking and tunneling layers, the TANVAS featured considerable field enhancement across the tunneling layer, thus much improving the program/erase efficiencies. In addition, owing to the suppression of defect creation in the tunneling layer, the TANVAS also exhibited superior retention characteristics. These excellent memory characteristics of TANVAS are therefore promising for the 3-D Flash and system-on-panel applications.**

***Index Terms*—Field-enhanced nanowire (FEN), high-k, poly-Si, system-on-panel (SOP), thin-film transistors (TFTs), trapping-charge memory.**

I. Introduction

THE silicon–oxide–nitride–oxide–silicon (SONOS)-type nonvolatile memory devices based on the poly-Si thin-film transistor (TFT) techniques have been extensively investigated for the realization of 3-D integrated circuits and system-on-panel (SOP) [1], [2]. In order to improve their inherent insufficient program/erase (P/E) speed, lots of device architectures were proposed to enhance the electric field across the tunneling layer via the sharp corner features [3], [4]. However, most of them were still required larger operation voltage to achieve a reasonable memory window, which seriously restricted TFT SONOS applications.

Recently, the adoption of high-k material as top blocking layer has been a practical scheme to reveal the low P/E voltage for single-crystalline-Si SONOS memory [5]. With raising the k-value difference between blocking and tunneling layers, the electric field across the tunneling oxide could be promoted more effectively [6], [7]. Nevertheless, rare research works demonstrated such dielectric engineering on poly-Si-TFT memories. In this letter, we proposed a novel poly-Si-TFT-based TiN–alumina–nitride–vacuum–silicon (TANVAS) memory device with field-enhanced nanowire (FEN). In addition to the high-k blocking oxide, the lowest k vacuum in nature was introduced to replace traditional tunneling oxide to further enhance the k-value difference between the tunneling and blocking layers. Furthermore, due to being immune against the defect creation in the tunneling layer, TANVAS exhibited much-improved retention characteristics as well. As a result, both the P/E speed and retention reliability could be significantly improved by means of TANVAS device structure.

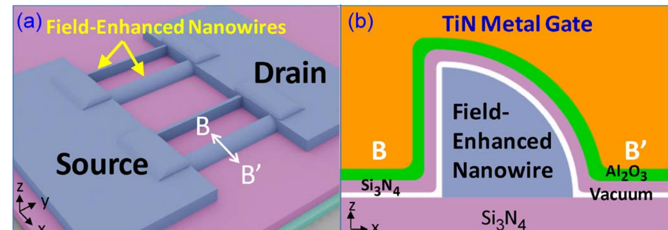

Fig. 1. Schematic diagrams of the key fabrication process steps of the proposed TANVAS. (a) FEN structure was formed after the removal of 100-nm-thick TEOS oxide strips by using diluted HF. (b) Cross-sectional schematic figure of fabricated TANVAS device with substituted vacuum tunneling layer [shown along the BB′ direction of (a)].

II. Device Fabrication

Based on our previous works, the fabrication process of poly-Si-TFT TANVAS memory device with FEN structure was schematically shown in Fig. 1 [8]–[10]. A 1.0-μm-thick thermal SiO_2 was first grown on a single-crystal silicon wafer as starting substrate. Next, an etch-stop layer of Si_3N_4 (50 nm thick) and a sacrificial layer of TEOS SiO_2 (100 nm thick) were sequentially deposited through the low-pressure chemical vapor deposition (LPCVD) system. The sacrificial SiO_2 layer was then etched as several dummy strips by reactive ion etch (RIE) process, followed by a layer of 100-nm-thick amorphous silicon film deposited at a temperature of 550 °C. After the source/drain (S/D)-pad lithography and its RIE process, pairs of a-Si sidewall spacers were *in situ* resided against the sidewalls of SiO_2 dummy strips and naturally connected to the S/D pads. The a-Si film was then transferred into the poly-Si by solid phase

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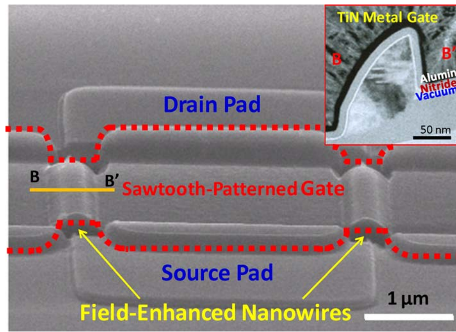

Fig. 2. SEM image of poly-Si-TFT TANVAS memory device after the removal of tunneling oxide. The inset plot shows the XTEM image of fabricated TANVAS device with substituted vacuum tunneling layer along the BB′ direction.

crystallization at 600 °C for 24 h in N_2 ambient. Next, the FEN structure was formed after etching the 100-nm-thick TEOS SiO_2 strips by using diluted HF, as shown in Fig. 1(a). Afterward, a 3-nm-thick TEOS SiO_2 film and an 11-nm-thick Si_3N_4 film were deposited sequentially by LPCVD as the tunneling and charge-trapping layers, respectively. Then, an 11-nm-thick Al_2O_3 film was deposited by metal–organic chemical vapor deposition system at 500 °C as the blocking layer. Behind the deposition of stacked gate dielectrics, a 300-nm-thick TiN metal gate was deposited by physical vapor deposition. Following the gate patterning, it should be noted that only the TiN gate, Al_2O_3 blocking layer, and Si_3N_4 trapping layer were etched by RIE, while the 3-nm-thick TEOS SiO_2 film still remained on the poly-Si nanowires. After the phosphorous ion implantation (at 40 keV to a dose of 5×10^{15} cm^{-2}) and the S/D activation, a 300-nm-thick Si_3N_4 layer was deposited and then etched back by RIE to form Si_3N_4 spacers. Because the Si_3N_4 spacers wrapped around the Al_2O_3 blocking layer, they were capable of preventing the Al_2O_3 from damage by the following wet etching. Next, the tunneling oxide was side etched off with diluted buffered oxide etch (BOE), and then, 400-nm-thick passivation oxide was deposited by SiH_4-based PECVD system to form a vacuum tunneling layer. The cross-sectional schematic figure of TANVAS device with substituted vacuum tunneling layer is shown in Fig. 1(b). Fig. 2 shows the scanning electron microscopy (SEM) image of poly-Si-TFT TANVAS memory device after the removal of tunneling oxide. The TANVAS with sawtooth-patterned gate was particularly designed to ensure that the gate would not collapse as the TEOS tunneling oxide was etched. By controlling the BOE immersion time, only the tunneling oxide above the nanowire channel region was side etched off, while most tunneling oxide below the broader area of the pattern gate could be remained to support the gate without collapsing. Finally, the contact hole opening and metallization completed the device fabrication.

For comparison, the TiN–alumina–nitride–oxide–silicon (TANOS) FEN devices with traditional oxide tunneling layer were also manufactured by the same process flow. The inset plot of Fig. 2 shows the cross-sectional transmission electron microscopy (XTEM) image of fabricated TANVAS device along the BB′ direction. The FEN structure with vacuum tunneling layer could be obviously seen after the removal of tunneling oxide and SiH_4-based passivation oxide deposition.

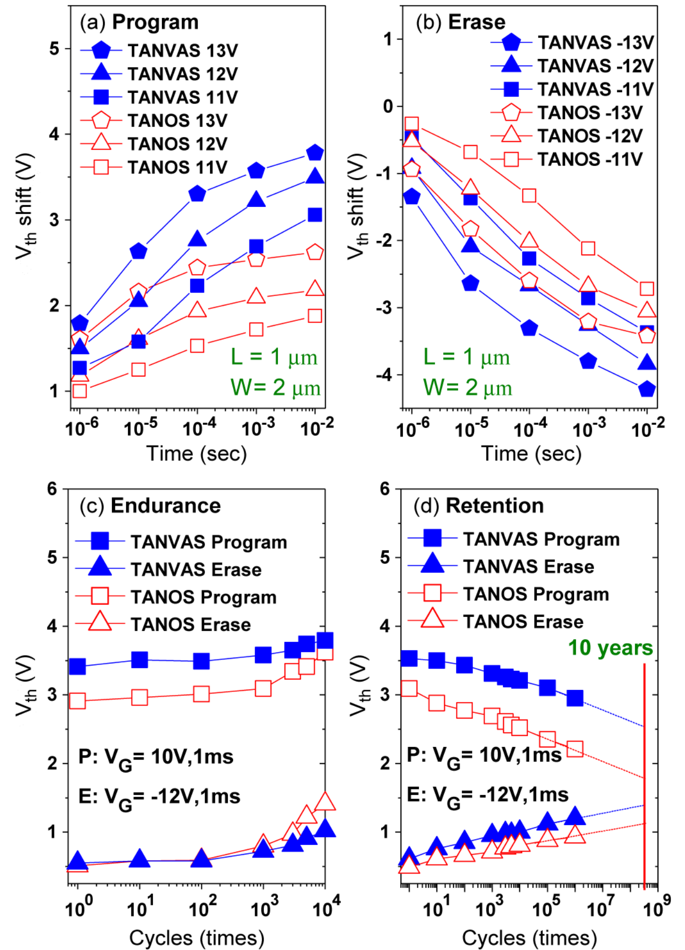

Fig. 3. (a) Threshold voltage (V_{th}) shift comparison of TANVAS and TANOS devices at a program bias (P) from 11 to 13 V. (b) V_{th} shift comparison of TANVAS and TANOS devices at an erase bias (E) from −11 to −13 V. (c) Endurance and (d) 85 °C retention characteristics of TANVAS and TANOS devices.

III. Results and Discussion

The memory devices with a channel length (L) of 1 μm and a channel width (W) of 2 μm were employed in this work. The subthreshold swing (SS) extracted from I_{DS}–V_{GS} curves were 243 and 249 mV/dec for the TANVAS and TANOS devices, respectively. It is well known that the SS is a parameter to monitor the device interface characteristics between channel and gate dielectric. Thus, the introduction of vacuum tunneling layer would not strongly degrade the Si/vacuum interface. The P/E efficiencies for both TANVAS and TANOS memory devices were characterized by means of the Fowler–Nordheim tunneling mechanism. Fig. 3(a) shows the threshold voltage (V_{th}) shift comparison of TANVAS and TANOS devices with various program times at an applied gate voltage of 11–13 V. The TANVAS exhibited a greater V_{th} shift of 3.78 V in 10 ms at a gate voltage of 13 V as compared to 2.62 V for the TANOS one. Likewise, Fig. 3(b) shows the similar trend that the TANVAS device had a faster erase speed than the TANOS counterparts. This indicated that the P/E efficiencies could be markedly upgraded by the introduction of vacuum tunneling layer. Since the vacuum was a lowest k value material in nature, the use of a low-k tunneling layer and high-k blocking oxide will simultaneously result in an increased electric field across

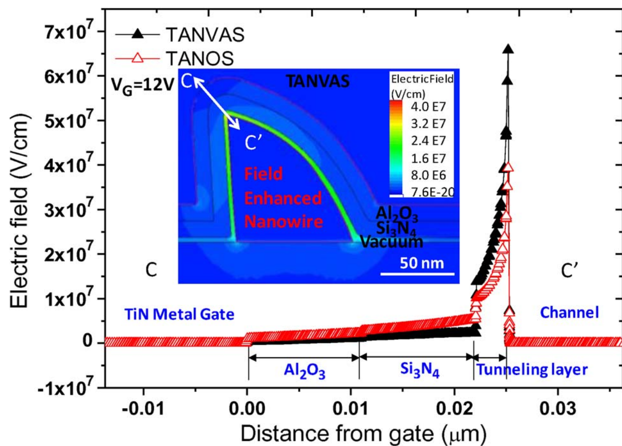

Fig. 4. Simulation results of electric-field distribution along the sharp corner for both TANVAS and TANOS across the stacked gate dielectrics.

the tunneling layer and an inhibitive feature at the blocking oxide. Therefore, more carriers could be injected from the poly-Si channel into the nitride layer for such field-enhancement scheme. The TANVAS memory structure enhanced the k-value difference between the blocking/tunneling layers, leading to an effective improvement of P/E speed. The endurance characteristics of TANVAS and TANOS devices are shown in Fig. 3(c). The good endurance performance of TANVAS was mainly contributed to the prevention of defect generation within the tunneling dielectric. Fig. 3(d) shows the data retention of both devices at 85 °C. The memory window of the TANVAS was about 1.2 V after extrapolating to retention time of ten years, whereas the TANOS one was only 0.65 V. This degradation could be ascribed to the defect creation in the relatively poor quality of low-temperature-deposited tunneling TEOS oxide. Defects in the tunneling oxide would create the leakage path so that the stored charges in the nitride could flow across the tunneling layer simply. In contrast, due to the empty property of vacuum tunneling layer, TANVAS could immunize against the defect creation and thereby well kept the data storage. Fig. 4 shows the simulated electric-field distribution along the sharp corner for both TANVAS and TANOS devices. The tunneling layer materials put a great influence on the electric-field distribution across the stacked gate dielectrics. As expected, the local electric field of tunneling layer could be further promoted via TANVAS structure at the same gate bias of 12 V. It was noticed that the maximum electric field was increased from 3.94×10^7 to 6.58×10^7 V/cm as the k-ratio of blocking/tunneling layers was increased from 2.3 (TANOS) to 9 (TANVAS). Consequently, the TANVAS device could acquire a better charge-trapping efficiency in the nitride layer, which is consistent with the experimental results.

IV. Conclusion

In this letter, a novel trapping-charge poly-Si-TFT memory with TANVAS FEN device structure has been proposed for the first time. By replacing the low-temperature tunneling oxide as the vacuum, the TANVAS devices exhibited a larger V_{th} shift of 3.78 V in 10 ms as compared to 2.62 V for the corresponding TANOS ones at an applied gate voltage of 13 V. These remarkable improvements could be attributed to the local electric-field enhancement of tunneling layer as raising the k-value ratio of the blocking/tunneling layers. Moreover, the better retention reliability for the TANVAS was ascribed to the empty feature of vacuum tunneling layer. Therefore, such a TANVAS memory is very promising for the 3-D Flash memory and SOP applications.

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