Foreword for the Special Issue on ESD Technology

THE CHALLENGES and complexity for ESD protection design are ever increasing with each new technology or as newer applications are introduced. To keep up with some of the latest developments, we have chosen to represent four invited papers with different focus areas. The first three are revised papers that were presented at the 2011 EOS/ESD Symposium, while the final ESD paper is an invited review paper to describe ESD protection design issues in state-of-the-art high voltage devices.

The first paper from the EOS/ESD Symposium is from S.-H. Chen *et al.* (IMEC) and it is about ESD robustness of GaN-on-Si Schottky diodes. The GaN technology on Si is very promising for power applications, also by virtue of low cost integration. ESD performance as Schottky Diodes for > 100 V applications is an important issue. The physics of the device behavior under both forward and reverse ESD-stress modes is explained in detail.

The second paper from Monnereau *et al.* (CNRS LAAS) investigates the probability of susceptibility failures due to ESD in systems. Whereas much of the focus of ESD protection has been on the IC component level, the failures at the system level are currently receiving the much needed amount of attention since the various electronic applications have become ubiquitous. Specifically, ESD events that can cause microprocessor failures are studied in terms of system susceptibility. The influence of external parameters on the probability of failure and the prediction model for this issue are discussed.

Following the same line of focus on system level ESD, the third Symposium paper by Diatta *et al.* (STM and University of Toulouse) investigates the statistical tools to analyze the stress test response variations from the ESD protection structures. This is important since the ESD Gun tests would require multiple stress events that would have variations in the pulse giving rise to cause variations of the device response.

The final invited paper by Srivastava and Gossner (Intel Mobile Communications) presents a comprehensive overview on DEMOS ESD phenomena. With increasing integration of high voltage analog applications into SoC designs, DEMOS devices are particularly sensitive to exhibit low ESD failure thresholds mainly because of the poor parasitic bipolar behavior compared to the standard low voltage MOSFET devices. As a result, there has been an intense research and development activity on the physics of these high voltage devices, in their various forms for different voltage applications. The paper gives a meticulous overview that should be of interest to the readers.

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