AIP | Applied Physics Letters

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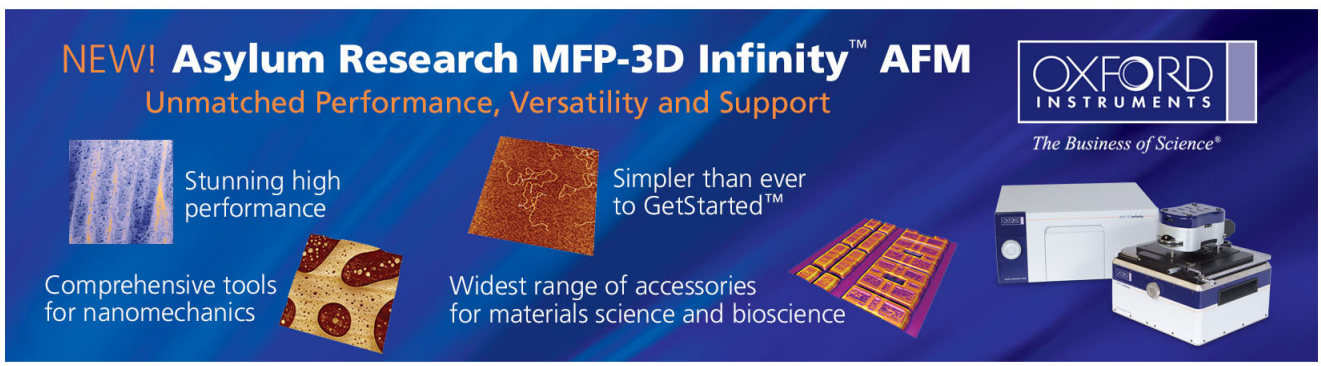
Citation: Applied Physics Letters **101**, 223502 (2012); doi: 10.1063/1.4767996
View online: http://dx.doi.org/10.1063/1.4767996
View Table of Contents: http://scitation.aip.org/content/aip/journal/apl/101/22?ver=pdfcov
Published by the AIP Publishing



The suppressed negative bias illumination-induced instability in In-Ga-Zn–O thin film transistors with fringe field structure

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(Received 14 September 2012; accepted 4 November 2012; published online 26 November 2012)

This study investigates the suppressed negative gate bias illumination stress (NBIS) -induced instability of via-type amorphous indium-gallium-zinc-oxide (a-IGZO) thin film transistors (TFTs) with fringe field (FF) structures. The less negative threshold voltage shifts of devices after NBIS are showed when device has larger FF structures. This finding is attributed to more dispersive distribution of photo-generated holes in the width direction of a-IGZO during NBIS, which reduce the hole trapping phenomenon in the front channel interface. The a-IGZO TFT with FF structure is expected to be an effective method to increase the electrical reliability of devices after NBIS. © *2012 American Institute of Physics*. [http://dx.doi.org/10.1063/1.4767996]

Amorphous metal oxide-based semiconductors (AOSs) have demonstrated the benefits of applications as thin film transistors (TFTs) in next generation displays due to their superior electrical performance, visible light transparency, and tunable carrier concentrations even when deposited at room temperature.[1,2] In particular, because of their high electron mobility and uniform electrical characteristic, all multi-functional devices can be integrated into a display by employing AOSs, known as "system-on-glass."[3–5]

During the past few years, amorphous indium-gallium-zinc-oxide (a-IGZO) has been intensively studied for adoption as the channel material in TFTs to replace amorphous silicon, especially for large area display applications (e.g., more than 55 in.).[6] The a-IGZO TFTs can offer high field effect mobility and low off-state current, which fit the high frame rate and lower power consumption requirements for displays. Although a-IGZO TFTs have demonstrated excellent performance, there are still some reliability problems in these devices.[7–9] When an a-IGZO TFT is used as the pixel switch in a liquid crystal display (LCD), the device normally experiences off-state bias (or negative gate bias) and inevitable back-light illumination.[10] Therefore, the instability of a-IGZO TFTs under negative gate bias illumination stress (NBIS) has became a crucial subject of study and has been reported to be induced by two main mechanisms: photo generation of ionized oxygen vacancies and trapping of photo-generated hole carriers at the channel/insulator interface.[10,11] The generated ionized oxygen vacancies usually accompanies a raised drain current (I_D) in the off state or an increase of subthreshold swing (SS). However, because the photo-generated hole trapping phenomenon is inherent for devices under NBIS, a practical device structure which diminishes this phenomenon is vital to study.

Previous studies have attributed the channel-length-dependent threshold voltage (V_T) shift of a-IGZO TFTs after NBIS to the increased lateral electric field difference between the source and drain electrodes as channel length decreases;[12] however, the influences of fringe structure on the electrical characteristics and stability of via-type a-IGZO TFTs have not yet been reported. Therefore, this study examines the electrical characteristics and the mechanism of electrical instability under NBIS of a-IGZO TFTs with fringe field (FF) structures. In addition, the decreased electrical instability of devices with an FF structure may provide a method to reduce the NBIS-induced electrical instability of a-IGZO TFTs.

Staggered bottom gate via-type a-IGZO TFTs are fabricated on glass substrate in this study. First, after a 150-nm-thick Mo film deposition as gate electrodes by sputtering, a 300-nm-thick SiO_x film is deposited as gate insulator using plasma enhanced chemical vapor deposition (PECVD). Then, a 50-nm-thick a-IGZO film was deposited as channel layers by sputtering at room temperature, using a target of In:Ga:Zn = 1:1:1 atomic ratio. A 200-nm-thick SiO_x etching stop layer was deposited by PECVD at 200 °C. The source (S)/drain (D) electrodes were formed by sputtering 150-nm-thick Mo. A 200-nm-thick SiO_x/SiN_x film was deposited as the passivation layer using PECVD. The channel width and length dimensions are defined as the width of S/D via-contact with IGZO, and the distance between the S and D via-contacts, respectively; both are about 10 μm. Finally, the devices were annealed in an oven at 240 °C in atmospheric ambient for final annealing. All electrical characteristic measurements were performed in the dark at room temperature using an Agilent B1500 semiconductor parameter analyzer. The threshold voltage (V_T) was determined by the constant current method as the gate voltage (V_G), which induces a I_D of 1 nA, and SS is determined by the equation of $SS = dV_{GS}/d(\log I_D)$ (V/dec) in the current range of 10^{-10} and 10^{-9} A. The light illumination of 10 000 lux intensity in

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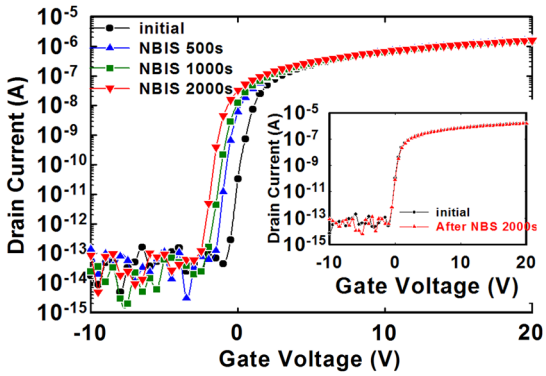

FIG. 1. Transfer I_D-V_G characteristics of a-IGZO TFT after NBIS for 2000 s. The inset shows the I_D-V_G characteristics of a-IGZO TFT after negative gate bias stress without light illumination.

this work was obtained by a halogen lamp whose spectrum is shown in the inset of Fig. 3(b).

Fig. 1 shows the instability of devices under NBIS with constant V_G of −30 V and grounded S and D. During and after NBIS, I_D-V_G shows continuously parallel negative shifts without increasing off state I_D or varying in SS, which indicates no defect generation. Under light illumination, electron-hole pairs can be generated from subgap photon excitation due to the existence of large deep-subgap density of states in a-IGZO.[10] Moreover, negative bias stress in a-IGZO TFTs makes holes drift toward the channel/insulator interface and become trapped in the preexisting interface traps, resulting in the negative V_T shift. A rare V_T shift after negative gate bias stress without illumination is observed in the inset of Fig. 1. This result suggests that the phenomenon of decreased hole trapping in a-IGZO TFTs after negative bias stress in the dark is due to quite low mobility of holes in a-IGZO, unless under illumination.[1]

In the application of an a-IGZO TFT as a panel switch in a display, devices experience not only off state (or negative gate bias stress) and light illumination but also positive drain bias.[12] Thus, NBIS with positive drain voltage (V_D) of 10 V, and a grounded S was applied to the device, which shows the I_D-V_G curves in Fig. 2(a). In addition, Fig. 2(b) shows the I_D-V_G curves with interchanged S and D (reverse I_D-V_G) during and after the NBIS. While the I_D-V_G and reverse I_D-V_G curves after NBIS with V_D show the same behavior of parallel negative V_T shifts, the reverse I_D-V_G demonstrates smaller shift. Also, the comparison of delta V_T after NBIS both with and without V_D is performed as shown in the inset of Fig. 2(a). The delta V_T of I_D-V_G after NBIS shows smaller negative shift than after NBIS with V_D; conversely, the reverse I_D-V_G shows larger negative V_T shifts than after NBIS with V_D. This result implies that holes may not be dispersed uniformly in a-IGZO under the NBIS with V_D. During the NBIS, the drain voltage causes a lateral electrical field from drain to source electrodes, which results in an asymmetrical distribution of the photo-generated holes. The mechanism on the asymmetrical hole trapping phenomenon can be explained by the band diagram along the channel direction, as shown in the inset of Fig. 2(b). Even the vertical electrical field is larger in a-IGZO near the drain region; more hole trapping can be expected near the S region due to the drain-bias-induced lateral electrical field in a-IGZO, which results in asymmetrical hole trapping in the device. Because the V_T of TFT is governed by the S barrier for electrons, the reduced hole trapping in the channel/insulator interface near the D region produces the smaller negative V_T shifts in the reverse I_D-V_G curves.

In this study, the a-IGZO TFTs with FF structures are investigated by varying the μm/side, as shown in the inset of Fig. 3(a). The μm/side is the measurement of the additional a-IGZO region extending from the S and D via-contacts along the width direction. This distance is measured as three μm/side values extending away from the via-contacts, as shown by blue arrows. Fig. 3(a) compares I_D-V_G curves measured in linear region with drain voltage (V_D) = 0.5 V for devices with different μm/sides and the same S or D via-contact size, and shows slight change. Although the area of the a-IGZO layer is increased in width as the μm/side increases, the I_D is dominated by the S or D via-contact size rather than the channel layer area. Moreover, the total capacitance of the device increases slightly by about 6 percent as the FF structure increases from 3 μm/side to 16 μm/side, as shown in the Fig. 3(b).

According to these results, the distribution of photo generated holes may be influenced by the electrical field in the channel layer. The I_D-V_G and reverse I_D-V_G curves for devices with a larger FF structure after NBIS with V_D are shown in Figs. 4(a) and 4(b), respectively. Although the larger negative parallel shift in I_D-V_G than in reverse I_D-V_G is still observed, smaller V_T shifts in I_D-V_G for larger FF structure devices is compared in Fig. 4(c). Apparently, negative V_T shifts are suppressed when the FF structure is increased. In literature, this phenomenon can be interpreted by the different potential between the channel layer with or without a S/D overlapped region in the width direction of a-IGZO.[13] The less hole trapping phenomenon in the front channel

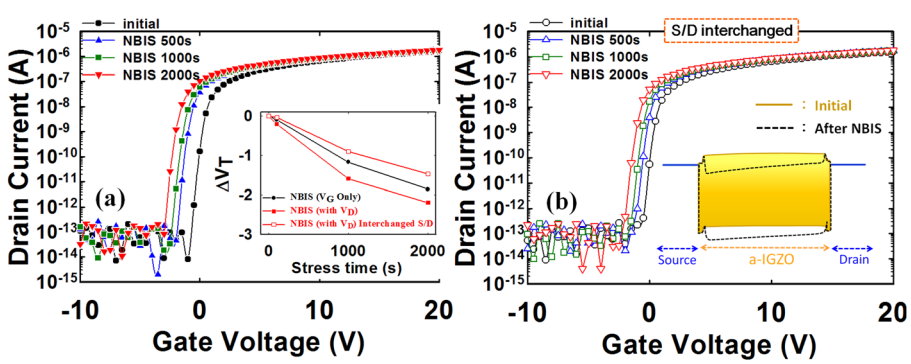

FIG. 2. (a) Transfer I_D-V_G characteristics of a-IGZO TFTs after NBIS with V_D for 2000 s. The inset shows delta V_T of I_D-V_G and reverse I_D-V_G characteristics during and after NBIS with and without V_D. (b) I_D-V_G characteristics of a-IGZO TFTs with interchanged S/D after NBIS with V_D for 2000 s. The inset shows the band diagram along the channel direction before and after NBIS with positive drain bias.

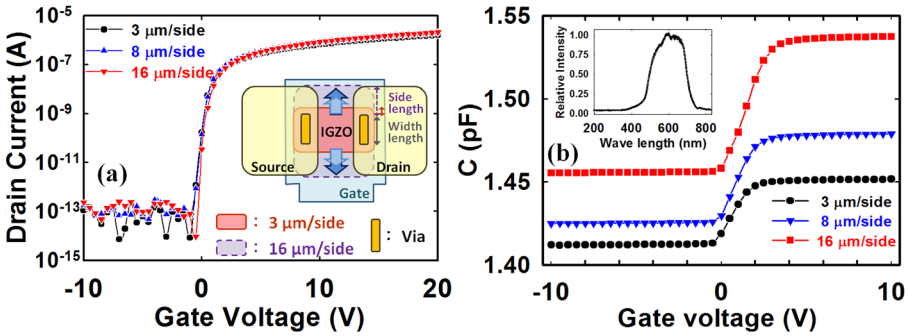

FIG. 3. (a) Transfer I_D-V_G characteristics of a-IGZO TFTs with 3 μm/side, 8 μm/side, and 16 μm//side FF structures. The inset shows the schematic top view of a fabricated a-IGZO TFT (b) The comparisons of total capacitance for devices with 3 μm/side, 8 μm/side, and 16 μm/side FF structures. The inset shows the illumination spectrum of the halogen lamp.

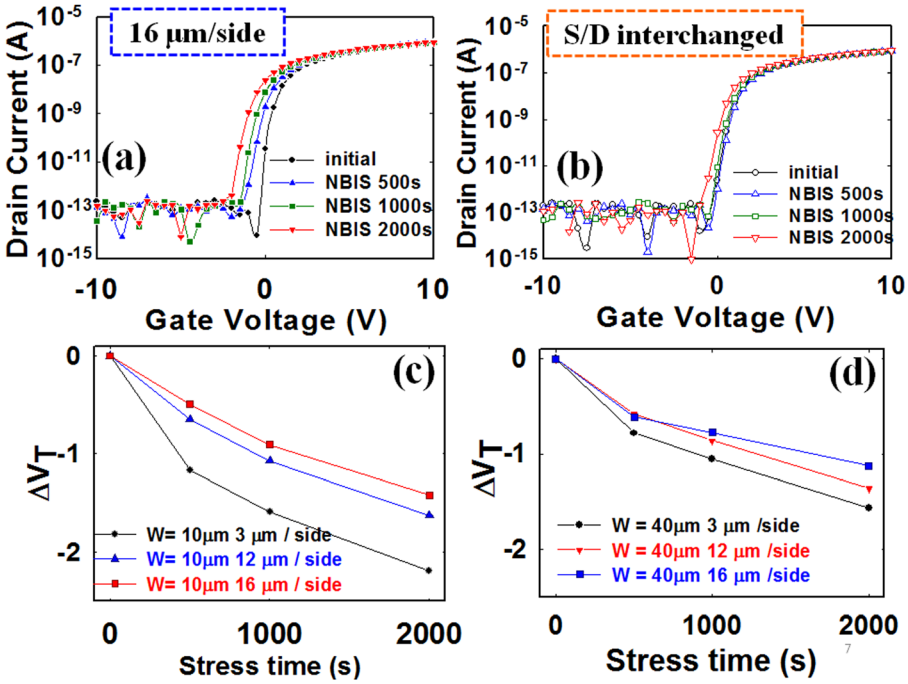

FIG. 4. (a) I_D-V_G characteristics of a-IGZO TFTs with 16 μm/side FF structure after NBIS with V_D for 2000 s. (b) I_D-V_G characteristics of 16 μm/side-FF-structure a-IGZO TFTs with interchanged S/D after NBIS with V_D for 2000 s. (c) The delta V_T of I_D-V_G characteristics of device with width/length 10/10 μm and 3 μm/side, 12 μm/side, and 16 μm/side FF structures during and after NBIS with V_D. (d) The delta V_T of I_D-V_G characteristics of device with width/length 40/10 μm and 3 μm/side, 12 μm/side, and 16 μm/side FF structures during and after NBIS with V_D.

interface can be attributed to more dispersive distribution of photo-generated holes in the width direction of a-IGZO during NBIS due to without the fixed potential of the back interface by the S/D. To assess the above model, the dependence of instability on the FF structure for device with larger width was still demonstrated. Fig. 4(d) shows the decreased change in delta V_T of a-IGZO TFTs with increased width of device and the same FF structure devices, which is less shift than the results in Fig. 4(c). Therefore, a lower hole concentration near the source side can be expected in devices with larger FF structures, which results in decreased negative V_T shifts. This result suggests that the NBIS-induced negative V_T shift of a-IGZO TFTs can be lessened in larger FF structure devices.

In conclusion, the asymmetrical degradation of device electrical characteristics in a-IGZO TFTs after NBIS with V_D is attributed to positive-drain-bias-induced asymmetrical hole trapping. By using a-IGZO TFTs with an FF structure, the negative V_T shift of I_D-V_G after NBIS can be reduced when the μm/side is increased. Consequently, even though the I_D-V_G characteristics show no difference for devices with different FF structures, the instability of a-IGZO TFTs under NBIS can be suppressed by increasing the FF region of devices.

This work was performed at National Science Council Core Facilities Laboratory for Nano-Science and Nano-Technology in Kaohsiung-Pingtung area. The authors would like to acknowledge the financial support of the National Science Council of the Republic of China under Contract Nos. NSC 101-2120-M-110-002.

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