AIP Applied Physics Letters

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Citation: Applied Physics Letters **101**, 223505 (2012); doi: 10.1063/1.4768687
View online: http://dx.doi.org/10.1063/1.4768687
View Table of Contents: http://scitation.aip.org/content/aip/journal/apl/101/22?ver=pdfcov
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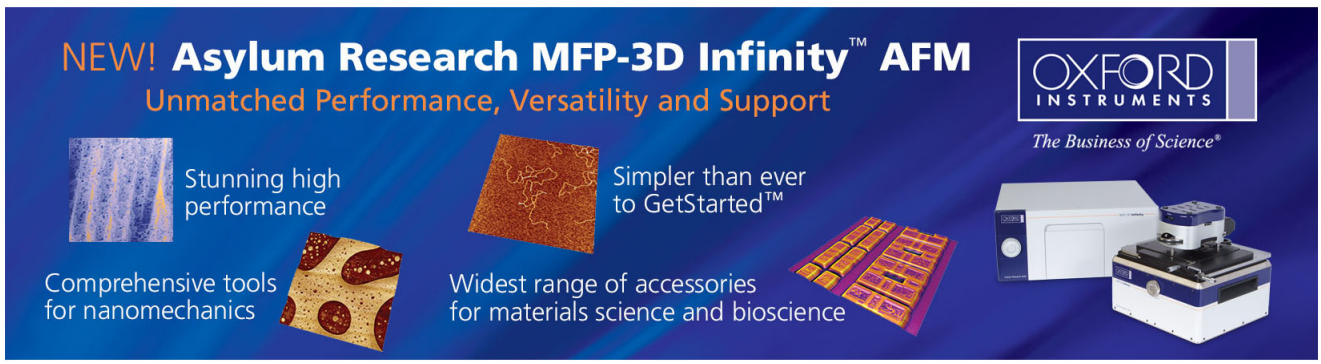

The mechanisms of random trap fluctuation in metal oxide semiconductor field effect transistors

E. R. Hsieh and Steve S. Chung[a)]
Department of Electronics Engineering and Institute of Electronics, National Chiao Tung University, Hsinchu, Taiwan

(Received 18 July 2012; accepted 8 November 2012; published online 27 November 2012)

An effect, called random trap fluctuation (RTF), is proposed to study the threshold voltage (V_{th}) fluctuation of metal oxide semiconductor field effect transistors (MOSFETs) under Fowler-Nordeim (FN) or hot carrier (HC) stress condition. Experiments have been demonstrated on n-channel MOSFETs, and it was found that not only the random dopant fluctuation (RDF) but also the stress-induced traps vary the V_{th} fluctuation. More importantly, the *stress-induced trap barrier* determines the V_{th} fluctuation. For devices after FN stress, V_{th} fluctuation is enhanced since the trap barrier regulates the transporting carriers. For devices after HC stress, V_{th} fluctuation is supressed since the carriers are backscattered into the channel by the trap barrier and fewer carriers with higher energy pass through the barrier. These results provide us a clear understanding on another source of V_{th} fluctuations in addition to the RDF as devices are further scaled. © *2012 American Institute of Physics*. [http://dx.doi.org/10.1063/1.4768687]

Moore's law has driven complementary metal-oxide semiconductor (CMOS) devices scaling for several decades.[1] The phenomenon of device fluctuations becomes increasingly important. One of the most significant issues in the scaling is the threshold voltage (V_{th}) fluctuation induced by the process or device structure;[1–11] especially the discrete-dopant in the channel induced random dopant fluctuation (RDF),[2] which is the major source of V_{th} fluctuation. It has been magnified by the scaling of device size (or area) because the electrical characteristics of the device become more and more sensitive to the number of dopants in the channel. Different configurations of dopant position will affect the value of the local V_{th} in the channel, and the electrical characteristics will not be uniform any more while the numbers of dopants are reduced to quite a few.[3] Recent studies have shown that the process-induced RDF, e.g., the non-uniform distribution of the generic dopants in the device channel, are required for the further scaling of device dimensions to drive the Moore's law. As a result, it has been a consensus to reduce the dopant concentrations in the device channel through the improvement of fabrication process, such as carbon co-implantation,[12] fully depleted silicon-on-insulator (FDSOI) or FinFET with undoped (lighter) channel,[13,14] which has been reported to reduce the V_{th} fluctuation effectively. On the other hand, as far as the reliabilities are concerned, for the devices after the stress, the bias-temperature instability (BTI) and random telegraph noise (RTN) may also raise the fluctuation of V_{th} with the evolution of time,[15–20] as a result of the dynamic exchange of carrier charges between the traps and channel.

Nevertheless, these transient responses of the electrical characteristics for the devices after the stress have never been examined in view of the variability, and the correlations between the reliability and variability have not been reported. In this paper, we present a concept that the stress-induced traps which caused the random trap fluctuation (RTF) can be considered as part of the fluctuations. Experimentally, for the device being stressed, the traps are generated in the oxide and at the interface with non-uniform distribution. It will affect the transport of carriers, giving rise to a similar fluctuation of the threshold voltage.[21,22] As a consequence, we are interested in understanding the mechanisms behind this additional source of V_{th} fluctuation. In this paper, the impact of RTF on the V_{th} fluctuation, caused by the Fowler-Nordheim(FN) or hot carrier (HC) stress, has been investigated.

By applying the Pelgrom plot,[23] i.e.,

$$\sigma V_{th,fresh} = A_{VT}/\sqrt{LW}, \tag{1}$$

where L and W are the device length and width, respectively, the dopant fluctuation before the stress can be interpreted and quantified by the standard deviation of $V_{th,fresh}$, e.g., $\sigma V_{th,fresh}$. The slope, A_{VT}, is an indicator of the $V_{th,fresh}$ fluctuation. For the device after the stress, the stressed V_{th} will be shifted, attributed to the trap generation. If traps are generated in the gate dielectric or the interface randomly after the stress, it is reasonable to treat this single trap as a delta function, i.e.,

$$\begin{aligned}\sigma V_{th,shift} &= q\sigma D_{trap}/C_{ox} \\ &= q\sqrt{\int_0^{Tox} \Delta N_{trap}(x)\delta(x - x_{trap})dx/(LW)}/C_{ox} \\ &\propto 1/\sqrt{LW},\end{aligned} \tag{2}$$

where $\sigma V_{th,shift}$ is the standard deviation of the threshold voltage shift after the stress. C_{ox} is the inversion capacitance; q is a constant value, 1.6×10^{-19} (coulomb); σD_{trap} is the standard deviation of trap densities; $\delta(x\text{-}x_{trap})$ is Dirac's delta-function, whose center is located at a trap position, x_{trap}, with value of unity or zero depending on the trap location. Now, the total variation of V_{th} after the stress, $\sigma V_{th,stress}$, can be considered as a root mean square of $\sigma V_{th,shift}$ and $\sigma V_{th,fresh}$, e.g.,

a)schung@cc.nctu.edu.tw.

$$\sigma V_{th,stress} = \sqrt{\sigma V^2{}_{th,fresh} + \sigma V^2{}_{th,shift}} \propto 1/\sqrt{LW}, \quad (3)$$

from which the actual $\sigma V_{th,stress}$ also holds the Pelgrom's inversion square rule as does for $\sigma V_{th,fresh}$ in Eq. (1). This can be judged from Fig. 1(b) in that the drain currents at the near threshold voltage region exhibit a parallel shift for the device after the stress.

It is well known that, after stresses, some charges trapped in defect states in the dielectric insulator of the gate exhibits a profound impact on the electric characteristics of nanoscale metal oxide semiconductor field effect transistors (MOSFETs).[24] These stress-induced traps will induce the electrostatic effect on the channel potential and will generate a localized barrier effectively, which will reflect the transporting carriers randomly. This trap-barrier leads to the V_{th} fluctuation,[25] and we call it RTF. Experimentally, to observe the influence of RDF on the V_{th} fluctuation, FN and HC stresses have been employed to generate different types of stress induced trap barriers. Fifty experimental samples, made by the state-of-the-art CMOS technology, are prepared for the experimental measurements. Equivalent oxide thickness (EOT) of these samples made by oxynitride (SiON) is 12 Å. Devices with various areas are measured to depict the Pelgrom plot. The threshold voltages of devices are determined by the $G_{m,max}$ method.

By collecting 50 sets of I_D-V_G curves measured at $V_{DS} = 50$ mV for fresh nMOS devices, the drain current population is shown in Fig. 1(a). In the enlarged insert of the figure, we can see the fluctuation of drain currents in response to the RDF effect, resulting in the V_{th} fluctuation before any stresses. In order to observe the stress-inudced V_{th} fluctuation, FN stress was carried out for those devices in Fig. 1(a). After the FN stress, traps were generated at Si/SiO_2 interface randomly. The FN stress then causes a fluctuation of the drain current such that the mismatch is significantly larger for stressed nMOS devices, compared to that of the fresh devices, as shown in Fig. 1(b). In general, the RTF will become increasingly significant since more traps will be generated as stress time evolutes.

In order to understand the physics of RTF, Fig. 2(a) shows the Pelgrom plot of these nMOSFETs after FN stress

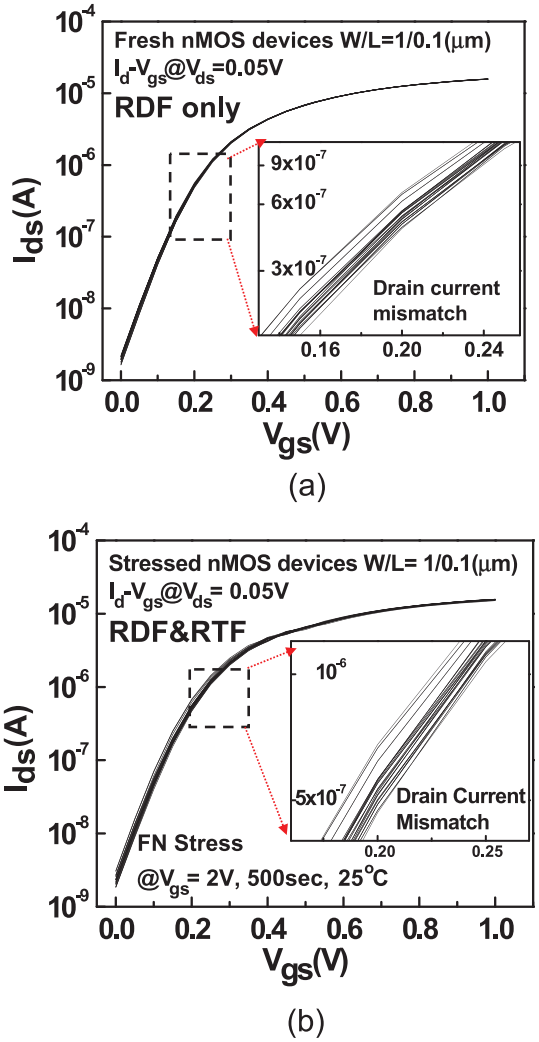

FIG. 1. (a) The measured drain current population on 50 sets of fresh n-MOSFETs with same dimensions and (b) the drain current population on 50 sets of n-MOSFETs with same dimensions after the FN-stress.

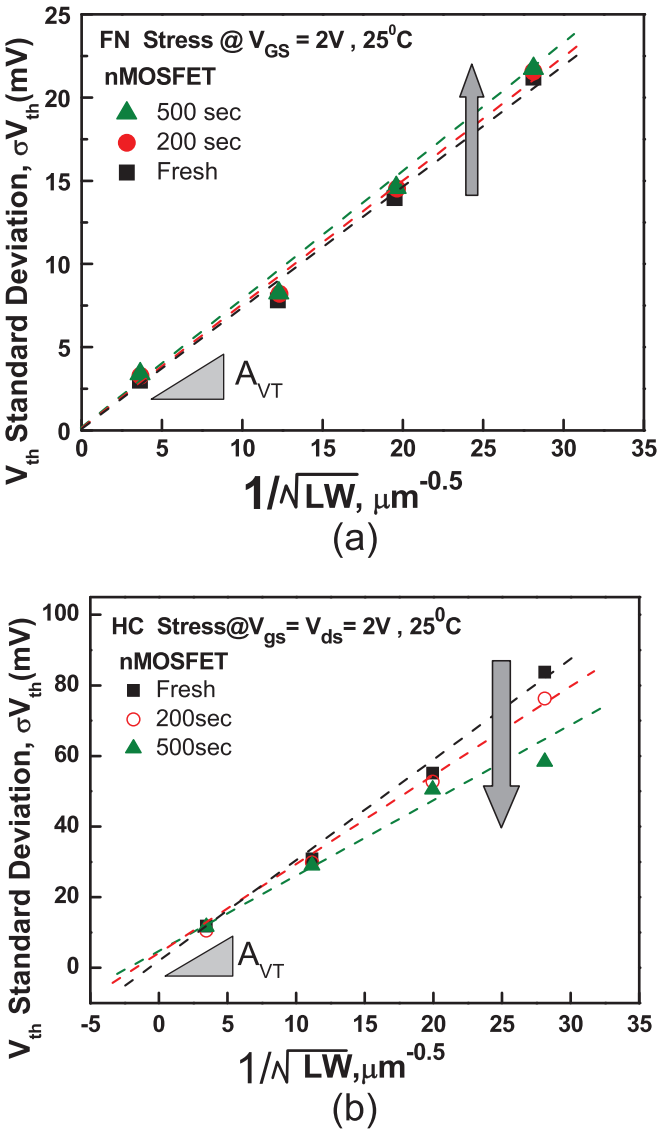

FIG. 2. The time evolution of the Pelgrom plot for n-MOSFETs (a) after FN stress and (b) after HC stress. The slope, A_{VT}, indicates the degrees of V_{th} fluctuation. The A_{VT} increases after the FN stress, but decreases after the HC stress. The device dimension from the left to right, W/L = 0.3/0.25, 0.2/0.13, 0.1/0.065, and 0.05/0.028 (μm/μm).

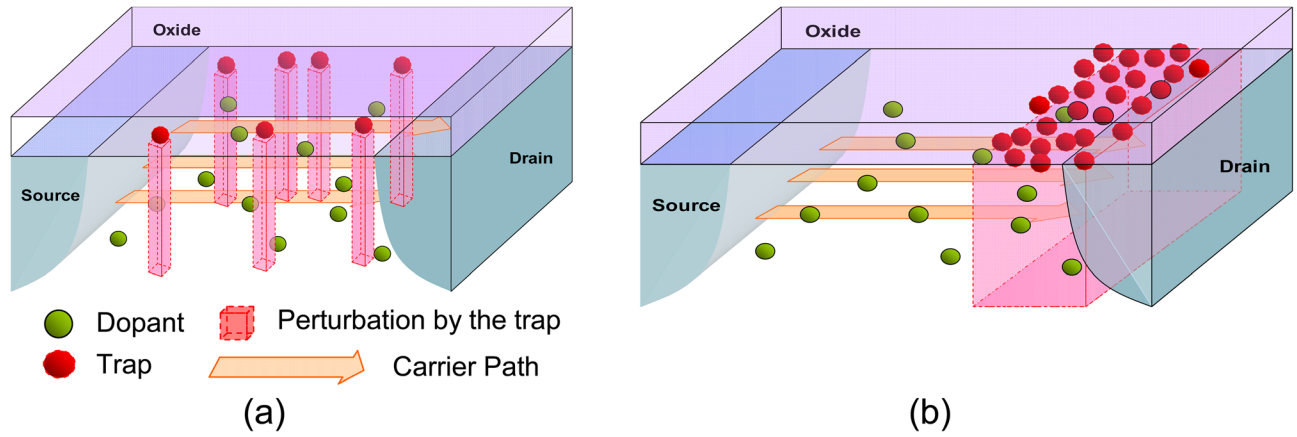

FIG. 3. The schematics to illustrate the dopant distribution, trap distribution, and the carrier transport path: (a) after the FN stress and (b) after the HC stress in n-MOSFETs.

with $V_{GS} = 2$ V for the fresh (0 s), 200 s and 500 s, respectively, showing the increase of the slope, A_{VT}, which is because during time evolution, random traps are increasingly generated such that the transporting carriers will go through more surface reflecting events from the interface of gate dielectric. On the other hand, we also applied HC stress to the devices with $V_{GS} = V_{DS} = 2$ V for the fresh (0 s), 200 s and 500 s, respectively. Surprisingly, it was observed an abnormal behavior as compared to that from the FN stress, i.e., instead the A_{VT} is decreased with increasing stress time after the HC stress, Fig. 2(b).

From the above two experimental observations, the evidence has been shown that the stress-induced V_{th} fluctuation will be dependent on the condition of electrical stress, i.e., FN or HC stress. The schematics in Fig. 3 illustrate the comparison of the generated traps between the two different

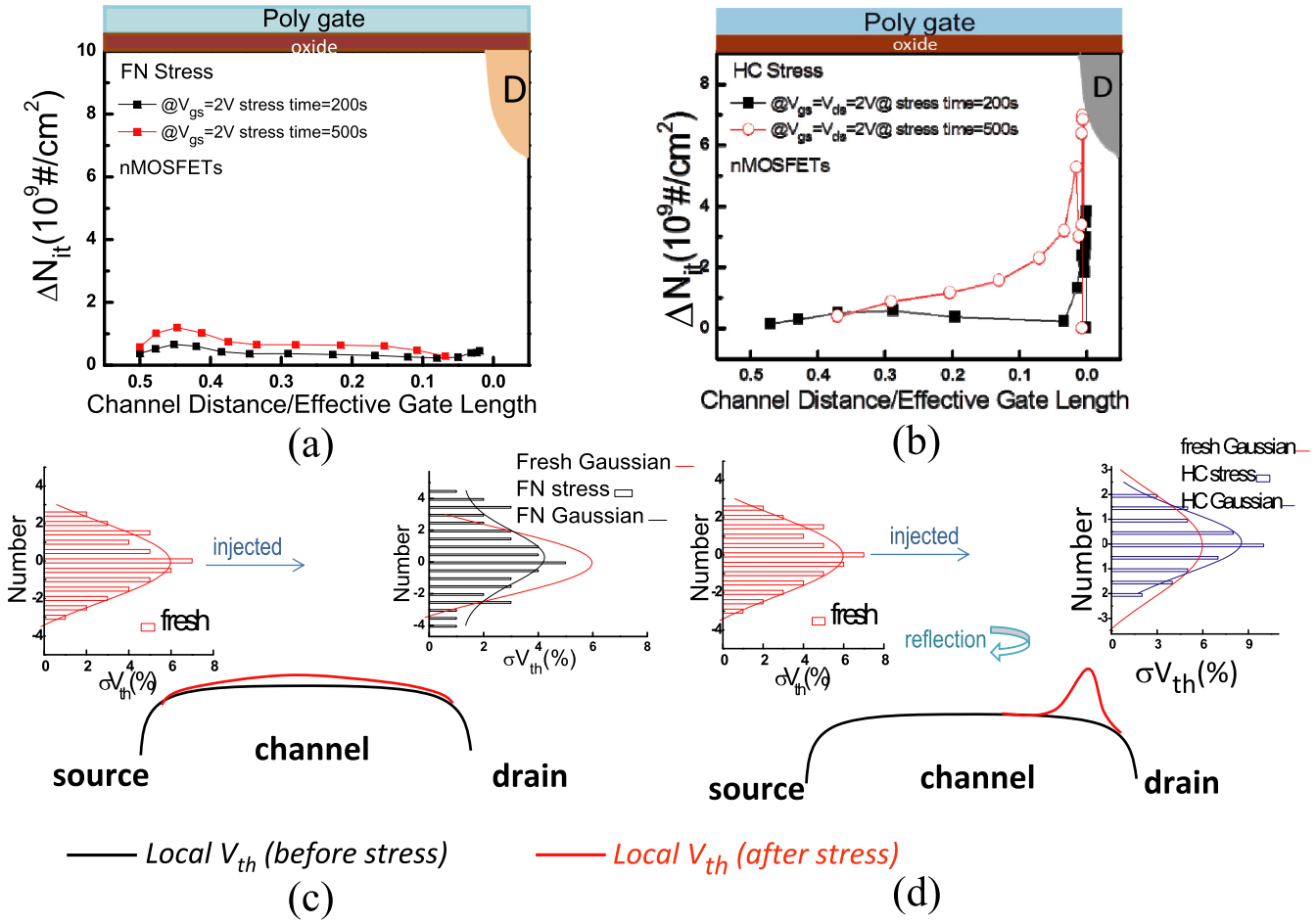

FIG. 4. The lateral profiling of interface traps, ΔN_{it}, (a) after the FN stress and (b) after the HC stress, by the charge pumping measurement. The schematic of the fluctuation induced by the trap barriers (c) after the FN stress and (d) after the HC stress. The perturbation of carriers by the trap barrier induces a much wider distribution of the carriers (solid black line) in (c), while the perturbation of carrier by the trap barrier in (d) results in a loss of the carrier bounced back to the channel, which gives rise to a narrower distribution of the carriers (solid blue line).

stress methods. In Fig. 3(a), under the FN stress, since the applying electrical field during the stress is uniform, it can be reasonably assumed that the generated traps in the channel potential are generated more evenly and sparsely on the gate dielectric, i.e., there is a random while sparse distribution of traps throughout the whole channel. These fluctuations of stress-induced trap-barriers cause the disturbance of the carrier transport such that the V_{th} of each transistor is raised as illustrated in Fig. 3(a), resulting in the random trap induced fluctuation. However, in Fig. 3(b), under the HC stress, since the high electrical field is located near the drain junction region, the generated traps are highly localized near the drain side. Compared to the random and sparse distribution of traps after the FN stress, traps caused by HC stress is confined only near the drain side and can be recognized as a trap barrier effectively. As carriers are traveling through this stress-induced trap barrier, those whose energies are within this barrier height will be reflected (backscattered), and only those whose energies are higher than the barrier height will reach the drain. In other words, the HC-stress induced trap barrier is an obstacle to reflect most of carriers, while just a small number of carriers can reach the drain side. As a result, the V_{th} fluctuation is supressed after the HC stress.

To verify the above experimental observation, the interface traps profiling techniques[26] by the charge pumping measurement has been utilized to characterize the distribution of traps generated after FN and HC stresses. Fig. 4(a) shows the generated distributions of the interface traps (ΔN_{it}) after the FN stress, in which the increment of N_{it} is more uniformly distributed along the channel except in the middle region of the channel, a little higher N_{it} was observed. In comparison, Fig. 4(b) shows the distributions of the interface traps (ΔN_{it}) after the HC stress, in which a huge number of traps were generated and highly localized in the near drain region. It has been reported that the scattering events will be affected by the generated traps after the stress.[27] In Figs. 4(c) and 4(d), the changes in σV_{th} distributions have been compared at the source and drain regions, respectively, from the experimental data of Fig. 2. In Fig. 4(c), the carriers travelling from the source with V_{th} distribution, in Gaussian shape (solid red line), are scattered by the FN-stress-induced traps and resulted in a broader distribution of σV_{th} (solid black line). In other words, after FN stress, σV_{th} becomes larger. In contrast, in Fig. 4(d), the carriers travelling from the source to the drain resulted in a narrower σV_{th} distribution. In other words, after the HC-stress, σV_{th} becomes smaller.

In conclusion, a RTF effect is proposed to study the mechanisms of the stressed induced fluctuations of MOSFETs. Different fluctuations are observed for the devices under different stress conditions. RTF effect increases the V_{th} fluctuations when the stress generated trap are uniform in the channel; while the V_{th} fluctuation is suppressed as a result of the trap barrier with highly nonuniform localized distribution near the drain. In other words, distributions of trap-barriers determine the V_{th} fluctuation. These results provide us an additional source of V_{th} fluctuation resulting from the interface traps caused by the FN or HC stress, i.e., $\sigma(V_{th})^2 = \sigma(\text{dopant})^2 + \sigma(N_{it})^2 + \sigma(\text{others})^2$. Furthermore, these results provide us a better understanding of the device reliability in terms of both the process and stress induced fluctuations.

The authors would like to thank the Central R&D, UMC, Taiwan for advanced wafer fabrication support and this work was supported by the National Science Council, Taiwan, under Contract NSC-99-2221-E009-192.

[1]G. Moore, Electronics **38**, 114 (1965).
[2]T. Mizuno, J. Okamura, and A. Toriumi, IEEE Trans. Electron Devices **41**, 2216 (1994).
[3]I. D. Mayergoyz and P. Andrei, J. Appl. Phys. **90**, 3019 (2001).
[4]T. Shinada, T. Kurosawa, H. Nakayama, Y. Zyu, M. Hori, and I. Ohdomari, Nanotechnology **19**, 345202 (2008).
[5]M. Hori, T. Shinada, K. Taira, N. Shimamoto, T. Tanii, T. Endo, and I. Ohdomari, Nanotechnology **20**, 365205 (2009).
[6]K. Inoue, F. Yano, A. Nishida, H. Takamizawa, T. Tsunomura, Y. Nagai, and M. Hasegawa, Appl. Phys. Lett. **95**, 043502 (2009).
[7]Y. Shimizu, H. Takamizawa, K. Inoue, T. Toyama, Y. Nagai, N. Okada, M. Kato, H. Uchida, F. Yano, T. Tsunomura, A. Nishida, and T. Mogami, Appl. Phys. Lett. **98**, 232101 (2011).
[8]M. Hori, T. Shinada, Y. Ono, A. Komatsubara, K. Kumagai, T. Tanii, T. Endoh, and I. Ohdomari, Appl. Phys. Lett. **99**, 062103 (2011).
[9]H. Takamizawa, Y. Shimizu, K. Inoue, T. Toyama, N. Okada, M. Kato, H. Uchida, F. Yano, A. Nishida, T. Mogami, and Y. Nagai, Appl. Phys. Lett. **99**, 133502 (2011).
[10]H. Takamizawa, Y. Shimizu, K. Inoue, T. Toyama, N. Okada, M. Kato, H. Uchida, F. Yano, A. Nishida, T. Mogami, and Y. Nagai, Appl. Phys. Lett. **100**, 253504 (2012).
[11]M. Hori, K. Taira, A. Komatsubara, K. Kumagai, Y. Ono, T. Tanii, T. Endoh, and T. Shinada, Appl. Phys. Lett. **101**, 013503 (2012).
[12]T. Tsunomura, A. Nishida, F. Yano, A. T. Putra, K. Takeuchi, S. Inaba, S. Kamohara, K. Terada, T. Mama, T. Hiramoto, and T. Mogami, VLSI Symp. Tech. Dig. **2009**, 110.
[13]K. J. Kuhn, Tech. Dig.—Int. Electron Devices Meet. **2007**, 471.
[14]O. Weber, O. Faynot, F. Andrieu, C. B. Dufournet, F. Allain, P. Scheiblin, J. Foucher, N. Daval, D. Lafond, L. Tosti, L. Brevard, O. Rozeau, C. F. Beranger, M. Marin, F. Boeuf, D. Delprat, K. Bourdelle, B. Y. Nguyen, and S. Deleonibus, Tech. Dig.—Int. Electron Devices Meet. **2008**, 245.
[15]B. Kaczer, T. Grasser, Ph. J. Roussel, J. Franco, R. Degraeve, L.-A. Rabnarsson, E. Simon, G. Groeseneken, and H. Reisinger, Proc.—Int. Reliability Physics Symposium **2010**, 26.
[16]M. Toledano-Luque, B. Kaczer, E. Simon, P. J. Roussel, A. Veloso, T. Grasser, and G. Groeseneken, Mocroelectron. Eng. **88**, 1243 (2011).
[17]M. Toledano-Luque, B. Kaczer, P. J. Roussel, T. Grasser, T. Y. Hoffmann, and G. Groeseneken, Tech. Dig. VLSI Symposium **2011**, 152.
[18]M. Houssa, M. Aoulaiche, S. De Gendt, G. Groeseneken, M. M. Heyns, and A. Stesmans, Appl. Phys. Lett. **86**, 093506 (2005).
[19]A. Ghetti, C. M. Compagnoni, A. S. Spinelli, and A. Visconti, IEEE Trans. Electron Devices **56**, 1746 (2009).
[20]T. Grasser, W. Goes, H. Reisinger, T. Aichinger, P. Hehenberger, P. J. Wagner, F. Schanovsky, J. Franco, M. T. Luque, and M. Nelhiebel, IEEE Trans. Electron Devices **58**, 3652 (2011).
[21]P. Andricciola, H. P. Tuinhout, B. De Vries, N. A. H. Wils, A. J. Scholten, and D. B. M. Klaassen, Tech. Dig.—Int. Electron Devices Meet. **2009**, 711.
[22]J. R. Brews, Appl. Phys. Lett. **43**, 2306 (1972).
[23]M. J. M. Pelgrom, IEEE J. Solid-State Circuit **24**, 1433 (1989).
[24]A. W. Krautschneider and S. Schwantes, Appl. Phys. Lett. **78**, 2790 (2001).
[25]A. Asenov, R. Balasubramaniam, A. R. Brown, J. H. Davies, and S. Saini, Tech. Dig.—Int. Electron Devices Meet. **2000**, 279.
[26]S. S. Chung, H. J. Feng, Y. S. Hsieh, A. Liu, W. M. Linz, D. E. Chen, J. H. Ho, K. T. Huang, C. K. Yang, O. Chenp, Y. C. Sheng, D. Y. Wu, W. T. Shiau, S. C. Chien, K. Liao, and S. W. Sun, Tech. Dig.—Int. Electron Devices Meet. **2004**, 477.
[27]E. R. Hsieh, S. S. Chung, P. W. Liu, W. T. Chiang, C. H. Tsai, W. Y. Teng, C. I. Li, T. F. Kuo, Y. R. Wang, C. L. Yang, C. T. Tsai, and G. H. Ma, Tech. Dig.—Int. Electron Devices Meet. **2009**, 780.