AIP Applied Physics Letters

Ohmic contact on n-type Ge using Yb-germanide

Zhi-Wei Zheng, Teng-Chieh Ku, Ming Liu, and Albert Chin

Citation: Applied Physics Letters **101**, 223501 (2012); doi: 10.1063/1.4768700
View online: http://dx.doi.org/10.1063/1.4768700
View Table of Contents: http://scitation.aip.org/content/aip/journal/apl/101/22?ver=pdfcov
Published by the AIP Publishing

Ohmic contact on n-type Ge using Yb-germanide

Zhi-Wei Zheng,[1] Teng-Chieh Ku,[2] Ming Liu,[1] and Albert Chin[2,a)]
[1]*Institute of Microelectronics, Chinese Academy of Sciences, Beijing 100029, China*
[2]*Department of Electronics Engineering, National Chiao Tung University, Hsinchu 300, Taiwan*

(Received 24 August 2012; accepted 8 November 2012; published online 26 November 2012)

Poor ohmic contact by Fermi-level pinning to valence band (E_V) edge is one of the major challenges for germanium (Ge) n-type metal–oxide–semiconductor field-effect transistor (nMOSFET). Using low work-function rare-earth ytterbium (Yb), good ohmic contact on n-type Ge with alleviated Fermi-level pinning was demonstrated. Such ohmic behavior depends strongly on the germanide formation condition, where much degraded ohmic contact at 600 °C rapid thermal annealing is due to the lower Yb/Ge composition found by energy-dispersive x-ray spectroscopy. The ohmic behavior of Yb-germanide/n-type-Ge has high potential for future high-performance Ge nMOSFET application. © *2012 American Institute of Physics*.
[http://dx.doi.org/10.1063/1.4768700]

Low power operation is the most important criterion for integrated circuit (IC). To reach this goal, high mobility channel materials will be required for complementary metal–oxide–semiconductor field-effect transistors (CMOSFETs)—the key element for IC. Germanium (Ge) is a promising candidate among various high mobility channel materials, due to both higher electron and hole mobility than silicon (Si), simpler process, lower cost, and potentially higher yield for next-generation low-power CMOS.[1–11] High performance Ge n- and p-type MOSFETs (nMOS and pMOS) with higher channel mobility than the universal mobility of SiO_2/Si MOSFET have been demonstrated at small equivalent-oxide-thickness (EOT).[4,11] Besides, the integration of defect-dislocation free Ge CMOS on Si has been realized by Ge-on-Insulator (GOI or GeOI) technology,[1] where the DC power consumption by the leakage current of small energy bandgap (E_G) Ge MOSFET can be largely improved by thinning down the body thickness of GOI.[5]

However, one major obstacle for Ge CMOS, to replace the Si counterpart, is the Fermi level pinning to valence band (E_V) edge that leads to poor contact for Ge nMOS.[12–17] This becomes more severe at highly scaled sub-14 nm nMOS with smaller contact area.[1] To address this issue, surface passivation using thin dielectric has been reported to decrease the Fermi level pinning.[13–17] Nevertheless, the extra tunneling resistance is the basic physical limitation that degrades the important transistor drive current. In this paper, we report a simple method to achieve less Fermi level pinning on n-type Ge (n-Ge). The Fermi level pinning depends strongly on the germanide formation condition. Ohmic behavior on low doped n-Ge contact was reached using low work-function ytterbium (Yb) and Yb-germanide with high Yb/Ge composition from energy-dispersive x-ray spectroscopy (EDS). Such good metal/semiconductor contact using germanide is similar to silicide contact for Si CMOS, with irreplaceable merits of low contact resistance and simple self-aligned process for device application.

Standard n-type Ge wafers for CMOS with resistivity of 1–5 Ω-cm ($1.5 \times 10^{15} \sim 5 \times 10^{14}\,cm^{-3}$) were used. After cleaning, the samples were immersed into diluted hydrofluoric acid (HF) solution to remove the native oxide, dipped in de-ionized (DI) water, dried with N_2, and immediately loaded into vacuum chamber. Then the 60 nm thick Yb, nickel (Ni), or platinum (Pt) was deposited using e-beam evaporation through a metal mask. An extra SiO_2 was also deposited on Yb to prevent oxidation once exposure to air. Then a rapid thermal annealing (RTA) was applied to improve the metal/n-Ge contact at 400 ~ 600 °C for 30 s. The covered SiO_2 on Yb/n-Ge was subsequently removed by a HF dip. The fabricated contacts were investigated by current-voltage, transmission electron microscopy (TEM) and EDS measurements.

Figure 1 shows the current density-voltage (*J-V*) characteristics of NiGe[12] and Pt on n-Ge contacts under different RTA temperatures. A low temperature of 300 °C was used for Pt contact to lower interface reaction; the NiGe temperature is also lower then that of NiGe Schottky barrier source-drain MOSFET.[12] However, rectifying Schottky diode characteristics were observed for these contacts on n-Ge wafers, which failed for ohmic contact application of Ge nMOSFET. The Schottky barrier height (Φ_b) and ideality

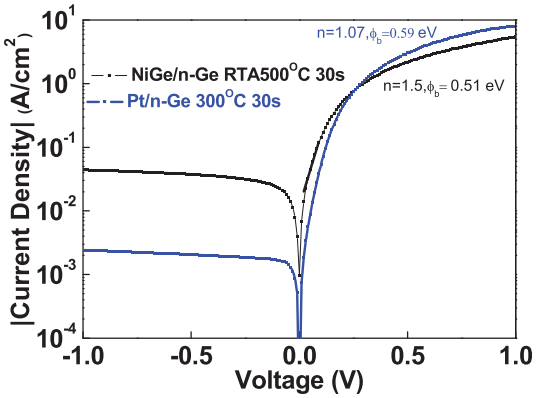

FIG. 1. *J-V* characteristics of NiGe and Pt contact on n-Ge wafer. The Schottky diode characteristics are suitable for Ge pMOS, but not for Ge nMOS.

a)Author to whom correspondence should be addressed. E-mail: albert_achin@hotmail.com. Tel.: 886-3-5731841.

factor (n) can be extracted from the J-V curves under forward bias ($V > 3kT/q$), according to the thermionic emission theory:[12]

$$J = A^*T^2\exp(-q\Phi_b/kT)\exp(qV/nkT), \quad (1)$$

where A^*, k, T, q, Φ_b, and n are the effective Richardson constant, Boltzmann constant, temperature, electron charge, effective Schottky barrier height, and ideality factor, respectively. The Φ_b of NiGe/n-Ge contact at 500 °C RTA and Pt/n-Ge contact at 300 °C RTA are 0.51 eV and 0.59 eV, with corresponding ideality factors of 1.5 and 1.07, respectively. The large Φ_b values further lead to small 0.16 and 0.08 eV energy difference to Ge E_V edge. The higher Φ_b of Pt/n-Ge contact is further evident from the much smaller reverse leakage current. However, the Φ_b difference of 0.08 eV is lower than the metal work-function (Φ_m) difference between Ni (5.0 eV) and Pt (5.3 eV). Therefore, the small Φ_b difference and large Φ_b values indicate the Fermi level pinning to E_V.

Figure 2 shows the J-V characteristics of Yb/n-Ge contacts at different RTA temperatures. Poor contact characteristics were found in Yb/n-Ge at 600 °C RTA that is consistent with previous report.[12] In sharp contrast to the rectifying diode behavior of NiGe/n-Ge and Pt/n-Ge contacts, the J-V characteristics of Yb/n-Ge contact at 500 °C RTA exhibit an ohmic behavior. Besides, a relatively low resistivity of 24 $\mu\Omega-$cm is obtained, although it is relatively higher than the typical 14 $\mu\Omega-$cm resistivity of NiSi. Such ohmic behavior is related to the low Φ_m of Yb (2.6 eV), suggesting the alleviated Fermi level pinning. It is important to notice that the ohmic contact on low doped Ge is significantly difficult compared with highly doped Ge;[18,19] however, this is necessary for Schottky barrier source/drain MOSFET.[20,21] The good ohmic contact on n-Ge is vitally important for Ge nMOS for sub-14 nm CMOS technology with small contact area.

To further investigate the ohmic behavior and alleviated Fermi level pinning at the lower RTA temperature, we have analyzed the Yb/n-Ge contact by cross-sectional TEM and EDS. Figure 3 shows the TEM image of Yb/n-Ge contact at 600 °C RTA, where $YbGe_x$ germanide, smooth Yb/n-Ge interface, and free from junction spiking were formed on n-Ge. However, these observations cannot explain the strong RTA-temperature dependence on contact characteristics.

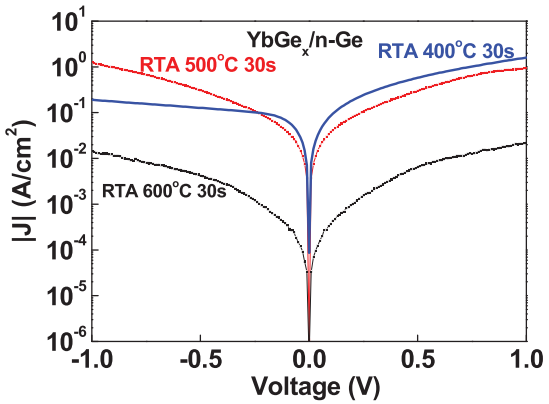

FIG. 2. J-V characteristics of $YbGe_x$ contact on n-Ge wafer at different RTA temperatures. The ohmic behavior is useful for Ge nMOS.

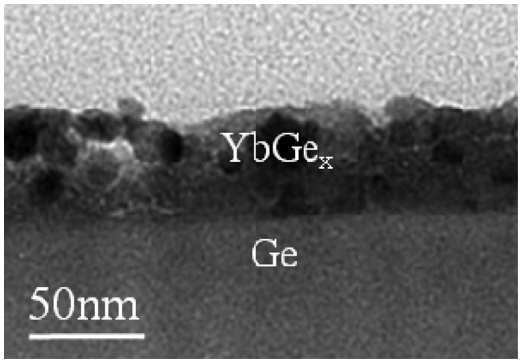

FIG. 3. Cross-sectional TEM image of $YbGe_x$ on n-Ge wafer after 600 °C RTA, with smooth interface and without contact metal spiking.

Figure 4 shows the EDS profile for $YbGe_x$/n-Ge formed at 500 °C and 600 °C RTA (The copper peaks are due to the copper net carrier). The Yb/Ge atomic ratios for the Yb/n-Ge contact at 500 °C RTA are larger than that at 600 °C RTA. This explains the better ohmic contact behavior for 500 °C RTA sample, where the higher Yb contact lowers the Φ_m that in turn decreases the Φ_b for ohmic contact. The possible reason for the lower Yb/Ge at 600 °C RTA may be due to the stronger Ge reaction and Ge diffusion[10] at higher temperature that leads to more dangling bonds formation. Such charged dangling bonds are linked to the strong Fermi-level pinning in Ge nMOS devices, where the pinning to E_V also causes poor ohmic contact to n-Ge.

In conclusion, good ohmic contact with alleviated Fermi level pinning on low doped n-Ge contact was demonstrated without insertion of an interfacial layer or surface passivation. The $YbGe_x$/n-Ge contact shows ohmic behavior, which depends strongly on the germanide formation condition. This $YbGe_x$/n-Ge ohmic contact shows high potential for future Ge nMOS application, where low contact resistance is required for sub-14 nm CMOS technology.

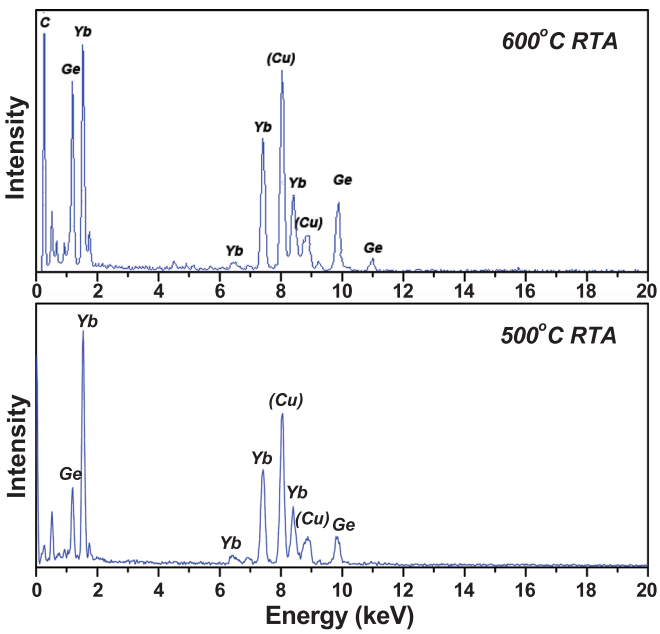

FIG. 4. EDS profile for $YbGe_x$/n-Ge contacts formed at 500 °C and 600 °C RTA.

[1]C. H. Huang, M. Y. Yang, A. Chin, W. J. Chen, C. X. Zhu, B. J. Cho, M.-F. Li, and D. L. Kwong, Symposium on VLSI Technology Digest (IEEE, New York, 2003), p. 119.
[2]K. Kita, K. Kyuno, and A. Toriumi, Appl. Phys. Lett. **85**, 52 (2004).
[3]T. Maeda, T. Yasuda, M. Nishizawa, N. Miyata, Y. Morita, and S. Takagi, Appl. Phys. Lett. **85**, 3181 (2004).
[4]D. S. Yu, A. Chin, C. C. Laio, C. F. Lee, C. F. Cheng, W. J. Chen, C. Zhu, M.-F. Li, S. P. McAlister, and D. L. Kwong, Tech. Dig. - Int. Electron Devices Meet. **2004**, 181.
[5]A. Chin, H. L. Kao, Y. Y. Tseng, D. S. Yu, C. C. Chen, S. P. McAlister, and C. C. Chi, Tech. Dig. – Eur. Solid State Device Res. Conf. **2005**, 285.
[6]V. V. Afanas'ev, Y. G. Fedorenko, and A. Stesmans, Appl. Phys. Lett. **87**, 032107 (2005).
[7]Q. Zhang, J. Huang, N. Wu, G. Chen, M. H. Hong, L. K. Bera, and C. X. Zhu, IEEE Electron Device Lett. **27**, 728 (2006).
[8]D. Kuzum, A. J. Pethe, T. Krishnamohan, Y. Oshima, Y. Sun, J. P. McVittie, P. A. Pianetta, P. C. McIntyre, and K. C. Saraswat, Tech. Dig. - Int. Electron Devices Meet. **2007**, 723.
[9]G. Mavrou, P. Tsipas, A. Sotiropoulos, S. Galata, Y. Panayiotatos, A. Dimoulas, C. Marchior, and J. Fompeyrine, Appl. Phys. Lett. **93**, 212904 (2008).
[10]W. B. Chen and A. Chin, Appl. Phys. Lett. **95**, 212105 (2009).
[11]W. B. Chen, B. S. Shie, C. H. Cheng, K. C. Hsu, C. C. Chi, and A. Chin, Tech. Dig. - Int. Electron Devices Meet. **2010**, 420.
[12]S. Zhu, R. Li, S. J. Lee, M. F. Li, A. Du, J. Singh, C. Zhu, A. Chin, and D. L. Kwong, IEEE Electron Device Lett. **26**, 81 (2005).
[13]A. Dimoulas, P. Tsipas, A. Sotiropoulos, and E. K. Evangelou, Appl. Phys. Lett. **89**, 252110 (2006).
[14]T. Nishimura, K. Kita, and A. Toriumi, Appl. Phys. Express **1**, 051406 (2008).
[15]Y. Zhou, M. Ogawa, X. Han, and K. L. Wang, Appl. Phys. Lett. **93**, 202105 (2008).
[16]M. Kobayashi, A. Kinoshita, K. Saraswat, H.-S. Philip Wong, and Y. Nishi, Dig. Tech. Pap. - Symp. VLSI Technol. 2008, 54.
[17]R. R. Lieten, S. Degroote, M. Kuijk, and G. Borghs, Appl. Phys. Lett. **92**, 022106 (2008).
[18]A. Firrincieli, K. Martens, R. Rooyackers, B. Vincent, E. Rosseel, E. Simoen, J. Geypen, H. Bender, C. Claeys, and J. A. Kittl, Appl. Phys. Lett. **99**, 242104 (2011).
[19]K. Gallacher, P. Velha, D. J. Paul, I. MacLaren, M. Myronov, and D. R. Leadley, Appl. Phys. Lett. **100**, 022113 (2012).
[20]S. Zhu, J. Chen, M.-F. Li, S. J. Lee, J. Singh, C. X. Zhu, A. Du, C. H. Tung, A. Chin, and D. L. Kwong, IEEE Electron Device Lett. **25**, 565 (2004).
[21]S. Zhu, H. Y. Yu, S. J. Whang, J. H. Chen, C. Shen, C. Zhu, S. J. Lee, M. F. Li, D. S. H. Chan, W. J. Yoo, A. Du, C. H. Tung, J. Singh, A. Chin, and D. L. Kwong, IEEE Electron Device Lett. **25**, 268 (2004).