Demonstration and Electrical Performance Investigation of Wafer-Level Cu Oxide Hybrid Bonding Schemes

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***Abstract*—Wafer-level Cu oxide hybrid bonding owns a number of merits, including simultaneous formations of electrical and mechanical bonds, underfill free, high alignment accuracy, increasing bond strength, and excellent reliability performance in 3-D integration. This letter demonstrates the fabrication of wafer-level Cu oxide hybrid bonding. Investigations of experimental and electrical simulation data of Cu oxide hybrid bonding structures are reported. Their alignment accuracy, frequency responses, and passive elements are compared for 3-D integration applications.**

***Index Terms*—Hybrid wafer bonding, wafer level, 3-D integration.**

I. Introduction

THREE-DIMENSIONAL integration is widely considered as an enabling technology to extend the lifetime of "Moore's law" [1]–[3]. Aligned wafer bonding is the key procedure to realize 3-D integration. Several bonding approaches, including metal bonding and hybrid bonding, are candidates to stack device layers vertically [3]–[5], [8]–[10]. The selection of 3-D bonding approaches depends on equipment availability, material properties, processing environment, product applications, etc. As ready in foundry and assembly houses, metal bonding is used predominantly [3]–[5]. The mechanism of thermocompression metal bonding is an interdiffusion reaction between two metals, while the drawback of open air gap may result in reliability concerns [6], [7]. Hybrid bonding (i.e., using both metal and dielectric or adhesive) is an interesting option for 3-D integration as it creates simultaneously direct electrical and mechanical connections between strata and requires no underfill [8]–[11].

This letter reports wafer-level Cu oxide hybrid bonding. Two alignment-bond structures, namely, "lock-n-key" and "oxide-recessed" structures, are designed and fabricated, with corresponding evaluations of their processing benefits and electrical performances. Both bonding schemes can be used in different 3-D integration schemes, including face-to-face and face-to-back schemes, with and without through-silicon vias (TSVs).

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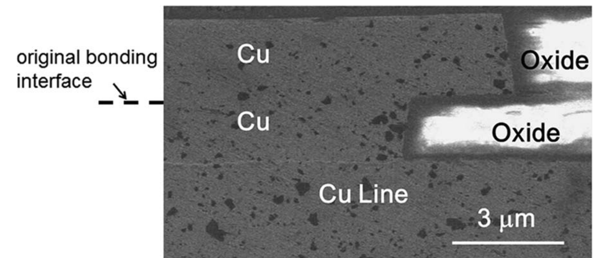

Fig. 1. SEM image of Cu oxide hybrid bonding structure. Cu–Cu and oxide–oxide were bonded simultaneously. The original Cu bonding interface becomes invisible in this structure.

II. Bond Structures and Performances

A. Cu Oxide Hybrid Bonding

Fig. 1 shows a cross-sectional SEM image of a successful Cu oxide hybrid bonding structure in a 200-mm wafer-level scheme. After a standard CMOS damascene processing, two 200-mm wafers were aligned and bonded face to face. Since damascene Cu was surrounded by oxide, two bonding processes, namely, Cu–Cu bonding and oxide–oxide bonding, were performed simultaneously. The bonding process was accomplished at 400 °C for 30 min in an EV Group bonder.

As shown in Fig. 1, Cu oxide structures from two wafers are bonded together. The original Cu–Cu bonding interface becomes invisible, indicating a well-bonded Cu structure. This bond structure can survive after following 3-D IC fabrication, including wafer thinning, TSV, and backside process.

B. Physical Configurations and Alignment Results

Fig. 2(a) and (b) shows the schematics of the "lock-n-key" and "oxide-recessed" alignment-bond structures for wafer alignment and bonding, respectively. The "oxide-recessed" structures are popularly used in the existing 3-D integration approaches. For a set of test vehicles, top Cu pad ($area = 20 \times 20\ \mu\text{m}^2$; $thickness = 1\ \mu$m) and bottom Cu pad ($area = 10 \times 10\ \mu\text{m}^2$; $thickness = 1\ \mu$m) are vertically bonded to each other, building the electrical and mechanical connects simultaneously. In the "lock-n-key" structure, the misalignment is confined by a design tolerance Δ, while the "oxide-recessed" one might shift by a value larger than Δ

$$\Delta = \frac{1}{2}(Top\ Pad\ Dimension - Bottom\ Pad\ Dimension). \quad (1)$$

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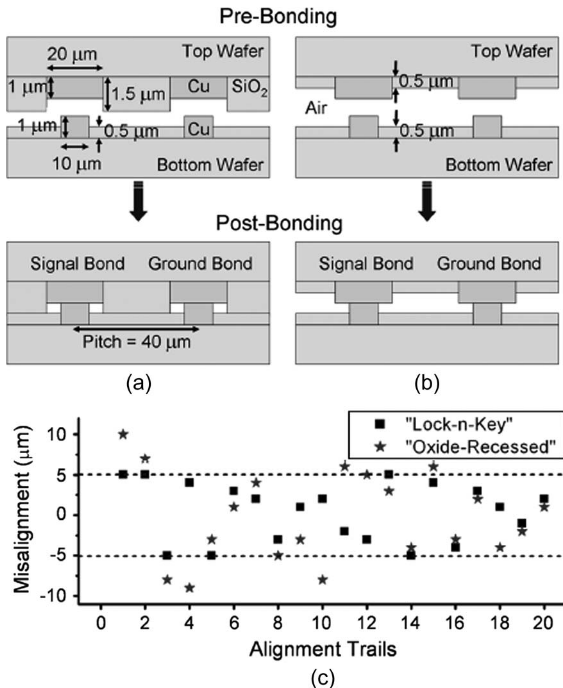

Fig. 2. Schematics of two different bonding structures (top Cu pads—$area = 20 \times 20\ \mu m^2$ and $thickness = 1\ \mu m$; bottom Cu pads—$area = 10 \times 10\ \mu m^2$ and $thickness = 1\ \mu m$). (a) "Lock-n-key" and (b) "oxide-recessed" structures. (c) Statistics of 20 alignment trials for the "lock-n-key" and "oxide-recessed" structures.

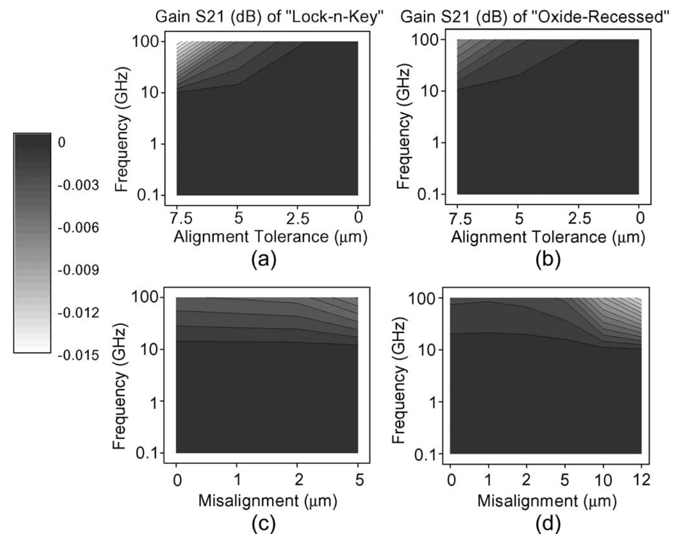

Fig. 3. Contours of signal gain S21 (in decibels) versus frequency and alignment tolerance for (a) "lock-n-key" and (b) "oxide-recessed" structures. S21 drops with the increasing frequency and alignment tolerance. Although the gain of the "lock-n-key" structure is smaller than that of "oxide-recessed" one, the overall signal loss is ignorable. Contours of signal gain S21 (in decibels) versus frequency and misalignment for (c) "lock-n-key" and (d) "oxide-recessed" structures. S21 drops with the increasing frequency and misalignment. The "lock-n-key" structure helps prevent a big signal loss when misalignment is out of design tolerance.

During bonding, the Cu and oxide surfaces of "lock-n-key" structures can be simultaneously bonded to each other, actually performing Cu oxide hybrid bonding. On the other hand, the "oxide-recessed" structure performs the conventional metal bonding with air gaps between wafers. With the same Cu bond sizes, the "lock-n-key" structure (SiO_2 thermal conductivity; 1.4 W/m · k) has better heat dissipation than the "oxide-recessed" one (air thermal conductivity; 0.025 W/m · k). Since both schemes can achieve good bond results, the impacts on transition delay should be small.

For comparison purposes, a pair of identical signal and ground bonds is used in both the "lock-n-key" and "oxide-recessed" structures, where the ground bond serves as the returning current path. The pitch of the signal and ground bonds is 40 μm.

Fig. 2(c) shows the alignment results of 20 successful trials on "oxide-recessed" and "lock-n-key" structures. First, several trials have high misalignment values caused by initial pattern recognition steps of an alignment tool. As the results shown in Fig. 2(c), the "lock-n-key" structure shows a better alignment accuracy, which is always within the design tolerance window ($\pm 5\ \mu$m), than that of the "oxide-recessed" one.

C. Design of Alignment Tolerances

Ansoft's HFSS and Q3D are used as the electromagnetic solvers. The electrical performances of the "lock-n-key" and "oxide-recessed" alignment-bond structures under high-speed operation between the top wafer and the bottom wafer are studied. By fixing the top pad dimensions ($20 \times 20\ \mu m^2$; $thickness = 1\ \mu$m) and changing the bottom pad size (5×5, 10×10, 15×15, and $20 \times 20\ \mu m^2$), different alignment tolerances ($\Delta = 7.5$, 5, 2.5, and 0 μm) are possible according to (1). Frequency responses up to 100 GHz are plotted in Fig. 3(a) and (b), where a tradeoff between signal gain S21 and alignment tolerance is observed. Signal is attenuated with increasing frequency, and small bottom pads allowing large alignment tolerances also decrease the signal gain. In the fixed alignment tolerance (i.e., in the range of 0–7.5 μm), a larger signal loss is possible for the "lock-n-key" configuration than the "oxide-recessed" one because of the air gaps, i.e., less dielectrics in-between for in the "oxide-recessed" structure. However, the values of magnitude are almost unchanged when signals are traveling along two bond structures because the bonds are fat and short in size.

Fig. 4(a) shows the dc and ac (100 GHz) parasitics (resistance, inductance, and capacitance) extracted by Ansoft's Q3D. As the frequency increases, the resistance goes up because of the skin effect, inductance decreases due to the disappearance of the conductor inner magnetic flux, and capacitance remains constant. In most cases, the parasitics of the "oxide-recessed" structure are slightly smaller, resulting in better behavior, which is consistent with the results in Fig. 3 from Ansoft's HFSS. This difference between the two structures is again due to the larger air gaps in the "oxide-recessed" structure. As shown in Fig. 4(a), the capacitance in the "lock-n-key" structure is larger because the signal and ground bonding pads are almost surrounded by the SiO_2 layer ($\varepsilon_r = 4$), whereas a larger portion of air gaps ($\varepsilon_r = 1$) exists in the "oxide-recessed" structure, leading to a reduced capacitance. However, again, we cannot tell the difference of the overall performances between these two bond structures as their passive elements are very small.

D. Bond Misalignments

Using the 5-μm alignment tolerance [Fig. 2(c)], the impact of the offset between the top and bottom pads on the electrical

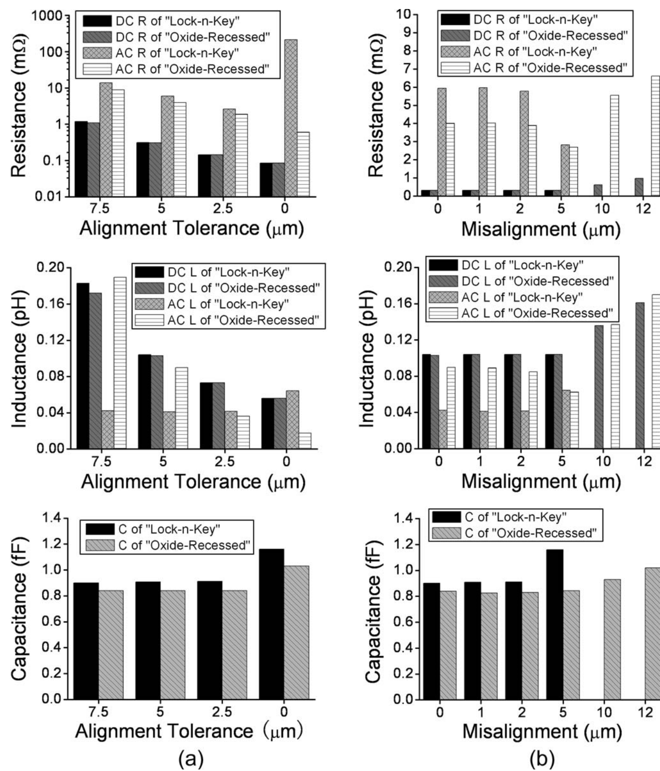

Fig. 4. DC and ac (100 GHz) parasitics extracted for the "lock-n-key" and "oxide-recessed" structures with (a) different design alignment tolerances and (b) different misalignments.

performance is studied. During alignment and bonding steps in 3-D integration, some undesired misalignments are inevitably introduced by processing variations (e.g., mechanical shifts and temperature gradients). Unlike in the "oxide-recessed" structure, the maximum misalignment cannot exceed the design tolerance in the "lock-n-key" structure.

Considering the single side displacement, in Fig. 3(c) and (d), S21 drops apparently from 10 to 100 GHz in the "oxide-recessed" structure, when the misalignment is out of the design tolerance. The "lock-n-key" structure effectively prevents this larger misalignment and ensures high-yield electrical interconnections, although as discussed hereinafter, its performance is a little worse than that of the "oxide-recessed" one when the pad misalignments are within the tolerance.

As can been seen in Fig. 4(b), all the parasitics are compared in both the "lock-n-key" and "oxide-recessed" structures with different misalignments. When misalignments are larger than 5 μm, the resistance and inductance of the "oxide-recessed" structure increase a lot. In the worst case, no electrical contact (i.e., infinite resistance) is formed between a pair of bond pads in the "oxide-recessed" structure for too large misalignment. However, if the misalignment can be always kept within the tolerance by the better tool/process control or low-temperature bonding, the "lock-n-key" structure does not provide the advantages compared to the "oxide-recessed" one.

This letter presents the electrical performances of bond elements. The TSV performance has to be taken into consideration as well for a whole 3-D interconnect analysis. For example, since the depth of TSV is usually larger than the thickness of bond pad and TSV sits inside a more lossy Si substrate, the TSV parasitics can have larger effect on the 3-D system performance.

III. Conclusion

Wafer-level Cu oxide hybrid bonding technology has been successfully demonstrated. The electrical performance simulation and alignment investigation of two wafer-level alignment-bonding schemes have been reported. These results help designers decide the alignment-bonding scheme, size of pad, and, hence, alignment tolerance in early stage. The Cu oxide hybrid bonding with "lock-n-key" structures shows excellent alignment accuracy and electrical performance. Misalignments can be confined within the design alignment tolerances by the "lock-n-key" bond, preventing a big signal loss when misalignment is out of design tolerance. The simulated signal losses and parasitics of both structures are small, which become poor with increasing frequency, relaxed design tolerance, and increasing misalignment.

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