Wafer-to-Wafer Alignment for Three-Dimensional Integration: A Review

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***Abstract*—This paper presents a review of the wafer-to-wafer alignment used for 3-D integration. This technology is an important manufacturing technique for advanced microelectronics and microelectromechanical systems, including 3-D integrated circuits, advanced wafer-level packaging, and microfluidics. Commercially available alignment tools provide prebonding wafer-to-wafer misalignment tolerances on the order of 0.25 μm. However, better alignment accuracy is required for increasing demands for higher density of through-strata vias and bonded interstrata vias, whereas issues with wafer-level alignment uniformity and reliability still remain. Three-dimensional processes also affect the alignment accuracy, although the misalignment could be reduced to certain extent by process control. This paper provides a comprehensive review of current research activities over wafer-to-wafer alignment, including alignment methods, accuracy requirements, and possible misalignments and fundamental issues. Current misalignment concerns of the major bonding approaches are discussed with detailed alignment results. The fundamental issues associated with wafer alignment are addressed, such as alignment mechanisms, uniformity, reproducibility, thermal mismatch, and materials. Alternative alignment approaches are discussed, and perspectives for wafer-to-wafer alignment are given. [2010-0363]**

***Index Terms*—Alignment, 3-D integration, wafer bonding, wafer-level packaging.**

I. Introduction

THERE IS a greatly increased demand for ever high-performance high-functionality integration driven by computation, mobile, and game industries [1]–[8]. Historically, it has been satisfied by downscaling transistors following Moore's law. However, the interconnect RC delay has become a major source of circuit delays as the size of transistors gets reduced with ever increasing integration scale. Three-dimensional integration has been introduced, developed, and recognized as one of the solutions in the International Technology Roadmap for Semiconductors in reducing the length of interconnects and, furthermore, in satisfying the demand of highly integrated electronic systems [1]–[24]. Whereas conventional integration connects circuits horizontally with long interconnection wires on one substrate, 3-D integration provides a new paradigm to vertically integrate various building blocks. Not only can 3-D integration shorten wires with smaller chip sizes, but also it is a new technology platform for heterogeneous integration by stacking and connecting dissimilar materials or different modules on one substrate.

Three-dimensional integration has emerged as a promising solution in driving the next generation of CMOS integration technology [1]–[20] and microelectromechanical systems (MEMS) [21]–[23]. The major processing of 3-D integration is composed of four basic unit processes: alignment, bonding, thinning, and interstrata interconnection [1]–[4]. These processes are under intensive development. For alignment, higher reliable alignment accuracy is required for higher density of through-strata vias (TSVs) and bonded interstrata vias (BISVs). For bonding, robust bonding interface and thermal management are quite challenging. For thinning, uniformity is a critical issue, whereas handling thinned wafers is difficult for some 3-D integration schemes. For interstrata interconnection, TSV technology has already been used for certain applications such as CMOS imagers, and various TSV technologies are being developed [14], [16], [19], [21], [23].

There are several 3-D technology platforms proposed [1]–[4], [10], [18], [24]–[28]. Fig. 1 schematically shows two 3-D platforms, i.e., via-first [28] and via-last [24]–[27]. They are classified by the sequence order of interstrata interconnection formation and wafer bonding. When wafer bonding is ahead of interstrata interconnection formation using TSVs, it is called "via-last." After two fully processed wafers are bonded, TSVs are formed to connect the top and bottom circuits. For the via-first 3-D process platform, a redistributed layer is formed on top of the fully processed device wafer. The redistribution layers are bonded directly face-to-face using BISVs. Depending on their applications, these platforms may use different materials, for example, for TSV formation, planarization on redistribution layer, alignment, and bonding dissimilar wafers [29], [30]. Various issues on wafer-level 3-D integration have been addressed [1]–[4], [10], [13], [31]. Among major 3-D processes, accurate alignment is essential between the bonded wafers to realize a high density of interstrata interconnects (i.e., TSVs and BISVs) and high volume throughput.

Historically, aligned wafer-to-wafer bonding was developed originally for MEMS process. Today, it is an important manufacturing technique not only for 3-D integration but also for advanced wafer-level packaging and microfluidics. The prebonding wafer-to-wafer alignment accuracy (i.e., pure

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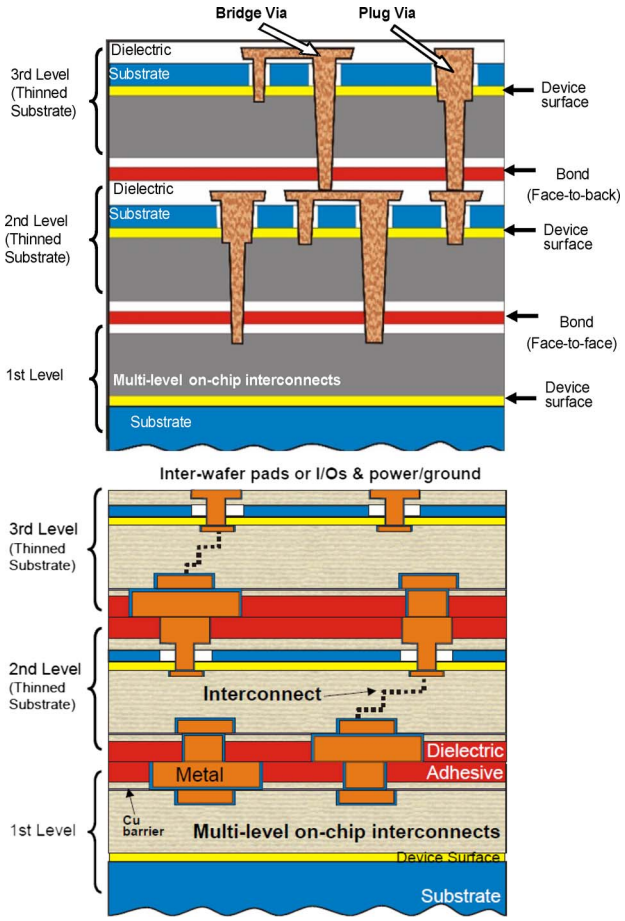

Fig. 1. Schematic representations of two major 3-D technology platforms for a monolithic 3-D hyperintegration showing (top) via-last and (bottom) via-first approaches [16]–[18].

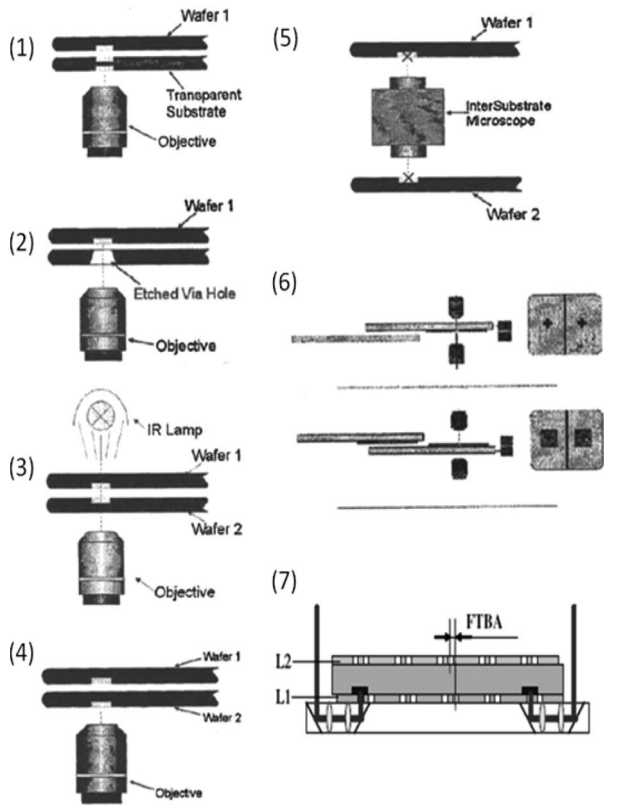

Fig. 2. Various types of alignment methods [21]–[28]. (a) Optical microscopy for transparent substrates. (b) Optical microscopy using through-wafer holes in combination. (c) IR transmission microscopy for IR transparent substrates. (d) Optical microscopy using front-to-backside alignment marks. (e) Intersubstrate microscopy for face-to-face wafer alignment. (f) SmartView alignment method. (g) 3DAlign method.

mechanical wafer-to-wafer alignment accuracy) can be achieved on the order of 0.25 μm using commercially available wafer-to-wafer alignment tools [30]–[35]. With continued efforts in developing wafer-to-wafer alignment tools, more precise accuracy toward the submicrometer regime of the wafer-level process can be achieved with tighter processing control [32]–[45]. However, it is difficult to improve the process-related misalignment by better alignment tools. The process-related misalignment has yet to be thoroughly studied, while it becomes more significant in MEMS and 3-D integration.

In this review paper, various alignment methods, accuracy requirements, and possible misalignment sources for MEMS and 3-D integration are addressed. Wafer-to-wafer alignment fundamentals, such as alignment mechanisms, uniformity, thermal mismatch, and materials, are discussed with detailed alignment results. Alternative alignment approaches and perspectives for wafer-to-wafer alignment are given.

II. Review of Alignment Methods

Compared to conventional mask-to-wafer alignment based on photolithography, wafer-to-wafer alignment is much more complicated. It requires different alignment concepts to align two processed wafers with devices (such as CMOS transistors).

In principle, wafer-to-wafer alignment uses alignment marks on two wafers to monitor the alignment process within an alignment tool. Once two wafers are aligned, they are temporarily brought into contact; at this stage, for optical or infrared (IR) transparent wafer, the misalignment can be inspected by imaging overlaid marks. The aligned wafers are usually transferred to a bond tool for wafer bonding. The misalignment can be inspected right after bonding or after substrate thinning by optical microscopy images of overlaid marks or by cross-sectional scanning electron microscopy (SEM) images of overlaid marks using focused-ion-beam (FIB) technique.

Various alignment techniques [32]–[45] have been introduced for wafer-to-wafer alignment, as shown in Fig. 2: 1) using the method for transparent substrates; 2) using through-wafer holes in combination with optical microscopy; 3) using IR transmission microscopy; 4) using front-to-backside alignment marks; 5) using intersubstrate microscopy [35], [36]; 6) using the SmartView alignment method [32], [33], [37]–[40]; and 7) using the 3DAlign method [34], [41]–[43].

A. Transparent Substrate

Similar to conventional mask alignment, optical microscope can view the alignment marks on the wafers through a transparent wafer (such as glass or some compound semiconductor wafers). Two wafers with alignment marks in a face-to-face fashion are aligned by moving the wafer stages until the alignment marks are overlapped. Alignment errors of ± 5 μm are not uncommon using this approach.

B. Through-Wafer Holes

As shown in Fig. 2(b), the alignment marks on one of the aligning wafers can be seen through the holes drilled or etched on the other. The dimension and position of the through-holes are very critical in this approach since the wafer with holes does not have particular alignment marks. It is very difficult for drilling and etching to reach the precise micrometer-level accuracy of the via-hole dimensions through the wafer substrate (e.g., $\sim$725-μm thickness for 200-mm silicon wafers). This technique is hardly to reach micrometer-level wafer-to-wafer alignment.

C. IR Transmission Microscopy

Instead of a visible light, an IR light is placed on one side of the wafer (opposite to the optical microscope), as shown in Fig. 2(c). Silicon wafers can be aligned since silicon is transparent to IR light. However, it is limited to the silicon wafers with polished double side surfaces. Alignment errors could be as small as ± 1 μm with this approach. However, the view is distorted by nontransparency of metal or heavily doped silicon layer.

D. Backside Alignment With Digitalized Image

Alignment marks are placed on the frontside (bond) of the first wafer and on the backside (counter-bond) of the second wafer. Similar to a mask aligner, alignment marks on the first wafer—face down toward the bottom microscope—is captured and stored as a digitalized image. The second wafer—bond face upward and alignment mark downward—is moved in between the first wafer and the microscope. The alignment marks on the backside of the second wafer are viewed and aligned with the stored image of the alignment mark on the first wafer. An alignment tolerance of ± 5 μm can be reached. It is critical to register well the alignment marks on the backside of the second wafer.

E. SmartView Alignment Method

Two pairs of microscopes (one pair on the "left" side and the other on the "right" side of the aligning wafers) are placed outside of the top and bottom wafers. The aligning wafers are placed "face-to-face" with a gap of less than 100 μm and vacuum-sucked on the top and bottom wafer stages, respectively. The two wafer stages can be moved back and forth horizontally. After the pair of top and bottom microscopes are aligned with each other (i.e., calibrated), the bottom wafer stage is moved inbetween the pairs of microscopes; the marks in the top microscopes are aligned to the alignment marks on the bottom wafer. The bottom wafer position is stored, and the bottom stage is retreated. The top wafer stage is moved to the position against the bottom microscopes. The alignment marks on the top wafer are then aligned to the bottom microscopes. The bottom wafer stage is moved back to its stored alignment position. Finally, the two aligned wafers are vertically moved to contact each other and are clamped to hold the alignment for wafer bonding. Misalignment tolerances can be achieved on the order of 0.25 μm in this method [32], [33], [36].

F. 3DAlign Method

It comprises two microscope sets and a modified wafer table. For double side aligning, one set views directly down to the frontside of a wafer and another set views through a special mirror like a modified periscope to the bottom side, as shown in Fig. 2(g). To align a wafer pair, the second microscope set views the bottom side of the second wafer. Two viewed images are overlaid and aligned. A submicrometer misalignment tolerance was demonstrated with this method [34], [42], [43].

III. Alignment Consideration on 3-D Platforms

Unlike conventional mask alignment in photolithography, the addition of a fully processed wafer or a handling glass wafer makes alignment more complicated. The alignment approaches described in Section II must be considered with each 3-D platform. Alignment marks and bond surface should be designed in advance for a given 3-D platform. Moreover, wafer bonding may cause further misalignment. Two alignment approaches possible for 3-D platforms [31], [41] are considered here in this paper: 1) face-to-face and 2) face-to-back.

A. Face-to-Face

At the bonding interface, the alignment marks on one wafer face the ones on the other wafer. In this case, alignment marks can be fabricated on the layer of top global interconnects. The alignment marks can also be fabricated on the CMOS layer if the frontside of the wafer is bonded on a temporary handle wafer (silicon or glass) and if the bulk silicon substrate of this wafer is removed. It is possible to view the aligning marks in a conventional mask alignment microscope only if a transparent wafer substrate is used (such as glass wafer using visible light or silicon wafer using IR). In this case, the alignment marks can be fabricated on either the layer of top global interconnects or the CMOS layer. With a nontransparent silicon substrate, there are a few ways to overlay the marks in this aligning method. SmartView, IR microscope, and intermicroscope are practically used for the face-to-face wafer alignment.

B. Face-to-Back

The alignment marks on both bonding wafers face toward a microscope, which means that the alignment marks on one wafer do not face those on the other wafer at the bonding interface. The backside alignment with digitalized image (as discussed in Section II-D) can be used with an optical microscope. With this approach, it is difficult to inspect the postbonding alignment accuracy with IR since the alignment marks on both wafers are not on the same focal plane. The face-to-face alignment method can also be used if alignment marks are fabricated on the backside of one wafer, although it is quite challenging to realize the alignment marks that are well aligned to the circuits on the wafer frontside.

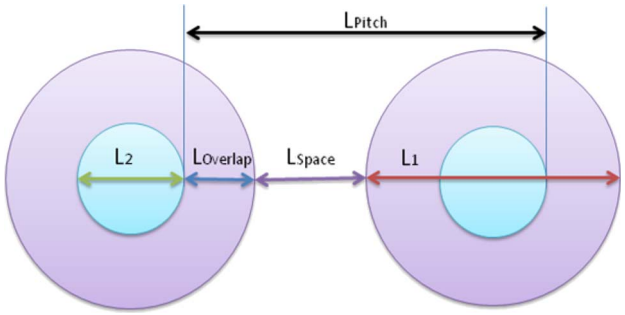

Fig. 3. Schematic of the bonding pads based on the via design rule. L_1 and L_2 are the diameters of the bonding pads on the first and second wafers, L_{Overlap} is the minimum overlay between the bonding pads on the first and second wafers, L_{Pitch} is the edge-to-edge distance of the bonding pads on the second wafer, and L_{Space} is the distance between two bonding pads on the first wafer.

In all of the 3-D platforms, after alignment, two aligned wafers may experience further thermal/mechanical processes such as bonding, thinning (grinding and polishing), further interconnect or redistribution layer formation, TSV formation, etc. These thermal/mechanical processes may affect the alignment accuracy obtained during the room-temperature wafer-to-wafer alignment. Therefore, those processes have to be evaluated and controlled for 3-D integration.

IV. Alignment Impact on Interconnect Via Density

Accurate alignment is a critical factor for high interstrata interconnection via density and multilevel stacking. Interstrata interconnection via density in wafer-level 3-D approach is directly related to the performance of the wafer-level alignment tool and the process control, which determines via pitch and size. The minimum pitch and overlap via size can be defined as follows [46]:

$$L_{\mathrm{Pitch}} = L_{\mathrm{Space}} + 2 \cdot L_{\mathrm{Overlap}} + L_2 \quad (1)$$

$$L_{\mathrm{Overlap}} = M_{\mathrm{Mean}} + 3 \cdot M_{\mathrm{Sdv}} + M_{\mathrm{Run\text{-}out}} \quad (2)$$

where L_2 is the diameter of the bonding pads (as shown in Fig. 3), $L_{Overlap}$ is the minimum overlay, L_{Pitch} is the edge-to-edge distance of the bonding pads on the second wafer, L_{Space} is the distance between two bonding pads on the first wafer, M_{Mean} is the mean of the wafer-to-wafer misalignment, M_{Sdv} is the standard deviation of the wafer-to-wafer misalignment, and $M_{\mathrm{Run\text{-}out}}$ is the maximum run-out misalignment. The maximum run-out misalignment may be controlled as discussed in the following sections.

For instance, with the current alignment technology, let us consider that both the mean and the standard deviation are 1 μm, and the maximum misalignment within a wafer with the best wafer bow control is also 1 μm. For the minimum landing pad size of 5 μm, the pitch size would be calculated as 12 μm if both via size and line spacing are 1 μm. The number of interwafer interconnects in an area of 10 mm^2 could be $\sim 2 \times 10^4$ when the interstrata interconnection area ratio (i.e., area of interstrata interconnects/die area) is 1% [9]. However, if the mean and standard deviation are 0.25 and 0.1 μm, the pitch size and the number of interstrata interconnects in the same area (10 mm^2) could be 5.1 μm and $\sim 6 \times 10^4$. The wafer-to-wafer alignment accuracy and the maximum misalignment with wafer are key factors affecting the pitch size and the number of interstrata interconnects, whereas the via size is dictated by the technology of via formation. As a comparison, a pitch size of 0.156 μm is projected for minimum global wiring pitch of microprocessor unit, and a pitch size of 0.1 μm is projected for Metal 1 wiring pitch of DRAM interconnect [19].

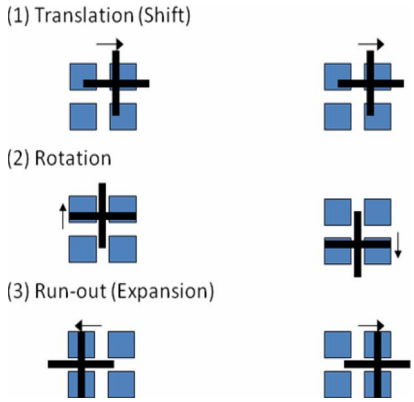

Fig. 4. Schematic of various misalignments. (a) Translation (shift). (b) Rotation. (c) Run-out (expansion).

V. Misalignment Category

Misalignments, such as translation (shift), rotation, and run-out (expansion) misalignment, have been studied in 2-D lithography in the form of mask-to-wafer alignment and in 3-D integration in the form of wafer-to-wafer alignment [38], [47], as shown in Fig. 4. Translation and rotation errors are steadily minimized by continued developments of commercial bond alignment tools, while run-out misalignment is still one of the most challenging issues in wafer-level 3-D integration because bonding/thinning processes inhibit maintaining the flatness of fully processed wafers in each layer-stacking process [47], [48]. Prior to wafer alignment and bonding, fully processed wafer may have certain compress or tensile stress on the device layer. Elevated bonding or debonding temperature enlarges the stress to induce wafer bow/warpage and nonlinear distortion [49]. Backside thinning makes internal shear stress dominated to the thin wafer, while a thick silicon substrate keeps the wafer flatness from the stress [49].

A. Thermal-Induced Misalignment

Thermal management has been a big hurdle for high-performance integrated circuit (IC) processing and could be even more important in multilevel 3-D integration [47]–[75]. Thermal-induced wafer distortion and mismatched thermal expansion of the wafers are the two major concerns in wafer-to-wafer alignment. For 3-D processing, the thermal expansion (run-out) error can occur in a wafer bonding/debonding process. It is critical to use materials with matched coefficients of thermal expansion (CTEs) and to control the temperature profile of any thermal processes. Table I shows the CTEs for the materials typically used in these 3-D integration platforms. As the CTEs of copper and BCB are much bigger than that of silicon, it is very delicate to integrate 3-D ICs that include

TABLE I
CTEs FOR THE MATERIALS COMMONLY USED IN SOME 3-D PLATFORMS

	CTE (ppm/°C)	Melting point (°C)	Young's modulus (GPa)
Si	2.5	1414	185
SiO_2	0.42	1600-1725	75
Si_3N_4	2.9	1900	210
GaAs	5.6	1510	86
InP	4.6	1330	61
Sapphire	8.4	2040	345
Pyrex 7740	3.2	820	72
Quartz	0.6	1670	63
Cu	16.8	1085	110-128
Au	14.2	1065	72
Al	26.5	660	70
In	35	156	12.74
Sn	25	232	50
BCB	32	350*	8.5
Polyimide 2611	5	360*	2.5

* Glass transition temperature

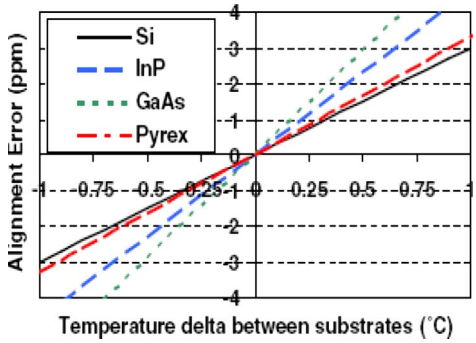

Fig. 5. Thermal expansion errors due to temperature differentials between bonded substrates [47].

copper or BCB. During wafer bonding, the temperatures on the two wafers that are to be bonded can be different because the aligned top and bottom wafers are usually heated separately by top and bottom hotplates. This temperature difference on the two wafers can result in different thermal expansions between these two wafers, leading to further misalignment (shown in Fig. 5). It is important to keep the bonding temperatures on the bond pair matched to avoid different thermal expansions.

It is also important to make sure that the stress of the device layer is released enough, thus reducing any wafer bow, which can also result in misalignment. Moreover, glass and silicon substrates are often used as transfer carriers. To minimize the residual stress from previous IC process, a CTE-matched low-stress polymer adhesive is required. In wafer bonding of dissimilar materials, the thermal expansion difference on the bonding pair would be significant; therefore, it is very difficult to keep the alignment unless the bonding process is done at room temperature or the bonding temperature profiles on the top and bottom wafers are so controlled to compensate the CTE mismatch.

B. Wafer Stress and Nonlinear Wafer Distortion

Wafer stress and localized wafer thickness variation induce wafer warpage/bow and nonlinear wafer distortion. Backside

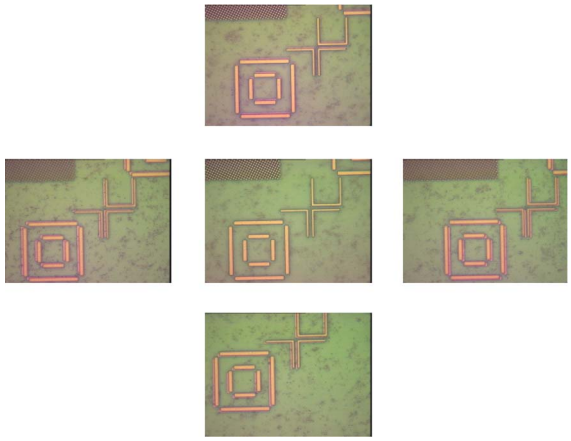

Fig. 6. Optical microscope images, taken at five spots on an aligned wafer pair, showing wafer-level "run-out" misalignments: 0.56- and 0.62-μm errors in 43.6-mm gap of the x- and y-directions from the wafer center for oxide fusion bonding [48].

wafer thinning such as chemical–mechanical polishing (CMP), grinding, and lapping makes internal residual shear stress revealed to the thinned wafer so that the wafer flatness is distorted nonlinearly. All of these types of nonlinear wafer distortions may cause further misalignments, as shown in Figs. 6 and 12 and Table IV. The localized thickness variation from nonuniform deposition or thinning can also induce the random directional expansion of alignment offsets in the x- and y-directions [47], [48].

VI. CASE STUDY OF THERMAL-INDUCED MISALIGNMENT

The correlation of misalignment and thermal management is discussed for four cases: 1) oxide-to-oxide bonding [49]–[52]; 2) metal bonding [53]–[65]; 3) adhesive bonding [66]–[71]; and 4) anodic bonding in MEMS application [72]–[75]. The postbonding thermal misalignment according to various wafer bonding methods for MEMS and 3-D integration and packaging applications is summarized in Table II. These following case studies show how the thermal mismatch affects alignment accuracy during 3-D processing.

A. Oxide–Oxide Bonding

This case is for a SOI-based 3-D assembly with the layer-transfer technology and oxide-to-oxide bonding [49], [50]. The device layer of a bonding wafer is transferred to a glass handling wafer by bonding and removing the silicon substrate. The n- and p-FET device layers are bonded together using PECVD oxide layers, and they are connected through inter-wafer through silicon vias (i.e., TSVs) [50]. A low-temperature PECVD oxide of 500 nm is deposited to both n- and p-FET wafer surfaces. Oxide layers are annealed at 300 °C and are smoothed using a CMP processing. Face-to-face alignment and bonding at room temperature were performed and annealed at 400 °C [49]. Whereas this transparency of a glass wafer provides good optical alignment accuracy, the CTE of the thin top layer with glass substrate does not match that of the bottom Si wafer. Upon the best alignment accuracy in the center area,

TABLE II
POSTBONDING ALIGNMENT ACCURACY IN VARIOUS BONDING APPROACHES [45], [50], [57], [61], [64], [69], [71]

Bonding method	Bonding temperature (°C)	Alignment accuracy (μm)
Silicon direct		
Si-Si	300	0.2
SiO_2-SiO_2	400	0.5
GaAs, InP	400	0.5
Metal compress		
Cu-Cu	400	0.5
Au-Au	400	0.5
Metal Euctetic		
An-Sn	280	2
Au-Si	363	2
Cu-Sn	231	2
Polymer		
BCB	250	0.5
Polyimide	300	2
SU-8	200	5
PMMA	200	0.5
Anodic		
Pyrex 7740	180-500	2-5

TABLE III
MISALIGNMENT RESULTS AFTER BONDING WITH DIFFERENT PROFILES [53]

Bonding profile	A	B	C	D
Misalignment x (μm)	2	0.5	2	0.5
Misalignment y (μm)	1.5	0.5	1	0.5

the alignment errors become larger toward the edges (so called "run-out"), as shown in Fig. 6. This run-out error due to thermal expansion can be analyzed by the study of wafer bow in the layer-transfer process of SOI-based 3-D assembly. The glass handle wafer is delaminated by a laser ablation technique. Fig. 6 shows the optical microscope images of wafer-level "run-out" misalignments: a 0.6-μm error in 43.6-mm gaps from the center. Misalignment is measured over the 200-mm wafer substrate in postalignment inspection before annealing. This run-out alignment error is caused mainly by the thermal stress of laminating the device layer to a glass handle wafer.

The alignment average (in micrometer), standard deviation (in micrometer), and run-out rate (in micrometer per millimeter) are measured as 0.16/0.26/0.0128 and 0.02/0.10/0.0156 for the x- and y-directions, respectively. Here, the run-out rate (in micrometer per millimeter) is defined as a misalignment error (in micrometer) over the distance (in millimeter) from the center of the wafer. The run-out error (expansion error), even after annealing, is 0.56 and 0.62 μm in the x- and y-axes on the die in the distance of 90 mm from the center, as shown in Fig. 6. These run-out errors may be explained as follows: 1) the large wafer bows at the steps of postlamination and postbonding film preparation caused the expansion mismatch between the glass and silicon device layers along with the large glass wafer bow; 2) during the expansion mismatch, a large residual stress was built on a silicon device layer from the previous steps; 3) thus, the patterns in the thin device layer are stretched out during the wafer bow correction step (preoxide bonding). Most of the bonding/debonding process involves inevitable thermal process. As an example of device layer expansion over a glass handle wafer during layer-transfer process regardless of glass wafer bow correction, Fig. 7 shows the wafer bow data at each layer-transfer process step in the oxide bonding even before the aligning and bonding steps. However, the measured large run-out after alignment means that the thermal expansion mismatch could not be corrected by bow correction of a glass handle wafer.

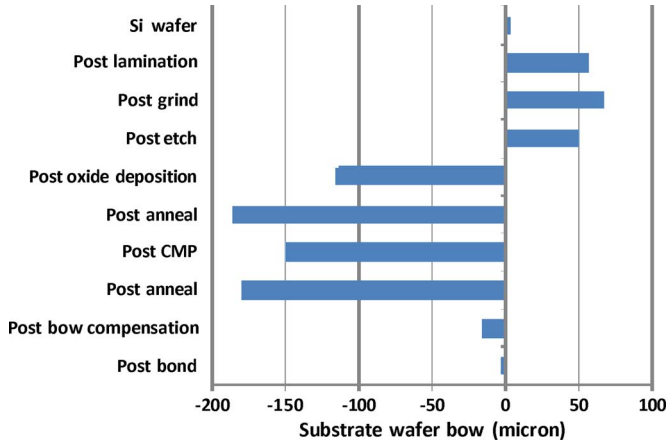

Fig. 7. Bow measurement at various process steps of the layer-transfer process. Bow compensation applied after the postanneal step [47], [50].

B. Metal Bonding

1) Thermal Compression Copper-to-Copper Bonding: The in-wafer thermal expansion mismatch between the copper via pads and the silicon substrate is discussed with the thermal expansion and the mechanical motion such as down-force and clamping [53]–[59]. It has been reported that copper-to-copper bonding surface can slide out by shear force of large down-force during bonding [54]. The bonding parameters such as down-force, bonding temperature, temperature ramping rate, and bonding time are sensitive factors in retaining the alignment during bonding. Experimental studies showed that bonding-induced misalignment can be improved by controlling the bonding parameters.

In one study [53], standard Cu interconnect damascene patterns were fabricated on both wafers, and then, an oxide layer was recessed by 40 nm lower than the Cu surface [58]. Cu round vias of 8μm were fabricated on the upper wafers, whereas 18-μm square landing pads were fabricated for the bottom wafers. In all bonding experiments, the bonding was conducted at 400 °C for 1 h, and no down-force was applied during the cooling cycle with a ~2-°C/min cooling rate, as shown in Fig. 8. The wafer-to-wafer alignment accuracy is measured using IR microscopy, looking at the alignment keys at the left and right wafer edges with a resolution in the range of 0.5 μm. Typically, Cu-to-Cu blank wafer bonding can be obtained with a high down-force (10 kN) at 350 °C−400 °C for 1 h, but patterned copper bonding becomes more complicated with thermal mismatch between the copper film and the silicon substrate. The following four different bonding profiles were further investigated based on the profile shown in Fig. 8:

Profile A: a small prebonding force of 1 kN, a fast ramping of 32 °C/min, and a full bonding force of 10 kN at 400 °C for 1 h;

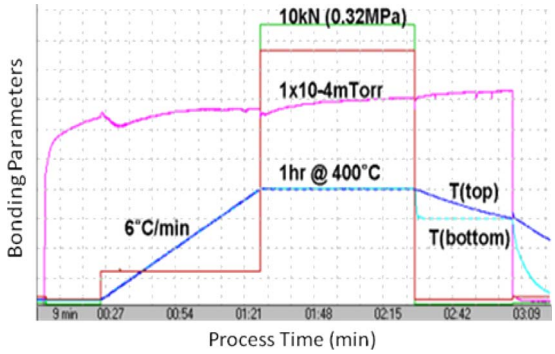

Fig. 8. Bonding process profile recorded. From the top in the middle area, (first line) down-force (10 kN), (second line) down-pressure, (third line) chamber pressure, and (fourth line) bonding temperature (top and bottom chucks) [48].

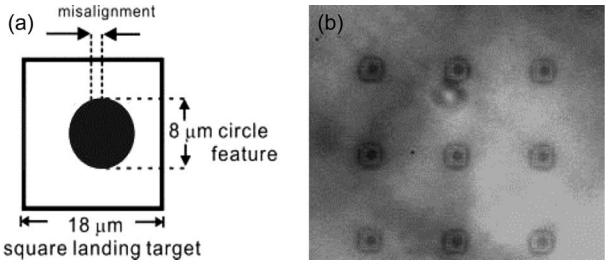

Fig. 9. (a) Schematic diagram of 8-μm Cu interconnects (with a pitch-to-diameter ratio of 10 : 1) bonded to 18-μm square landing pads. (b) IR image showing typical misalignment results after clamping and bonding for the same interconnect pattern geometry [53].

Profile B: a small prebonding force of 1 kN, a slow ramping of 6 °C/min, and a full bonding force of 10 kN at 400 °C for 1 h;

Profile C: no prebonding force, a slow ramping of 6°C/min, and a full bonding force of 10 kN at 400 °C for 1 h;

Profile D: a full prebonding force of 10 kN and a slow ramping of 6 °C/min, keeping the full bonding force at 400 °C for 1 h.

Fig. 9 shows the following: 1) a schematic diagram of an 8-μm Cu via bonded to an 18-μm square landing pad and 2) an IR image showing typical misalignment results after bonding. Table III shows the misalignment data for each bonding profile. Less misalignment error (within 0.5 μm) is obtained for profiles B and D, indicating that thermal control is an important factor to copper bonding because intimate wafer contact with prebonding force and slow ramping rate ensure that the temperatures on the top and bottom wafers stay closely the same during temperature ramping-up. To emphasize the importance of the thermal control, Fig. 10 shows wafer offsets (possible misalignment between two wafers) versus wafer temperature for several temperature differences between the wafers. As shown, a 1° temperature variation between wafers at 400 °C could cause a 0.6-μm offset of the 300-mm wafer ($\sim$0.4 μm even at room temperature) [57].

Fig. 11 shows the temperature differences between the top and bottom wafers for each bonding profile. For profiles B and D, with a slow ramping rate (6 °C/min), the temperature difference fluctuates within 5 °C. However, the temperature difference fluctuates up to 35 °C (varying slowly) for profile A

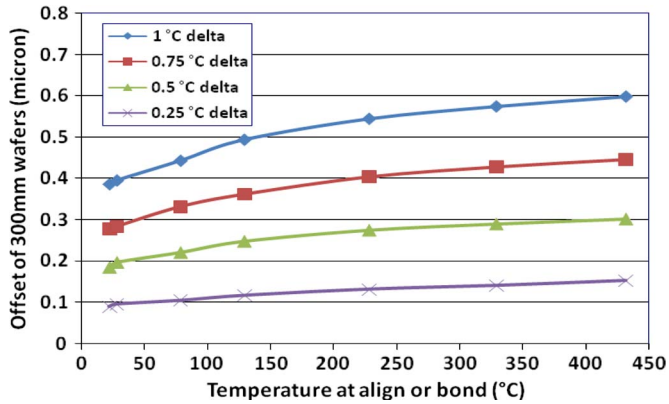

Fig. 10. Wafer offset versus temperature difference between wafers [57].

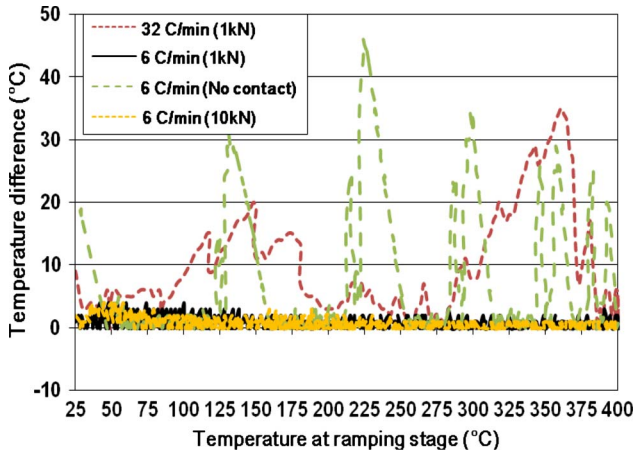

Fig. 11. Temperature difference and fluctuation during the ramping step. Fast ramping rate with 1-kN down-force, slow ramping rate with 1-kN down-force, slow ramping rate with no intimate contact between wafers, and slow ramping with 10-kN down-force [48].

(fast ramping and wafers in contact) and up to 45 °C (varying fast and frequently) for profile C (no intimate contact between wafers). A slow ramping rate (6 °C/min) avoids the large mismatch of the thermal expansions between wafers by keeping the temperature difference between wafers within 2°, as designed by the bonding tool. A fast ramping rate (32 °C/min) resulted in heating wafers with high overshoots due to a slow response of the heating to the thermal sensor's feedback. For profile C (no intimate contact between wafers), there is a large misalignment even at a low ramping rate, indicating that intimate contact between two wafers is essential to equalize the temperature of the wafers. The wafer contact step should be ahead of this temperature ramping. A 1-kN down-force should be enough to enable the intimate contact. To compare profile B with profile D, profile B is preferred because a large down-force could cause an undesired shear force during the temperature ramping [54].

Moreover, a large temperature difference with profiles A (fast ramping) and C (no intimate contact) could also cause a nonlinear and irregular expansion of the Cu/oxide damascene layer over Si substrate. This expansion may lead to possible nonlinear wafer warpage or bow along with surface morphology; thus, it should be avoided.

2) Eutectic Bonding: In MEMS and device packaging, eutectic bonding is widely used for hermetic seals and flip chip

bonding [60]–[65]. At eutectic point, a solid phase of alloy is directly transformed to a liquid phase. Using this soft bonding interface, metal alloy bonding is fulfilled without a high down-force. As an example of eutectic bonding, Au-Sn alloy has a composition ratio of Sn (20 wt%) and Au (80 wt%), and its eutectic point is 280 °C. The eutectic bonding was made under a down-pressure of 5000 mbar at 300 °C for 10 min. The liquid phase of alloys at eutectic point induces self-aligning to reduce the shearing force [60], [64]. However, since various metal alloys are bonded generally below 400 °C, a soft interface is able to provide a chance to heated wafer bond pair to be bowed or nonuniformly distorted. It causes a large thermal misalignment. A process control such as ramping time and a proper sequence of down-force and bonding temperature are required. Postbonding alignment accuracies of ∼2 μm can be expected [60], [65].

C. Adhesive Wafer Bonding

1) Permanent Bonding: Adhesive wafer bonding is a simple robust bonding process for 3-D integration and packaging due to the ductile and thermal deformable properties of polymer adhesives [66]–[69]. However, improper polymer or bonding processes can lead to large misalignment. Thermal expansion mismatch in adhesive bonding is more significant than in metal bonding. The thermal-induced misalignment can be affected by polymer thickness variation, reflow, and shear force due to the nature of the polymer (low viscosity at certain temperature). For instance, a little shear force may cause a large misalignment for a bonding polymer with very low viscosity (at the reflow temperature). Benzocyclobutene (BCB) has been verified as a very promising polymer for adhesive dielectric bonding because it is a thermo-set polymer without outgassing and has a high viscosity provided by cross-linking after curing. It was reported that a small thermal-induced misalignment (on the order of 1 μm) can be achieved using a partially cured BCB (with a high viscosity) in adhesive wafer bonding [64].

2) Temporary Bonding: Adhesive wafer bonding is also used for temporary handling support of the layer-transfer process [48], [70], [71]. Fig. 12 shows the change of alignment accuracy after wafer bonding, and Table IV shows the misalignment data over a 200-mm wafer substrate in postalignment inspection before annealing for polymer-to-polymer bonding [48]. Expansion errors occur even before the aligning step. The alignment average (in micrometer), standard deviation (in micrometer), and run-out rate (in micrometer per millimeter) for this polymer bonding are measured as −1.2/1.0/0.055 and 0.4/2.6/0.058 for the x- and y-directions, respectively. These misalignment data explain that a thick polymer bonding can induce severe misalignment. Fig. 13 summarizes the wafer bow data at each layer-transfer process step in this polymer bonding even before the aligning and bonding steps. This is a typical example of device layer expansion over a glass handle wafer during the layer-transfer process, regardless of glass wafer bow correction. It shows a large wafer bow (up to 200 μm) during postlamination and postbonding film preparation. The wafer bow of prebonding wafers is much improved to ∼50 μm by depositing a bow correction layer on the backside of the glass wafer. However, the run-out errors with this polymer bonding are very large, i.e., 4.95 and 5.22 μm in the x- and y-axis directions on the die in the distance of 90 mm from the center, as shown in Fig. 14. It means that thermal expansion mismatch could not be corrected by bow correction of a glass handle wafer.

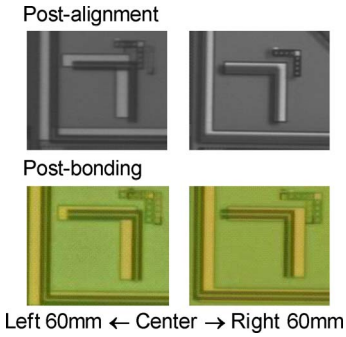

Fig. 12. Alignment changes before and after bonding [48].

TABLE IV
MISALIGNMENT DATA AND WAFER-LEVEL ALIGNMENT YIELD [48]

Bonding Type	Shift x (μm)	Shift y (μm)	Rotation (radian)	Run-out x (μm/mm)	Run-out y (μm/mm)
Center	0.1	0.6	-	-	-
Ave./Sigma	-1.2/1.0	0.4/2.6	-44.2	0.055	0.058

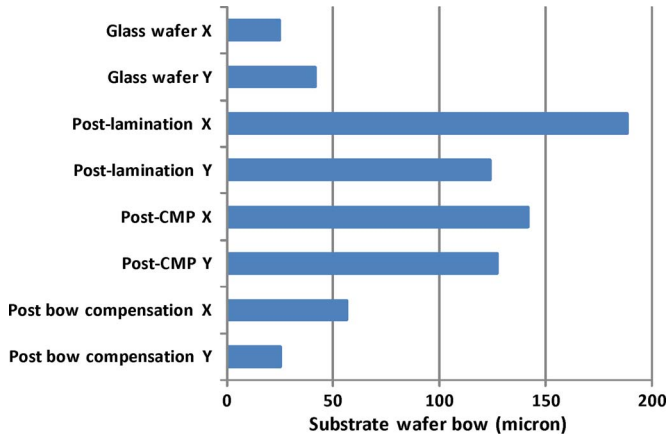

Fig. 13. Wafer bow measurement at each process step for temporary adhesive bonding [48].

D. Anodic Wafer Bonding

MEMS devices, including moving parts such as vibratory gyroscope and accelerometers, often suffer from misaligned wafer bonding and thermal stressed anodic bonding because the sensitive mechanical change is essential to the MEMS devices [72]–[75]. For example, in the decoupled vibratory gyroscope [72], resonators oscillating at their natural resonant frequency are very sensitive to the small deformation of the resonator induced by fabrication errors and/or thermal stress. Anodic bonding is the major process step causing thermal expansion mismatch in the fabrication of the gyroscope because the bonding is conducted at a temperature of 460 °C and at a voltage of 450 V. This high-temperature process brings out large wafer

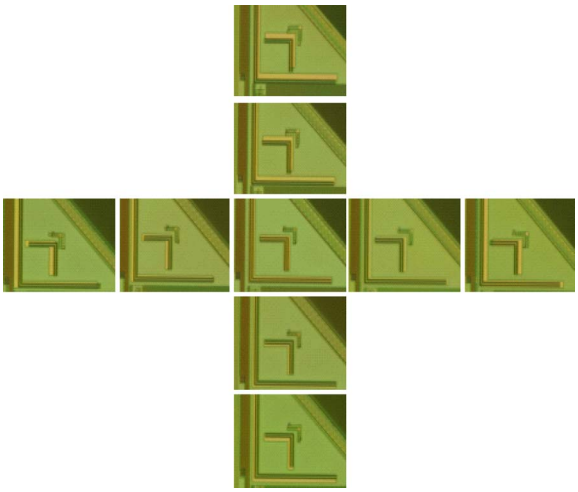

Fig. 14. Wafer-level misalignments. Optical images taken at nine spots on the wafer along the x- and y-directions, showing misalignments due to the process of layer-transfer using polymer adhesive. 4.95- and 5.22-μm errors in 90-mm gap of the x- and y-directions for polymer bonding [45].

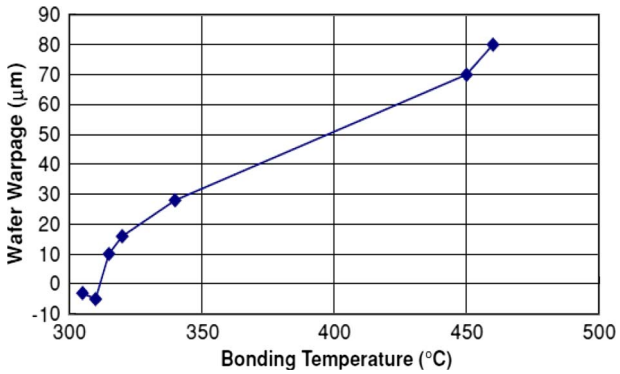

Fig. 15. Wafer warpage of the SOI wafer bonded to glass with increasing bonding temperature [72].

bowing, degrading the device performance. Fig. 15 shows the bonding temperature dependence of wafer warpage. The wafer bowing increases up to 80 μm as the bonding temperature elevates to 460 °C, while the bowing is 10 μm at 330 °C. Alignment accuracy can be achieved within ± 5 μm in the bow of 10 μm of silicon/glass anodic bonding. For a certain material such as 7070 glass, it induces bowing itself when bonding temperature reaches the strain point. The bow is in the opposite direction to the bow due to thermal expansion mismatch. This is used for bow control [75].

VII. Techniques to Alignment Accuracy Improvement

In order to reach or keep submicrometer alignment accuracy, better alignment tools are obviously required. Some possible solutions [5], [76]–[90] have been developed to prevent or reduce large misalignment, including thermally distorted misalignment in terms of process control.

A. Surface Heating

A temperature control unit can be employed to the alignment process. For example, if the top and bottom chucks are heated separately, the stressed wafer warpage could be relaxed temporarily before in-contact. Local or global surface heating compensates the different wafer warpage of two aligning wafers correcting the expansion offset [5].

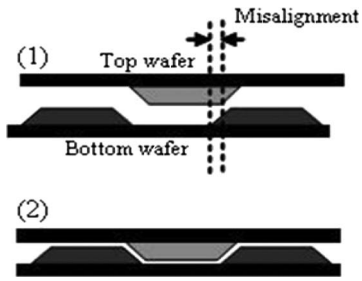

Fig. 16. Schematic drawing for a conceptual mechanical interlocking mechanism. (a) Tapered surfaces slide in the misalignment range. (b) Key structures are interlocked [75].

B. Mechanical Interlocking

1) Anisotropic Etched Silicon Structure in MEMS: Using the anisotropic (KOH) etching of silicon, the concept of mating pyramid (convex) and groove (concave) elements can be used to improve the wafer alignment accuracy down to a few micrometers and better as a passive mechanical wafer alignment technique by sliding to mate and locking the structure [76], [77]. Potential applications of this technique are precision alignment for bonding of multiwafer MEMS devices and 3-D ICs, as well as one-step alignment for simultaneous bonding of multiple wafer stacks. Alignment accuracy can be achieved as better than 200 nm at the bonding interface [77].

2) Transfer–Join Approach: In this approach [6], [78], the pillarlike copper key structure (Cu stud) is plugged into polymer-pocketed copper pads. The pocketlike lock is provided at the bottom with a Cu pad that is to be bonded to the Cu stud later. The stud and the combined thickness of the adhesive and the insulator are adjusted so that the Cu-stud-to-Cu-pad contact is first established during the bonding to form a metal–metal bond. Under the continued bonding pressure, the stud height is compressed, and the adhesive is brought into contact with the opposing insulator surface and bonded. There is no sliding guideline between the stud and the pad. Only the polymer window to the pad keeps the stud from later expansion misalignment. For this approach, the bottom lock structures are designed to be larger than the key structures. Therefore, there is room to accommodate misalignment during operation.

3) Tapered Keyed Structures: Similar to the anisotropic etched silicon structures in MEMS, a tapered structure on the bonding surface can be created to interlock the wafers mechanically [79]. The conceptual mechanism [80] is that the keyed structures can slide into each other along the tapered planes and are mechanically interlocked so that it can prevent wafers from shifting relative to each other and so that wafers can maintain their aligned position during the bonding process. Fig. 16 shows a conceptual mechanical interlocking mechanism: 1) the tapered surfaces slide in the misalignment range, and 2) the key structures are interlocked. The measured alignment accuracies are shown in Fig. 17. Preliminary results also indicate

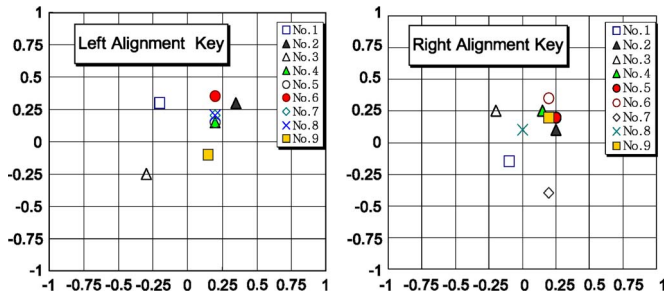

Fig. 17. Wafer alignment accuracy using the keyed alignment structures after alignment, contact, and clamping, showing a standard deviation of the alignment accuracy within a quarter micrometer [75].

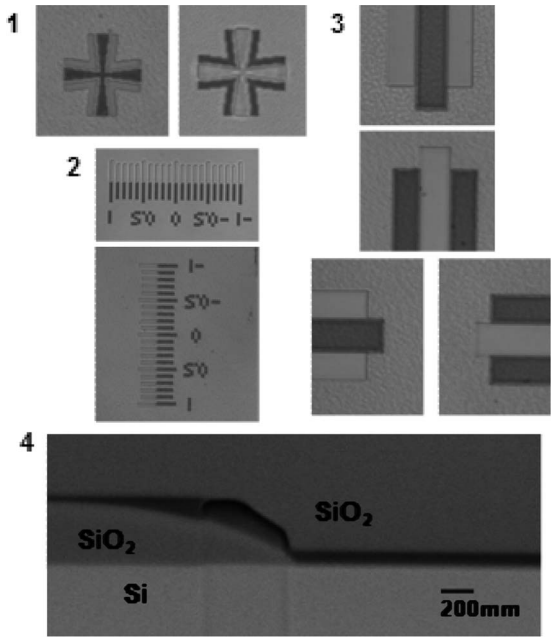

Fig. 18. Optical 20× images of the overlaid keyed structures. (a) Alignment marks. (b) Vernier structures for reading alignment accuracy. (c) Bar interlock structures. (d) SEM image of cross-sectional view of interlocked structures.

that these self-alignment structures at the wafer surfaces can adjust and improve the prebonding wafer-to-wafer alignment accuracy to well below 1 μm, approaching 100 nm. Fig. 18 shows the optical 20× images of the keyed structures used for the measurement of alignment accuracy: overlaying alignment marks, vernier structures for reading alignment accuracy, bar interlock structures, and SEM image of the cross-sectional view of the interlocked structures. For the via-last process, this keyed interlocking concept is more feasible since the tapered key structure is easy to implement on the bonding surface (oxide or polymer adhesive).

For the via-first process, it should be patterned into the surface of copper/oxide or copper/dielectric redistributed with more process steps. This may affect the surface condition or may cause thermal distortions of aligning wafers. To prevent thermally induced postbonding misalignment, the keyed structures can provide the additional fiction into a mating surface to prevent bonding-induced thermal misalignments. As an example, the keyed alignment structures were aligned and bonded using a 0.2-μm-thin BCB layer. Fig. 18(d) shows an FIB–SEM image of the cross section of the keyed alignment structures on

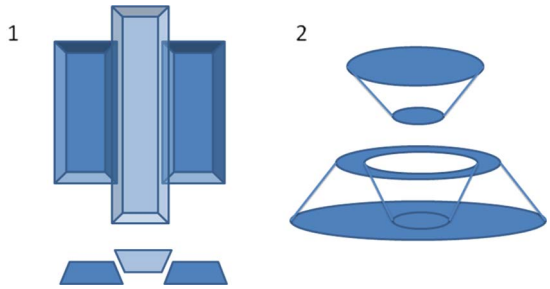

Fig. 19. Schematic of conceptual keyed structures. Pyramidlike and cornlike.

the left side of the wafer stack, describing that the misalignment is reduced and maintained.

To improve the sliding effect, the two design modifications of the keyed structure are discussed as follows, i.e., pyramid and corn structures, shown in Fig. 19. A pyramidlike structure offers a large contact area with long tapered plane, which enables a strong key-locking effective, whereas a large friction generated in a large rotation alignment error would hinder the locking effect. On the contrary, a cornlike structure has a small contact area, providing less locking effect but more freedom of error correction, especially rotation and run-out errors. The size and angle of the tapered structure determine allowable alignment tolerance, possibility, and thickness of the bonding layer. A stiffer tapered angle provides a shorter travel range to correct misalignment. Using vertical down-force when two wafers brought together, key-lock structures slide into each other in a horizontal direction to correct the misalignment. Tapered slope and down-force should be optimized to give enough force for the wafers to slide. The number of keyed structures can be two or more along the edge of the wafer. However, more keyed structures make the sliding and locking of keyed structures more difficult.

C. Submicrometer Aligned Wafer Bonding Via Capillary Forces

The alignment concept of capillary forces and surface tension was introduced to die-to-die or die-to-wafer bonding [82]–[86]. A droplet of waterlike liquid can hold a die on another die or a substrate to an alignment accuracy of a micrometer since the strong surface tension can pull and keep a die in micrometer scale. The capillary-force-assisted self-alignment method is applied to wafer-to-wafer aligned bonding, shown in Fig. 20 [86]. In this process, liquid droplets are applied uniformly at the interface. The droplets via capillary forces minimize their surface energy at the pinning boundaries of the droplets. Fig. 21 shows the average misalignment across the wafer as a function of the number of droplets used. It explains that the misalignment is reduced over the increasing droplet density [86]. One critical huddle is to apply the droplets across the entire wafer. The other is to eliminate the unnecessary residual liquid at the wafer interface before wafer bonding.

VIII. Alignment Characterization Techniques

Accurate alignment inspection and read-out offer iterative feedback correction and analysis for the development of

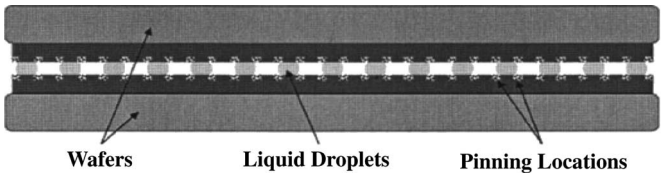

Fig. 20. Schematic of the capillary-force-assisted wafer bonding [86].

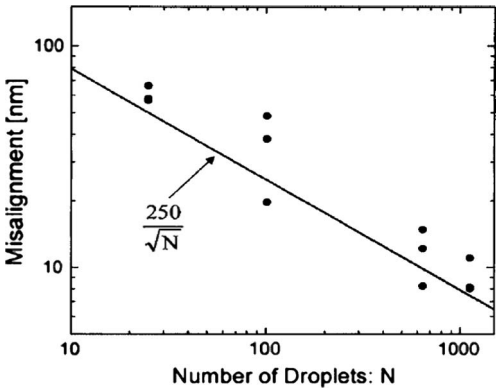

Fig. 21. Average misalignment across the wafer due to patterning error as a function of the number of droplets used [86].

alignment techniques. Alignment inspection is being investigated for commercialization of this 3-D technology [87]–[94]. Alignment accuracy is characterized usually at two stages: prebonding and postbonding. Prebonding alignment inspection is limited to in-focus checkup. Postbonding alignment is difficult to inspect since the aligned marks are at the bond interface. In practice, three methods are used for 3-D integration: optical, IR, and cross-sectional inspections. While the first two methods are nondestructive methods, optical inspection is limited to a transparent wafer. It requires a transparent handle wafer to view the alignment marks on the multistacked device layers. IR inspection provides the real-time reading of nontransparent silicon bonding. However, IR lights are attenuated along with the thickness of the silicon and cannot pass through multilayered metal lines. Cross-sectional destructive approach provides the most accurate alignment inspection. It may be feasible only at a research and development stage. To realize high-precision wafer-to-wafer alignment and nondestructive measurement of misalignments, a variety of inspection methods such as the 2-D Moiré method is developed [87], [89], [91].

IX. Summary and Conclusion

The wafer-to-wafer alignment techniques and issues for wafer-level 3-D integration have been reviewed and discussed. Alignment accuracy directly affects the density of TSVs and BISVs (hence the applications of 3-D integration). Various wafer alignment approaches have been developed. An alignment accuracy of 1 μm or smaller can be achieved, depending on the alignment approaches and 3-D applications. Thermal expansion at various wafer processing stages (i.e., prior to, during, and after wafer alignment) is a significant factor affecting 3-D wafer alignment for the major wafer bonding schemes. For oxide fusion bonding proposed using an SOI-based 3-D assembly process, a layer-transfer process affects the wafer-level alignment yield. For copper bonding, modifying the bonding process parameters can reduce thermal-expansion-induced misalignments. For adhesive bonding, increasing the viscosity of the thermal setting material can prevent shear-bonding-force-induced misalignments. Keyed alignment structures using a mechanical interlocking mechanism can further improve the alignment accuracy and can prevent thermal-expansion-induced misalignments.

Wafer stress engineering, thermal process control, and 3-D platform selection are critical for 3-D wafer alignment. Precise alignment issues are yet to be fully addressed, whereas alignment tools are being developed toward deep submicrometer mechanical alignment accuracy at room temperature.

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