Multi-Objective Display Panel Design Optimization using Circuit Simulation-Based Evolutionary Algorithm

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***Abstract*— We for the first time implement a multi-objective evolutionary algorithm (MOEA) to optimize the display panel gate driver circuits with amorphous silicon thin-film transistors (ASG driver circuit). The MOEA is integrated with a circuit simulator based upon a unified optimization framework. The results of this study indicate the developed optimization flow can find the better solutions than a simple GA. The measurement data of the fabricated sample further show the achieved result is robust and superior to the original design. This approach benefits design and manufacturing of display panels in the industry of information and communications technology.**

Keywords – Multi-objecive Evolutionary Algorithm, NSGA-ll Sensistivity, Panal Driver Circuit.

I. INTRODUCTION

For display panel manufacturing, the circuit on amorphous silicon is an attractive and unstoppable approach because of the elimination of the driver ICs, single with low-cost processes. Therefore the integrated gate circuit on amorphous silicon (ASG driver circuit) [1, 2] is used on TFT-LCD [3]. However, the amorphous silicon has underperformed characteristics and leads to some barriers to design integrated circuits. For example, it likes the less mobility of carriers because the lack of p-type transistors, the self-heating effect causes the circuit performance degeneration. For above reasons, a designer, who wants to design advanced ASG driver circuits, needs strong domain knowledge to size the ASG driver circuits repeatedly for achieving required specifications. In consideration of that, a simulation-based optimization program by genetic algorithm (GA) for automatic sizing was reported in our recent work [4]. It reaches an astonishing result, but this approach only can solve the single objective function. However, the engineering optimization is multi-objective problem generally [5-8].

In this work, we perform a circuit-simulation based multi-objective evolutionary algorithm (MOEA) for display panel circuit design optimization using fast non-dominating sorting genetic algorithm (NSGA2). The NSGA2 can be implemented on the unified optimization framework (UOF) and shows good computational performance. Achieved results are fascinating and better than the reported data using GA [4]. Moreover, how to choose proper solutions among the numerous results resulting from the MOEA is crucial issue. To solve the problem, we further use the technique of sensitivity analysis to make a decision. We thus successfully suggest an optimization flow for multi-objective display panel circuit design optimization.

This paper is organized as follows. Section II introduces the proposed flow and its background. Section III shows the tested ASG driver circuits and states the optimization problems solved by proposed flow. In Section IV, the results are discussed. Finally, we draw the conclusions.

II. BACKGROUND AND THE PROPOSED ALGORITHM

A. Genetic Algorithm

Genetic algorithm [9-10] is a population-based optimization method, as shown in Fig. 1. According to simulated natural including mutation, selection, and recombination, GA can select the individuals relatively better to compose the "gene pool" and then recombination operator is applied to generate the new offspring. The mutation operator may change the individual in the offspring. Finally, the new offspring is set to the "pool" and take the operation iterative until stop criteria is achieved.

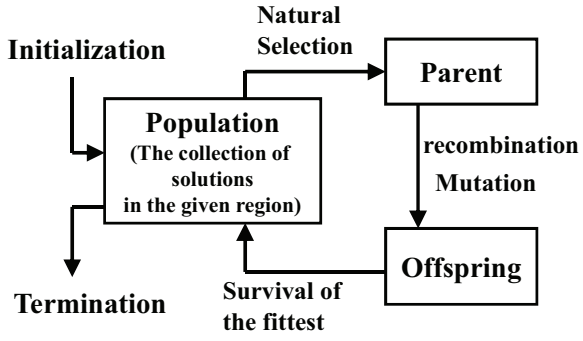

Figure 1. Iliustration of the genetic algorithm, which consists of the mutation, selection, and recombination.

978-0-7695-4919-4/12 $26.00 © 2012 IEEE
DOI 10.1109/TAAI.2012.48

B. Multi-Objective Evolutionary Algorithm

In this work, we use NSGA2 to solve the multi-objective problem [8,11] which can find multiple Pareto-optimal solutions in one single simulation run. One of the main differences between the conventional GA and the NSGA2 is that the NSGA2 modifies the fitness before the selection of parent on the objective space distinct from the decision space, as shown in Fig. 2. Because the NSGA2 can find the Pareto front on the objective space, it can get the many excellent spreads of solutions. The decision-makers can choose the solution according to their requirements. It is quite different from the conventional GA which only has one and only one solution.

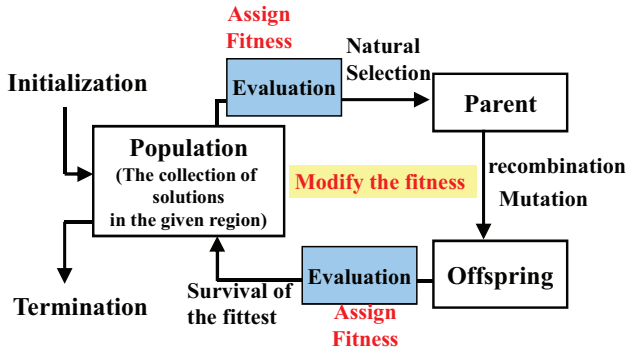

Figure 2. A evolutionary flow of the MOEA, which modifies the fitness from the conventional GA.

C. Unified Optimization Framework

Unified optimization framework [12] is an object-oriented optimization framework for general problem optimization developed in our earlier work. UOF has shown diverse applications in the fields of electrical and computer. Its cells include "Solver", "Evaluator", "Initializer", and "Problem"…, etc, as shown in Fig. 3. In this work, we modify the objects, the Solver, and the Problem in the UOF. We combine the solver to the MOEA and define the problem to the ASG driver circuit.

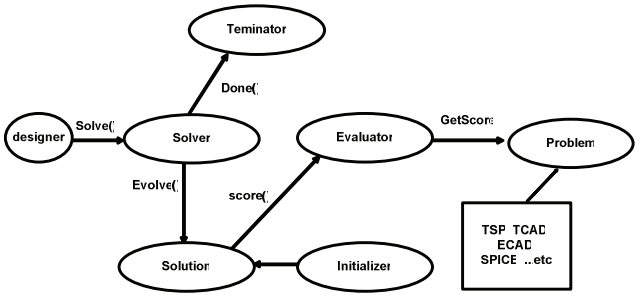

Figure 3. Illustration of the UOF. The designer use the "Solver" to optimize the solution wich is defined by the "Problem". The "Evaluator" is to get score form the "Problem" for each solution. "Initializer" is used to get the initial value for problem.

D. Sensitivity Analysis

Sensitivity analysis is a method that can find the influence of each parameter of the circuit design. We can discover the relationship between each parameter, and beyond this, it can help us to choose the solution with lowest sensitivity to avoid the process variation during the fabrication of display panel circuits. For the ASG driver circuit, the sensitivity is analyzed for the intrinsic parameters by varying 0.5 μm of each device's width. The normalized sensitivity equation is shown as:

$$\text{Normalized Sensitivity: } Z_i = \left| \frac{\partial f_0^*/f_0^*}{\partial x_i/x_i} \right| \times 100\%. \qquad (1)$$

E. Overall Optimization Flow for the Display Panel Circuit

Figure 4 shows the flowchart of the application flow. First, we put the setting files which describe the circuit and parameter of the optimization process. For example, the parameters are the size of each transistor, the capacitance, or inductance … etc.

Second, we use the UOF [12] to be the interface to optimize the circuit characteristics. Based on evolutionary algorithms, numerical deterministic methods, and C++ objective design, the UOF possesses real-world applications for various optimization problems. The UOF is with an interface between the defining a general problem and generic solver. The UOF's components are categorized into problem and solver parts, and they work independently. Therefore, the reusable high level code allows the adaptation to new problem and solver quickly. In this study, we have successfully developed a new solver of MOEA within the framework of UOF.

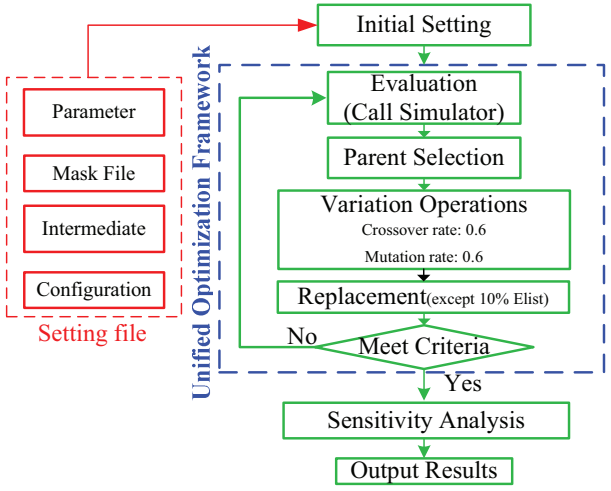

Figure 4. The optimization flowchart of the proposed flow. It combines the MOEA and sensitivity analysis by our UOF. The setting file includes parameters to define the instrinsic parameter, Mask file combines with parameters into intermediate file to run the simulator. And, the configuration file sets the MOEA's parameters.

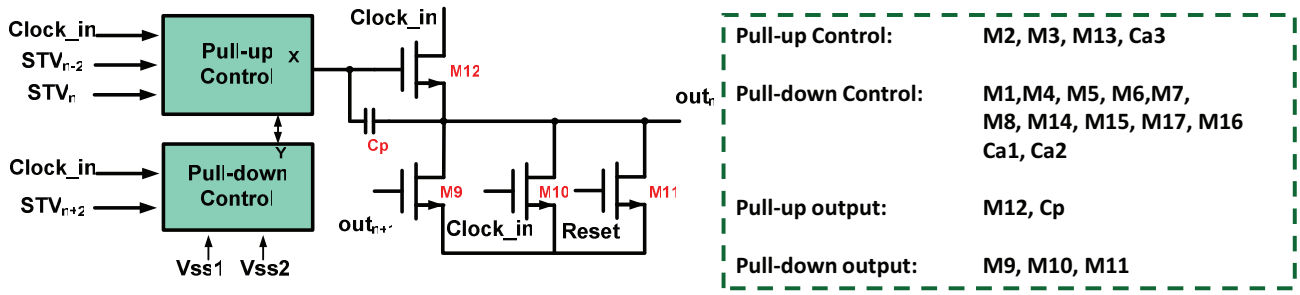

Figure 5. A block diagram of the tested 10.1 ASG drive circuit in this study. Each block contains TFTs and capacitors to be optimized.

The final step is the sensitivity analysis. With many variables in the circuit design, the sensitivity analysis can define the instability of each parameter. Consequently, it can make the designer knows which parameter is important. In this flow, we use the sensitivity analysis to help us to choose the solution, as shown in Fig. 2, from the evolutionary processes of MOEA. The analysis can point out the solution which has the lowest sensitivity and indicate if they are more stable and suppress the process variation. We perform the UOF to run the MOEA and then to optimize the circuit and find the Pareto front on the objective domain. The sensitivity analysis is thus to examine the robustness of the optimized solutions. We choose the lowest sensitivity solution as the best one. We can write the entire algorithm as the following pseudo codes:

```
UOF(){
Setting_File(Paramter, Mask, Intermediate, Configuration);

initialize();

while( Meet_Criteria == 0 )
      Call_Simulator();
      Evaluation();
      AssignFitness();
      Parent_Selection();
      Variation_Operations(Crossover_rate=0.6,
      Mutation_rate=0.6);
      Replacement(Elist=0.1);
end

Sensitivity_Analysis();
return output;
}
```

III. The Circuit Design Problem

A. The Tested Circuit

The tested circuit is the ASG driver circuit which could be applied to display panel production. The circuit has 21 parameters, which include 17 transistors' width and 4 capacitances' dimensions. The important dynamic electrical characteristics of the tested circuit such as, the rise/fall time, and the ripple, are significant for evaluating the performance of the specified design. In practical, these characteristics are not only requested to meet given specifications to promise the quality of the display panels but also hoped to minimize for performance improvement.

B. The Formulated Optimization Problem

To optimize the explored circuit [13], we choose the rise / fall time and the ripple as the multi-objective functions to be minimized. All parameters and the objective function have their associated constraints. In this problem, we optimize the width of each transistor with the help of search range definition by empirical assignment and the evaluation task is mainly by running the external circuit simulator. The problem can be defined as follows.

$$\begin{aligned}
&\text{Min} \quad \text{riseTime}\,(w),\\
&\qquad \text{fallTime}\,(w),\\
&\qquad \text{ripple}\,(w)\\
&\text{simultaneously, as } w = [w_1, w_2, \ldots, w_{21}];\\
&\text{s.t. riseTime}\,(w) \le SPEC_R\\
&\quad \text{fallTim}\,(w) \le SPEC_F\\
&\quad \text{ripple}\,(w) \le SPEC_P\\
&\quad w_{min} < w < w_{max}
\end{aligned}$$

The vector w is the parameters of the tested circuit. Each parameter has its lower and upper bounds w_{min} and w_{max}, respectively. In the following simulations, V_H, V_{ss1}, and V_{ss2} are set to 26.5 V, -5.5 V, and -10 V, respectively, the row line load is approximated by a six-stage RC circuit, and the length of each TFT is fixed to 4.5 μm. Figure 4 and Table 1 show the simulation results of the original and the MOEA optimized designs. The rise time is defined by the interval of time required for leading edge of the pulse raised from 10% to 90% in the peak pulse amplitude and the definition of fall time is contrary to rise time. The ripple of the output node, denoted as ripple-X, is defined by the maximum voltage level after the desired pulse. In addition to the above characteristics, we pay

special attention to the ripple of X node (denoted as ripple-X). The original design shows excellent performances on the rise time and fall time, but the ripple-X is poor.

TABLE I. THE COMPARISON OF THE TFT'S WIDTHS OF ORIGINAL AND OPTIMIZED DESIGNS (THE UNIT OF ALL TRANSISTORS IS MICROMETER).

	The Simulation Results			
	Spec.	***Original***	***GA_opt***	***MOEA_opt***
Rise Time(μs)	< 3	1.91	1.86	2.37
Fall Time(μs)	< 2	0.88	0.84	1.04
X Ripple(V)	< -5.5	-3.02	-2.54	-7.17
CK-C_{tot}(pf)	< 21.18	17.12	17.87	14.63

IV. RESULTS AND DISCUSSION

A. The Optimized and Measured Results

The optimized circuit is fabricated and measured. After the optimization, we successfully maintain all characteristics in the desired specifications and the ripples of the solutions are dramatically decreased. The Ripple-X is reduced from -3.0203 V to -7.1729 V. The improvement promises the robustness of stable output waveform. The Table II indicates the original and optimized sizes of the circuit. The summations of widths of original and optimized design are 9962 μm and 8312 μm, respectively.

TABLE II. THE COMPARISON OF TFT WIDTHS OF ORIGINAL AND OPTIMIZED DESIGN (THE UNIT OF ALL TRANSISTORS IS MICROMETER).

	M14	***M13***	***M15***	***Ca3***	***M16***	***Ca1***	***Ca2***
Original	30	520	60	1.3p	90	50f	50f
Optimized	10	350	50	0.6p	100	44.7f	43.4f
	M1	***M2***	***M17***	***M5***	***M4***	***M6***	***M7***
Original	12	600	50	60	18	120	120
Optimized	10	660	30	20	80	60	60
	M3	***M8***	***Cp***	***M12***	***M9***	***M10***	***M11***
Original	700	150	6p	5400	800	800	450
Optimized	400	120	10p	4400	970	910	590

Sensitivity analysis is an important strategy applied on the circuit design to verify how small changes in the fabrication affect the electronic characteristics. If the f_0 (x^*) represents the characteristic in the analysis point (the nominal case), the sensitivity of f_0 in x^* respect to x_i is defined as Eq. (1). In our simulation and verification, the sensitivity is further performed for all cases with varying (plus and minus 5%) device's width of the optimized circuit. The achieved results reveal the characteristic dependency is continuously varying with significant variation of device's width. According to the achieved results, the analysis of sensitivity with respect to device's width is less than 10%, which confirms the stability of optimized results.

In addition, the measured rise time of sample is better than theoretically simulated data, as shown in Table III. All the achieved electrical characteristics are in the specifications. The measurement data has demonstrated the feasibility of the proposed optimization.

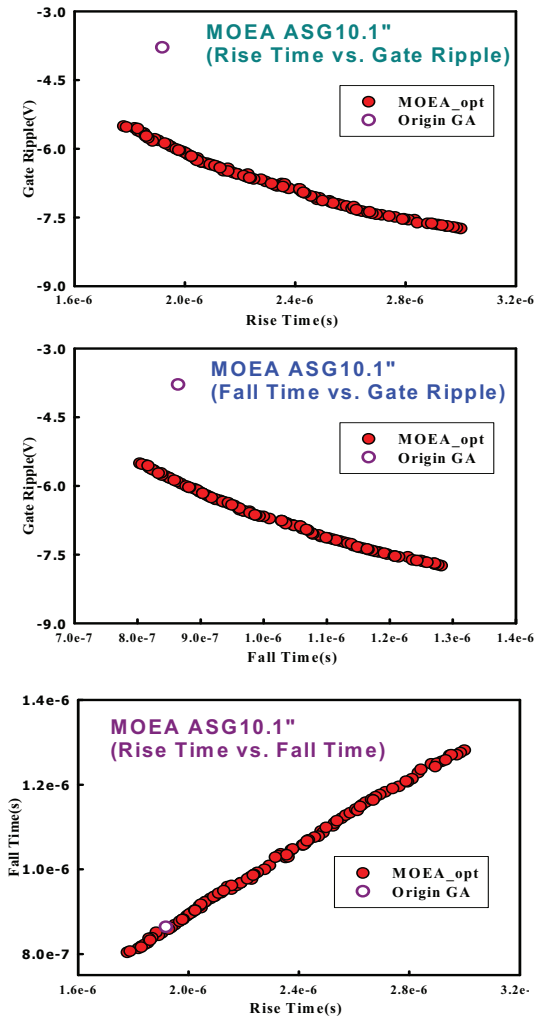

Figure 6. Pairwised comparision between the MOEA and the GA reveals the MOEA can obtain interesting solutions on each dimension, compared with the results of conventional GA.

B. Comparision between MOEA and Conventional GA

The result of the simulation is shown in Table I. The MOEA can get the better solution on each dimension in Fig. 6. The conventional GA solves the multi-objective problem using the weighting, so it can only find a solution on the Pareto front.

GA needs to try different weighting to find the superior solutions. GA can't optimize all the objective function at the same time. As listed in Table I, the GA can only get excellent performance on some dimension not all dimensions.

TABLE III. THE MEASUREMENT DATA OF THE SAMPLE.

Approach	Electrical Characteristics		
	***Rise Time* (μS)**	***Fall Time* (μS)**	***Ripple* (V)**
Spec.	< 3	< 2	< -5.5
MOEA_opt	1.74	1.96	-6

V. CONCLUSIONS

In this work, we have successfully used the multi-objective evolutionary algorithm to optimize the ASG gate driver circuit. The optimized design has superior characteristics including the rise time, fall time, and output ripple. Besides, the stable output waveform can be guaranteed by reducing the ripple of X node and also minimize the power consumption. For fabrication consideration, the sensitivity analysis is also implemented to verify the design, and the results show excellent practicability. And the achieved measurement data have demonstrated the feasibility of the propose optimization.

ACKNOWLEDGEMENT

This work was supported in part by Taiwan National Science Council (NSC), under Contract No. NSC-101-2221-E-009-092, NSC-100-2221-E-009-018, and NSC-99-2221-E-009-175, and by the Chimei-InnoLux Display Corp. Miao-Li, Taiwan under a 2009-2011 grant.

REFERENCE

[1] V. Vaidya, S. Soggs, K. Jungbae, A. Haldi, J. N. Haddock, B. Kippelen, and D. M. Wilson, "Comparison of Pentacene and Amorphous Silicon AMOLED Display Driver Circuits," *IEEE Transactions on Circuits and Systems I: Regular Papers,* vol. 55, pp. 1177-1184, 2008.

[2] Y. Li, K.-F. Lee, I.-H. Lo, C.-H. Chiang, and K.-Y. Huang, "Dynamic Characteristic Optimization of 14 a-Si:H TFTs Gate Driver Circuit Using Evolutionary Methodology for Display Panel Manufacturing," *Journal of Display Technology,* vol. 7, pp. 274-280, 2011.

[3] C.-H. Shen, Y. Li, I.-H. Lo, P.-J. Lin, and S.-C. Chuang, "Modeling temperature and bias stress effects on threshold voltage of a-Si:H TFTs for gate driver circuit simulation," in: *2011 IEEE International Conference on Simulation of Semiconductor Processes and Devices* (*SISPAD*), 2011, pp. 251-254.

[4] I.-H. Lo, Y. Li, and K.-F. Lee, "Hybrid Genetic Algorithm with Mixed Mutation Mechanism for Optimal Display Panel Circuit Design," in: *2010 IEEE International Conference on Technologies and Applications of Artificial Intelligence* (*TAAI*), 2010, pp. 222-225.

[5] P. A. N. Bosman, "On Gradients and Hybrid Evolutionary Algorithms for Real-Valued Multiobjective Optimization," *IEEE Transactions on Evolutionary Computation,* vol. 16, pp. 51-69, 2012.

[6] M. A. C. Pacheco and M. M. R. Vellasco, "Automatic repair techniques for analog circuits," in: *2002 IEEE International Conference on Industrial Technology* (*IEEE ICIT '02*), 2002, vol. 2, pp. 804-809.

[7] P. Changhao, W. Jin, and L. Zhiyong, "Using MOEA to evolve a combinational circuit on a FPGA chip," in: *7th World Congress on Intelligent Control and Automation, 2008* (*WCICA 2008*), 2008, pp. 6267-6271.

[8] K. Deb, A. Pratap, S. Agarwal, and T. Meyarivan, "A fast and elitist multiobjective genetic algorithm: NSGA-II," *IEEE Transactions on Evolutionary Computation,* vol. 6, pp. 182-197, 2002.

[9] J. Vesterstrom and R. Thomsen, "A comparative study of differential evolution, particle swarm optimization, and evolutionary algorithms on numerical benchmark problems," in: *Congress on Evolutionary Computation, 2004* (*CEC2004*), 2004, Vol. 2, pp. 1980-1987.

[10] M. Srinivas and L. M. Patnaik, "Genetic algorithms: a survey," *Computer,* vol. 27, pp. 17-26, 1994.

[11] M. A. Abido, "Multiobjective evolutionary algorithms for electric power dispatch problem," *IEEE Transactions on Evolutionary Computation,* vol. 10, pp. 315-329, 2006.

[12] Y. Li, S.-M. Yu, and Y.-L. Li, "Electronic design automation using a unified optimization framework," *Mathematics and Computers in Simulation,* vol. 79, pp. 1137-1152, 2008.

[13] I.-H. Lo, H.-W. Cheng, Y. Li, P.-J. Lin, and C.-H. Shen, "A novel integrated amorphous silicon TFT gate driver circuit with optimized design for TFT-LCD display panel manufacturing," in: *2011 IEEE 3rd Asia Symposium on Quality Electronic Design* (*ASQED*), 2011, pp. 262-265.