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# Fabrication of High Electrical Performance NILC-TFTs Using FSG Buffer Layer

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Fluorinated-silicate-glass (FSG) was combined with Ni-metal-induced lateral crystallization (NILC) polycrystalline silicon thin-film transistors (poly-Si TFTs). It was found that the electrical performances were improved because the trap-state density was decreased by fluorine-ion passivation. Moreover, FSG-NILC-TFTs possess high immunity against the hot-carrier stress and, thereby, exhibit better reliability.

## Introduction

Polycrystalline silicon thin-film transistors (poly-Si TFTs) have been widely used in active matrix organic liquid crystal displays (AMOLCDs) because their higher carrier mobility and lower threshold voltage than conventional amorphous thin-film transistors (a-Si TFTs) (1). Ni-metal-induced lateral crystallization (NILC) is one of these effective methods that can reduce the crystallization temperature to fabricate poly-Si TFTs on inexpensive glass substrates (2-3). However, in NILC, the poly-Si grain boundaries would trap Ni and $NiSi_2$ precipitates which induce trap-state density increased, resulting in threshold voltage shifting and lower field-effect mobility (4-5). In this letter, fluorine-ion was introduced to buffer oxide layer, subsequently deposited a-Si film and transformed the buffer layer to fluorinated-silicate-glass (FSG) layer at 550$^{o}$C. Then the fluorine-ion would diffuse to the active layer and passivate the trap-state defect when NILC was carried out. The above phenomenon cause electrical characteristic enhancement (6-7). Moreover, the presence of Si-F bonds strengthens electrical endurance against hot-carrier impact.

## Experiment

First, a 500-nm-thick $SiO_2$ buffer layer was fabricated by thermal furnace. Then, the fluorine-ion was implanted into the buffer oxide layer to form FSG layer. The projection range of fluorine-ion was set at the middle of the FSG layer and the accelerating energy was 30 keV. The dosage of fluorine ions was $2\times10^{14}$ cm$^{-2}$. Next, a 100-nm-thick undoped amorphous silicon layer was deposited by low pressure chemical vapor deposition (LPCVD) system on the FSG layers. The photoresist was patterned to form desired Ni lines, and a 5-nm-thick Ni film was deposited on the a-Si, subsequently annealed at 530$^{o}$C for 48 h to form the NILC poly-Si film. To reduce Ni contamination, the unreacted Ni metal was removed by chemical etching. After the crystallization of the a-Si, the active regions were defined by RIE. The 100-nm-thcik TEOS oxide was deposited by plasma-enhanced CVD (PECVD) for gate oxide and 100-nm-thick poly-Si film was deposited by LPCVD for gate electrodes. $P^+$-ion was implanted at a dose of $5\times10^{15}$ cm$^{-2}$ to form the source/drain and gate after defining the gate pattern by RIE etching. The activation of the source/drain regions was realized by the thermal furnace under $N_2$

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ambient at 600°C for 24 h. For comparing the effect of fluorine-ion passivation, a typical NILC-TFT with $SiO_2$ buffer layer was also fabricated.

## Results and Discussions

Fig. 1 show the $I_D$–$V_G$ transfer characteristics of FSG-NILC-TFTs and typical NILC-TFTs. The measured and extracted key device parameters are summarized in Table I. The performance of FSG-NILC-TFTs was far superior to that of typical NILC-TFTs. This implied when NILC was carried out; the fluorine-ion would diffuse to the active layer from FSG buffer layer, terminate dangling bonds, and replace the weak Si-H bonds in the grain boundaries and $SiO_2$/poly-Si interface by forming stronger Si-F bonds (8-9). Fig. 2 show the secondary-ion mass spectroscopy (SIMS) analysis of FSG-NILC-TFTs of the fluorine, silicon, and oxygen atoms. It was found that the F-ion was piled up at the interface of FSG layer/poly-Si channel and poly-Si channel/gate oxide. The phenomenon indicated fluorine-ion effectively passivated the dangling bonds in the channel of FSG-NILC-TFTs, resulting in the trap-state density ($N_T$) was reduced and improved electrical properties (10). The trap state density, which could be extracted using Levinson and Proano's method (11-12), was reduced from $4.6\times10^{12}$ $cm^{-2}$ to $3.1\times10^{12}$ $cm^{-2}$, as show in Table I, leading to high field-effect mobility ($\mu_{FE}$), low threshold voltage ($V_{TH}$), low subthreshold slope (S.S.) and high ON/OFF-current ratio ($I_{ON}/I_{OFF}$) in FSG-NILC-TFTs.

## Conclusions

An investigation of the effects of fluorine-ion passivation using the FSG buffer layer on the improvement of the electrical characteristics and reliability of NILC poly-Si TFTs has led to the development of a simple, effective process for improving the TFT electrical properties. The FSG-NILC-TFTs can be improved not only the transfer characteristics but also the electrical reliabilities. This result can be attributed to the fluorine-ion passivation effects and the weaker Si-H bonds and Si-Si bonds were replaced by stronger Si-F bonds.

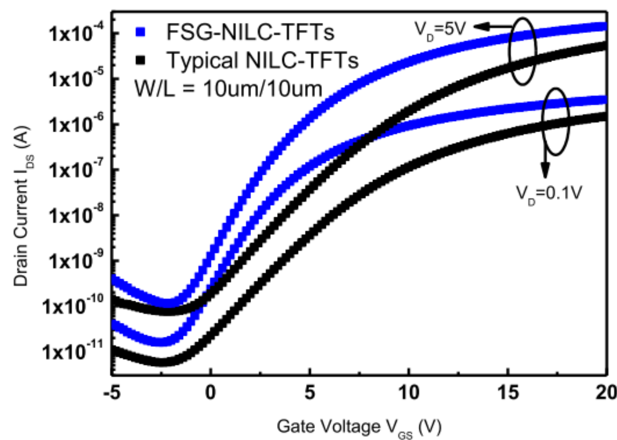


Fig. 1 Transfer characteristics of FSG-NILC-TFTs and typical NILC-TFTs



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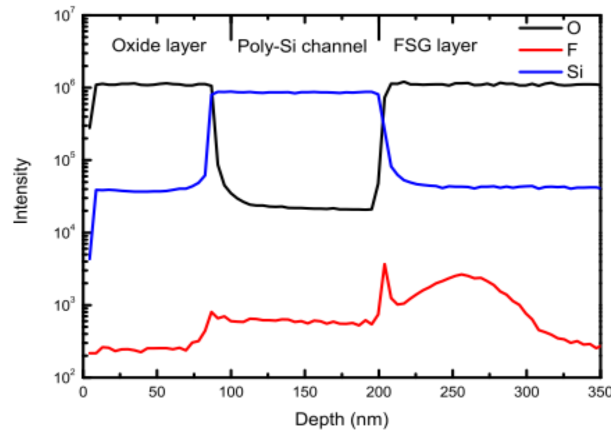


Fig. 2 The SIMS depth profile of FSG-NILC-TFTs of the fluorine, silicon, and oxygen atoms

**Table I.** Device characteristics of FSG-NILC-TFTs and Typical NILC-TFTs

| Device characteristics | FSG-NILC-TFTs | Typical NILC-TFTs |
|---|---|---|
| $N_T$ ($10^{12}$ $cm^{-2}$) | 3.1 | 4.6 |
| $\mu_{FE}$ ($cm^2$/ Vs) | 77.8 | 55.1 |
| $V_{TH}$ (V) | 3.1 | 6.1 |
| S.S. (V/dec) | 1.3 | 2.1 |
| $I_{ON}/I_{OFF}$ ($10^6$) | 2.2 | 0.5 |

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