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Improved Performance of MIC Poly-Si TFTs Using Driven-in Nickel Induced Crystallization (DIC) with Cap SiO_2 by F implantation

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A cap oxide layer was employed to substantially decrease nickel residues and passivate the trap states of the devices. F^+ implantation was used to drive Ni in α-Si layer to induce crystallization (DIC) process with cap oxide to reduce Ni concentration and minimize the trap-state density. As a result, DIC-TFT with cap oxide exhibit higher field-effect mobility, lower subthreshold slope, lower threshold voltage, higher on/off current ratio, and lower trap-state density (N_t) compared with conventional MIC TFTs.

Introduction

Low-temperature polycrystalline silicon thin-film transistors (LTPS-TFTs) have attracted considerable interest for their use in active-matrix liquid crystal displays (AMLCD). MIC is an effective method to obtain high-quality LTPS bellow 600°C. However, Ni and $NiSi_2$ precipitates were trapped in the poly-Si grain boundaries, which increase the leakage current and shift the threshold voltage (1, 2). Therefore, it is important to reduce Ni contamination to enhance the performance of the device. Furthermore, several studies have demonstrated the use of fluorine-ion implantation to improve the device performance because Si-F bond is stronger to show a better stability. Unfortunately, the leakage current, the most important character of MIC/MILC TFTs performance, was not decreased with the passivation process (3).

In this study, a cap oxide layer was employed to substantially decrease nickel residues and passivate the trap states of the devices. F^+ implantation was used to drive Ni in α-Si layer to induce crystallization (DIC) process with cap oxide to reduce Ni concentration and minimize the trap-state density.

Experimental

N-type self-alignment poly-Si TFTs were investigated in this study. A 100-nm-thick undoped α-Si layer was deposited onto a 500-nm-thick oxide-coated Si wafer by low pressure chemical vapor deposition (LPCVD) system. The 5-nm-thick cap oxide layer was formed by a simple chemical method (4). A 5-nm-thick Ni film was then deposited. Samples were subjected to F^+ implantation to drive Ni in the α-Si layer, as shown in Fig.1. The projection range was set at the 15 nm of depth near cap oxide/α-Si layer interface. The ion-accelerating energy and dosage was 13 KeV and 2×10^{15} cm^{-2}, respectively. To reduce the Ni contamination, the remained Ni film and cap oxide layer were then removed by wet etching, and subsequently annealed at 500°C for 1 h in N_2 to form poly-Si films. The islands of poly-Si regions were defined by Reactive ion etching (RIE). Next, a 100-nm-thick α-Si as a gate insulator was deposited by PECVD. Then a 100-nm-thick poly-Si film was deposited as the gate electrode by LPCVD. After defining the gate, self-aligned 30 keV phosphorous ions were implanted at a dose of 5×10^{15} cm^{-2} to form the

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source/drain and gate. Dopant activation was performed at 600°C in N_2 ambient for 12 h. It is worthy to note that this DIC process does not need any additional annealing step and is compatible with MIC processes.

RESULTS AND DISCUSSION

Fig. 2 shows the I_D–V_G transfer characteristics at a drain bias of 5 V for 10 × 10 μm^2 devices with and without FODIC treatment. The measured and extracted key device parameters are summarized in Table I. The threshold voltage (V_{th}) is defined at a normalized drain current of I_{DS} = (W/L) × 100nA at V_{DS} = 5V. The field-effect mobility (μ_{FE}) is extracted from the maximum value of transconductance at V_D = 0.1V. The electrical characters of DIC-TFTs with cap oxide are significantly improved, in particular the leakage current of 0.39 pA/μm and the on/off current ratio of 8.72 × 10^5. Compared with conventional MIC-TFTs, it shows 4.97-fold decreasing in the leakage current and 8.93-fold in the on/off current ratio. The leakage current improvement was attributed to lower nickel concentration in the DIC poly-Si films. In the poly-Si film, nickel residues serve as deep-level traps to dominate thermionic-emission leakage current in the low-gate and drain-voltage region (5, 6). From the SIMS data, cap oxide might reduce content of Ni into channel layer during driven-in process to conspicuously decrease leakage current. In addition, FODIC-TFT shows higher on-current than MIC-TFT. The trap state density (Nt) of MIC-TFT and FODIC-TFT was extracted using Levinson and Proano's method (7). It was found that MIC-TFT exhibits a Nt of 5.69 × 10^{12} cm^{-2}, whereas FODIC-TFT was 5.24 ×10^{12} cm^{-2}. The reduction in Nt values implies that those defects have been effectively terminated using F^+ implantation. Therefore, the carrier mobility increases due to decrease in the boundary scattering by passivation of grain boundaries defects.

Summary

The cap oxide between Ni and α-Si layer led to Ni content much lower than F^+ implant dosage, so that the Ni induced leakage current was decreased and F^+ passivation effect was increased. The electrical performance of FODIC-TFTs was improved substantially due to low content of nickel and passivation of fluorine-ion in the poly-Si films.

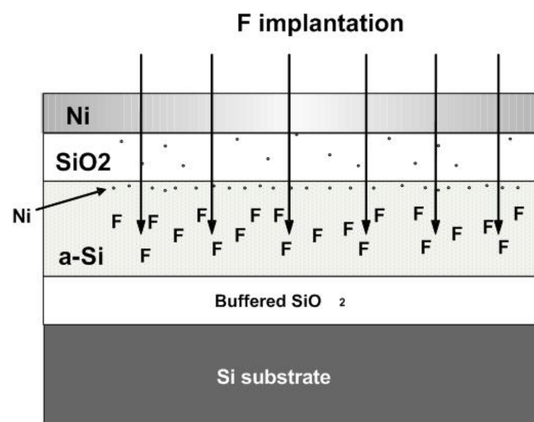

Fig. 1 The key process of poly-Si TFT device.

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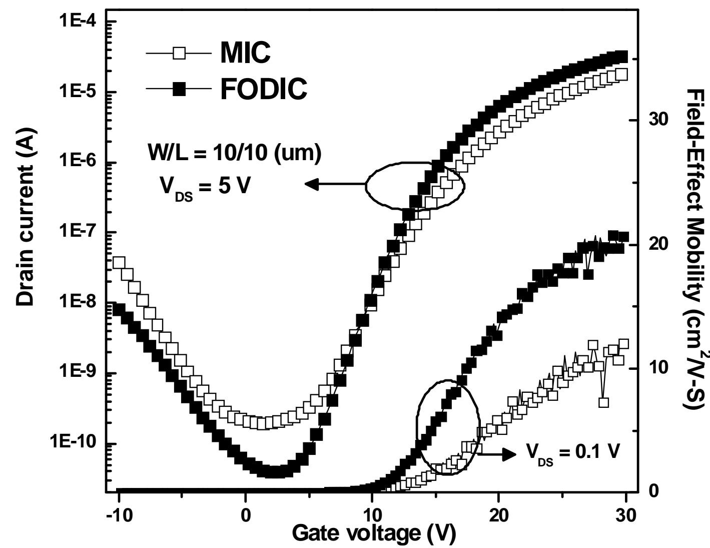

Fig. 2 Typical I_{DS}-V_{GS} transfer characteristics and filed-effect mobility.

TABLE I. Device characteristics of the MIC-TFTs and FODIC-TFTs

Device Parameters	MIC	FODIC
Field-Effect Mobility μFE (cm2 / V-s)	13.22	21.18
Threshold Voltage Vth (V)	12.96	12.10
Subthreshold Slope S.S (V / dec)	2.72	2.03
Imin (pA/μm)	1.94	0.39
Max on/off ratio (×10^5)	0.98	8.72

Acknowledgments

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