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Effect of Thermal Treatments on $HfO_2/In_{0.7}Ga_{0.3}As$ Metal-Oxide-Semiconductor Capacitor Characteristics

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Post deposition annealing is a critical process for the quality improvement of gate oxides on III-V MOS capacitors. Though high temperature annealing would effectively repair defects, it could also induce undesired electrical characteristics due to the crystallization of the gate oxide. In this work, we investigate the novel two steps annealing technique to improve the $HfO_2/In_{0.7}Ga_{0.3}As$ MOSCAP properties. The two steps process takes advantage of 1st high temperature annealing (550°C) to improve the interface quality and 2nd low temperature annealing (450°C) for curing bulk oxide without oxide crystallization. The two steps annealing technique greatly improves the $HfO_2/In_{0.7}Ga_{0.3}As$ properties as compared to single step process and is expected to be helpful for future III-V MOSFET development.

Introduction

The IC performance improves rapidly in the past decade due to the continuous scaling of metal–oxide–semiconductor field effect transistors (MOSFET). However, as channel lengths are down to the 22nm node, conventional Si-based technology comes to the serious scaling limits. The high mobility III-V channel materials have attracted much attention. Among the choices of several alternative channels, In-rich InGaAs exhibits superior characteristics of high electron mobility, high saturation drift velocity, and high transconductance when used as n-channel materials (1).The lack of native oxides for III-V channel materials is a limitation for III-V MOSFET development.

The introduction of deposited oxides as gate dielectrics would solve this problem. The integration of III-V compound semiconductors with high-k dielectrics is very important for further scale down the devices for high speed logic applications. Previous study has focused on deposited SiO_2 gate oxides (2). However, SiO_2 would induce serious gate leakage and high bulk charge densities. Recently, several high-k materials had been studied as gate dielectrics for III-V devices, such as Al_2O_3, HfO_2, and Gd_2O_3 et al (3-4). The $In_{0.7}Ga_{0.3}As$ MOSFET devices with Al_2O_3 and HfO_2 as a gate dielectric had been proposed (5-6). Among theses high-k dielectrics, HfO_2 is very promising for deep

submicron MOSFET devices because of its high dielectric constant which is 4-5 times than SiO_2 and sufficient high bandgap (7). The post deposition annealing (PDA) is a critical process for quality improvement of gate dielectrics in III-V MOSFET. There are still very few studies regarding to this issue. In this study, the novel thermal treatment of "two steps annealing" on the electrical behaviors of the $HfO_2/In_{0.7}Ga_{0.3}As$ MOS capacitors are investigated.

Experiments

In the one step annealing, the HfO_2 dielectric was deposited by MBE method on the P^+ $In_{0.7}Ga_{0.3}As/P^+$ $In_{0.53}Ga_{0.47}As/InP$ epilayer structure followed by 400~550^{0}C RTA annealing. The "two steps annealing" was performed by 1st annealing of the thin 5nm deposited HfO_2 layer at 550^{0}C and followed by the 2nd lower temperature annealing at 450^{0}C after another 10nm HfO_2 was deposited. After the 2nd annealing, the W electrode was deposited on the top of the dielectric and Au ohmic was deposited on the back of the substrate. The device structures and process sequences of the one step and two steps annealings are shown in Fig. 1(a) and (b).

Results and Discussion

The temperature of post dielectric deposition annealing is critical for the improvement of the gate dielectric quality. We investigated PDA temperature ranging from 400~550^{0}C for $HfO_2/ In_{0.53}Ga_{0.47}As$ capacitors. The accumulation capacitances measured at -2.5V, 100 kHz and the interface trap density (D_{it}) versus RTA temperatures for one step annealing samples are shown in Fig 2. The accumulation capacitance increased and the interface states decreased with increased RTA temperature. The inset shows the 100 kHz C-V curves for samples with several different RTA temperatures (400~550^{0}C). The high frequency C-V curves with high annealing temperature exhibit strong inversion. The results indicate that the high temperature annealing could effectively reduce the interface states densities (D_{it}) and enhance gate capacitances.

However, the high temperature could induce additional gate leakage paths, hysteresis and bulk oxide traps due to the crystallization of the gate oxide. In Fig. 3, the gate leakage current and the C-V hysteresis of the one step annealing samples are studied. The high annealing temperature of 550^{0}C shows high gate leakage current and large C-V hysteresis. It indicates that the extremely high annealing temperature could cause bulk dielectric trap formation though the interface states are significantly improved. Therefore, we adopted the two steps annealing process for $HfO_2/ In_{0.53}Ga_{0.47}As$ capacitors to take advantages of high temperature annealing for interface states reduction and low temperature annealing to prevent the additional bulk dielectric trap formation.

The two steps annealing was demonstrated by initial deposition of the 1st thin 5nm HfO_2 layer which is annealed at 550^{0}C and sequentially deposition of the 2nd 10nm HfO_2

which is annealed at lower temperature (450^{0}C). In Fig. 4, the C-V characteristic of the 2 steps annealing sample show greatly improvement compared to the one step annealing sample. The 2 steps annealing sample exhibits improved C-V inversion hysteresis, gate capacitance, and gate leakage current behavior. The improvement is believed to be due to the remove of the interface traps due to the 1st high temperature annealing and the improvement of the crystal quality without further crystallization. Since further crystallization will provide more paths for leakage current.

Conclusion

We have studied the two steps annealing effect on the $In_{0.7}G_{a0.3}As$ MOS capacitor with high-k HfO_2 dielectric. The HfO_2/ $In_{0.7}G_{a0.3}As$ MOS capacitor exhibits improved performances over conventional one step annealing samples with better C-V characteristics and lower gate leakage current.

Acknowledgments

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Figures

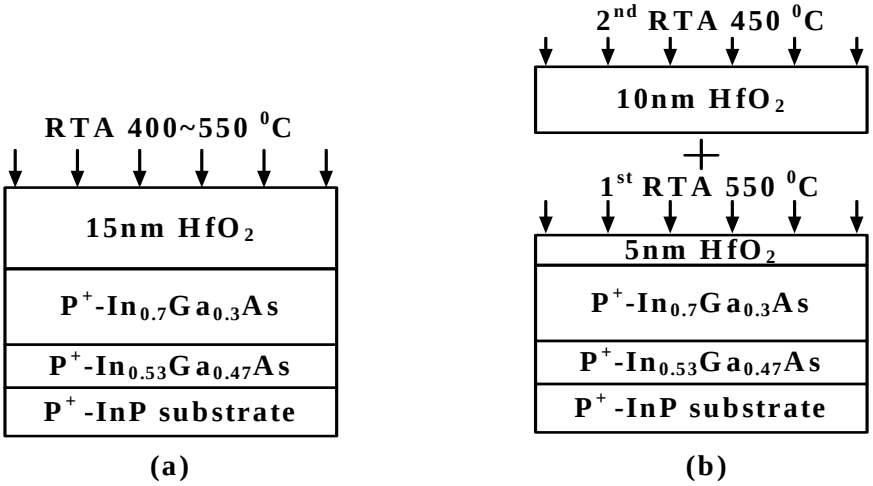

Figure 1. The device structures and processes of HfO_2/ $In_{0.7}Ga_{0.3}As$ capacitors with (a) one step annealing and (b) two steps annealing.

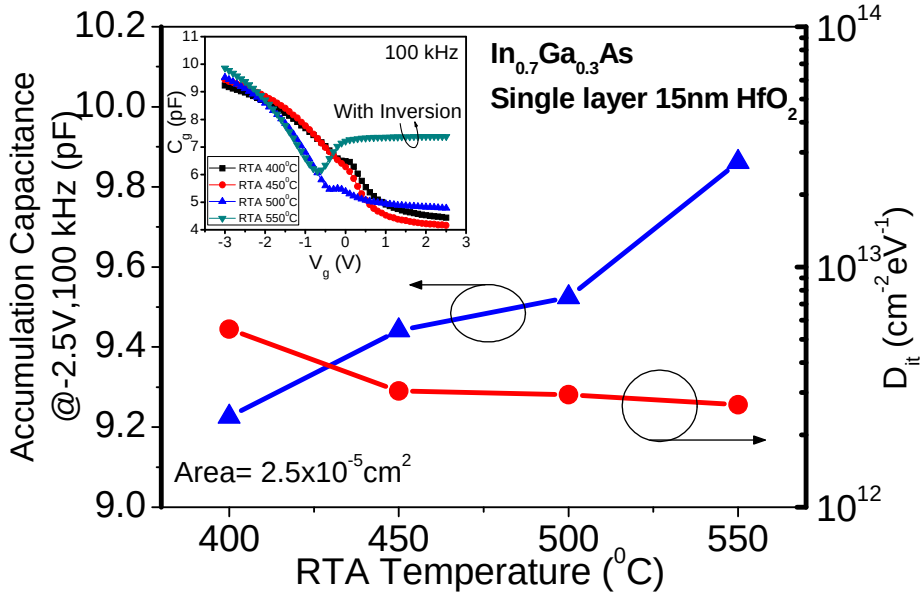

Figure 2. The accumulation capacitances and D_{it} in relation with RTA temperature for one step annealing samples. The inset shows the 100 kHz C-V curves for samples with several different RTA temperatures (400~550□).

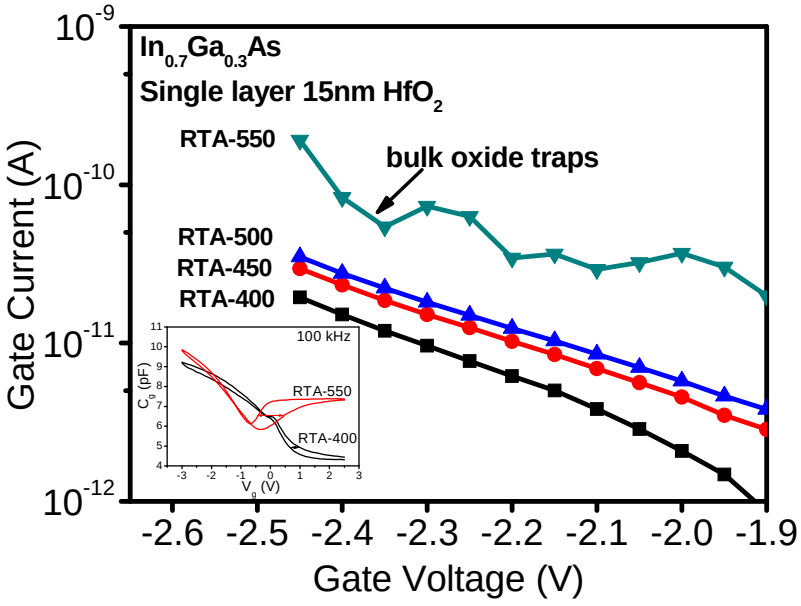

Figure 3. The gate leakage currents of one step annealing samples. The inset shows the hysteresis C-V curves.

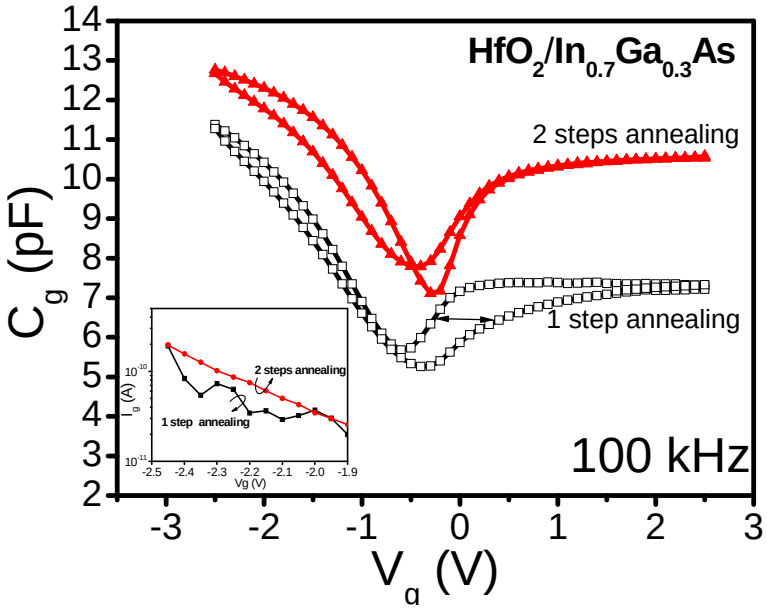

Figure 4. The hysteresis C-V curves of one and two steps annealing samples. The inset shows the gate leakage currents of one and two steps annealing samples.