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Interface Morphology Investigation of Bonded p-GaAs/p-Si Wafers

Cheng-Yu Hsieh and YewChung Sermon Wu

Department of Materials Science and Engineering, National Chiao Tung University,
Hsinchu, Taiwan, R.O.C

The integration of GaAs and Si can combine the superior electrical and optical properties of GaAs with the mechanical and economical advantages of Si. It presents great potential for OEICs applications. In this study, direct wafer bonding was applied to combine bulk p-Si and p-GaAs. Interface morphologies of bonded p-GaAs/p-Si wafers were investigated by TEM.

INTRODUCTION

Fabrication of III-V materials on Si substrate is a promising approach to device design. Si can offer many advantages such as the low cost, high mechanical strength, and advanced VLSI technology. Using Si as substrate to replace expensive III-V substrates will bring several economical advantages and it can be done by applying Smart Cut™ technology to transfer thin III-V layer onto Si (1). Base on this technology, the novel III-V/SOI structure was used to promote the performance of MOSFET (2) and it did enhance the electrical properties of device. Although Si has been widely used, the application for optical use was limited due to its indirect band gap. The combination of direct band gap materials and silicon can introduce established Si system into OEIC and make device designing free (3). These purposes can be done by growing heteroepitaxially layers on silicon, but the lattice and thermal expansion coefficient mismatch lead to defect formation that will decrease device performance. Using wafer bonding technology to fabrication III-V materials on Si can restrict defects to interface and reduce the negative effect by these defects. However, bonding process is usually accompanied by high annealing temperature and lead to lots of problems, such as interdiffusion and thermal stress. In this paper, the effect of bonding conditions on the bonded p-GaAs/p-Si was investigated.

EXPERIMENTAL

In this study, B doped (001) p-Si and Zn doped (001) p-GaAs wafers were used. All samples were diced to 10x10mm^2 pieces. The thickness of GaAs wafer was 500µm, while that of Si wafer was 300µm. To reduce the thermal stress caused by the thermal expansion mismatch, 300x300µm^2 and 150-µm-depth mesa structure was applied on Si wafer (4). Both wafers were degreased in acetone and IPA. After N_2 dry, the wafers were immersed in H_2SO_4:H_2O_2:H_2O solution .For hydrophobic bonding, both Si and GaAs were dipped in 10% HF solution for 30s. Cleaned wafers were brought into contact and pressed against each other in a fixture composed of Mo and stainless steel (5). Then, the fixture was loaded into a furnace and annealed at different temperature (500 to 900 °C) for 2 hours in Ar ambient. The TEM samples were prepared by grinding and Focus Ion Beam (FIB).

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RESULTS AND DISCUSSION

Three sets of sample have been successfully bonded. The microstructures of bonding interfaces were investigated by TEM, as showed in Figure 1. The amorphous layer was confirmed to be silicon oxide rich phase by EDX. The thickness of amorphous layer increased dramatically from 600°C to 800°C and decreased from 800°C to 900°C. The oxygen content in this layer was found higher in sample annealed at 800°C than others.

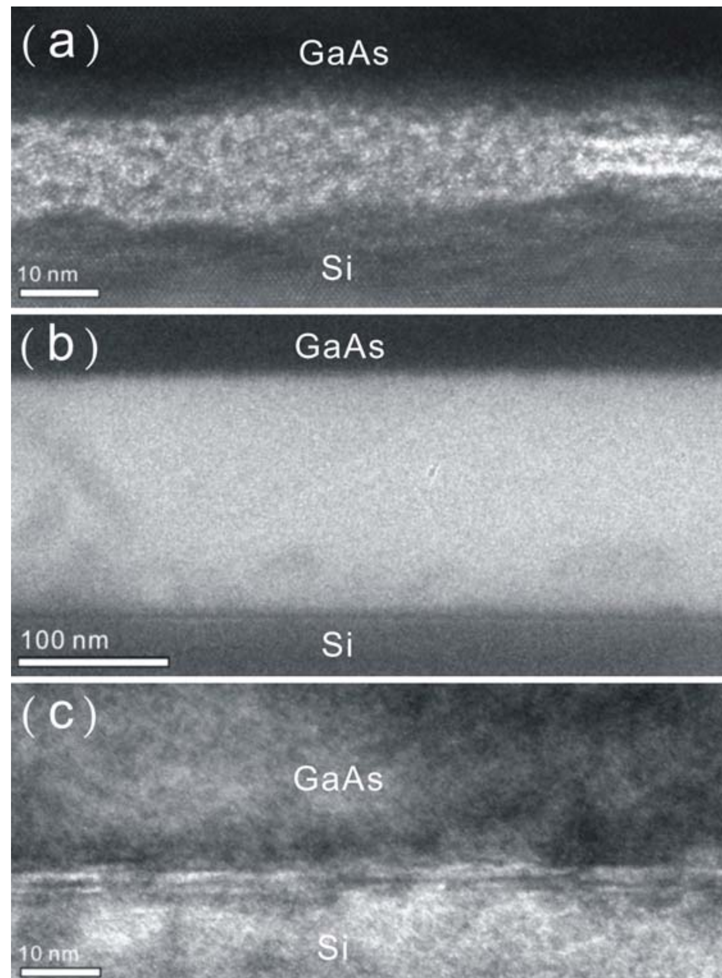

Figure. 1 Cross-sectional TEM images of Si/GaAs interface bonded at (a)500 (b)800 (c)900

When bonded at 500°C, a thin oxide layer was presented at the interface. This is because it is hard to remove native oxide from sample surface. It suggests that wafer pairs are bonded by native oxide not by GaAs/Si chemical bond.

When bonded at 800°C, the oxide thickness increased to 200nm. This result is different from experience of GaAs/GaAs bonding case (6), in which the thickness of oxide layer decreased due to the diffusion of oxygen into GaAs matrix. EDX analysis (Fig. 2) revealed that most content of this bonded interfacial amorphous layer is oxygen. It suggests there are other sources of oxygen diffusing into the bonded interface. The

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increase of amorphous layer might have resulted from the out-diffused oxygen from CZ grown Si wafer.

When bonding temperature reached 900°C, the oxide layer diminished and performed perfect bonding in most area. Only discontinuous oxide exist at interface was observed in this sample. The diffusion of oxygen from silicon was retarded by self-interstitial silicon (7) near interface and high oxygen diffusion rate in GaAs matrix.

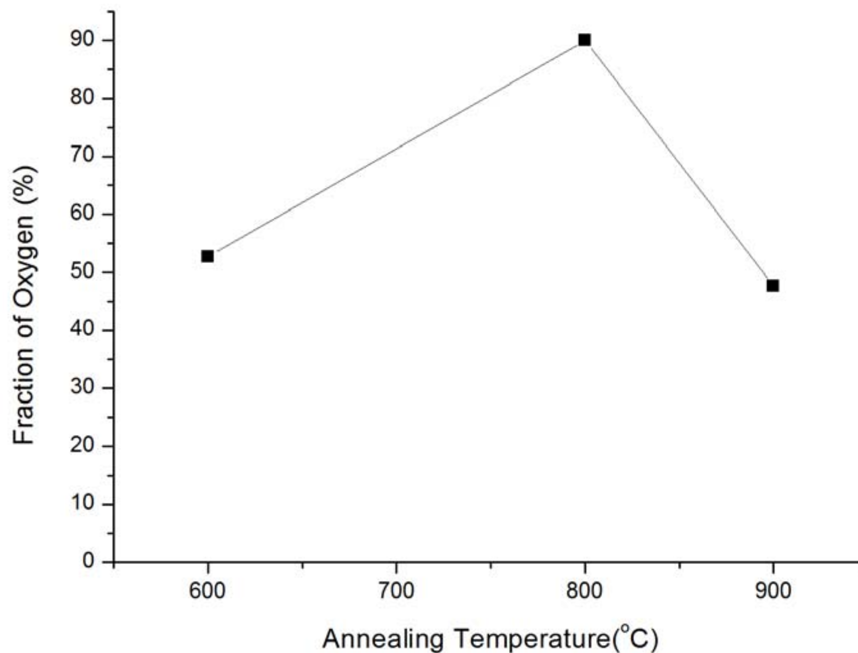

Fig. 2 Fraction of Oxygen in amorphous layer

Conclusion

p-GaAs and p-Si wafers was successfully bonded at temperature ranging from 500 to 900°C. The bonding mechanism and bonded interfaces were investigated. The interfacial amorphous oxide layer was increased when bonding temperature was increased from 500 to 800ºC. This might be the result of the out-diffused oxygen from CZ grown Si wafer. When bonding temperature reached 900°C, the oxide layer diminished. This is because the oxygen diffusion in silicon was retarded by self-interstitial silicon near interface and high oxygen diffusion rate in GaAs matrix.

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