Characteristic of p-Type Junctionless Gate-All-Around Nanowire Transistor and Sensitivity Analysis

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***Abstract*—The characteristics and sensitivities of p-type junctionless (JL) gate-all-around (GAA) (JLGAA) nanowire transistors are demonstrated by simulating a 3-D quantum transport device with a view to their use in CMOS technology. The concentration of dopants in a p-type JL nanowire transistor is not as high as that in an n-type device owing to solid solubility of boron in silicon. However, we can use a midgap material as gate electrode to design an appropriate device threshold voltage. The p-type JLGAA transistor exhibits a favorable on/off current ratio and better short-channel characteristics than a conventional inversion-mode transistor with a GAA structure. Sensitivity analyses reveal that the channel thickness and random dopant fluctuation substantially affect the device performance in terms of threshold voltage ($V_{\rm th}$), on current ($I_{\rm on}$), and subthreshold slope because of the full depletion condition of the channel. The channel length and oxide thickness have less impact because the short-channel effect is well controlled.**

***Index Terms*—Gate-all-around (GAA), junctionless (JL), nanowire transistor, sensitivity.**

I. Introduction

GATE-all-around (GAA) silicon nanowires are promising candidates for use in next-generation high-speed and low-power electronic devices owing to their excellent gate controllability, low leakage, and good carrier transport properties [1]–[3]. Recently, the concept of the junctionless (JL) MOS device, which contains a single doping species at the same level in its source, drain, and channel, has been proposed and investigated [1]–[6]. GAA architecture is extremely suitable for fabricating JL devices as the gate creates a depletion region at all sides of the device to turn off the device. However, the high surface-to-volume ratio in nanowires improves its sensitivity to any change in process [1]–[3], [7], [8]. Since the variability issue was more pronounced in nanometer CMOS devices [7]–[10], variations in process change should be considered carefully. Additionally, many studies have focused on the scaling of n-type devices [2]–[6], [11], [12], but few have addressed the use of p-type JL transistor for CMOS technology.

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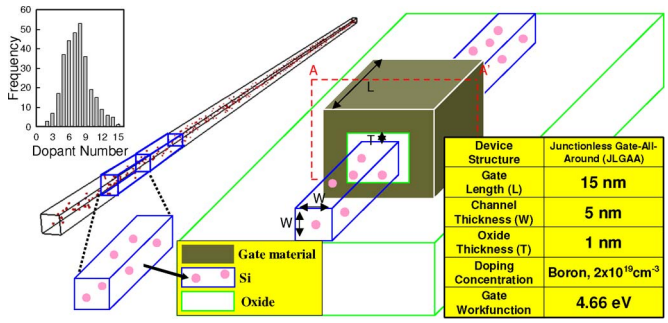

Fig. 1. Device structure and parameters of simulated JLGAA nanowire transistor.

This letter studies the characteristics and sensitivities of a p-type JL GAA (JLGAA) nanowire transistor by simulating a 3-D quantum transport device with a view to the integration of such transistors in CMOS technology. This letter is organized as follows. In Section II, the simulation technique for studying the JLGAA transistor is introduced. In Section III, the performance of the device is discussed. In Section IV, an analysis of sensitivity to the source of variation is presented. Finally, conclusions are drawn.

II. Simulation Methodology

Fig. 1 shows the structure of the p-type JLGAA nanowire device and the parameters that are used in this work. In the standard device architecture used in this study, the gate/source/drain lengths are all 15 nm, the equivalent oxide thickness is 1 nm, and the channel has a square cross section with a width of 5 nm. Owing to the solid solubility of boron in silicon, the doping concentrations of the channel and the source/drain are all 2×10^{19} cm^{-3} with continuous doping concentration, which is lower than that of an n-type device [2]–[6]. The gate work function is 4.66 eV for an appropriate threshold voltage, which can be easily obtained by using a midgap metal material, such as TiN. To obtain accurate numerical results for a nanoscale device, the device is simulated by solving 3-D quantum transport equations using the commercial tool Synopsys SDevice [13]. For considering random dopant fluctuation (RDF) in sensitivity analysis, dopants are randomly generated following a Poisson distribution in a very long cuboid, which

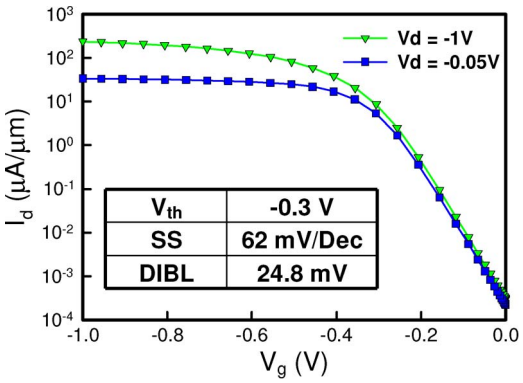

Fig. 2. I_d–V_g curves of the p-type JLGAA nanowire transistor; the threshold voltage ($V_{\rm th}$), SS, and DIBL are shown in the inset.

the equivalent doping concentration is 2×10^{19} cm^{-3}. The long cuboid is then partitioned into 300 subcuboids. The number of dopants in each cuboid varies from 1 to 15, and the average number is eight. These subcuboids are mapped into the device Si region (including channel, source, and drain) for 3-D device simulation with discrete dopants [7], [8], [13]. In quantum transport equations, a density gradient model [14] is used, as listed hereinafter

$$p = N_V F_{1/2}\left(\frac{E_{F,p} - E_V - \Lambda_p}{kT_p}\right)$$
$$\Lambda_p = -\frac{\gamma\hbar^2}{12m_p}\left[\nabla^2 \ln p + \frac{1}{2}(\nabla \ln p)^2\right] \quad (1)$$

where p is the hole concentration, N_v is the effective density of states of valence band (E_v), $F_{1/2}$ is the Fermi–Dirac integral, m_p is the effective mass of hole, and T_p is the hole temperature. The corresponding parameters are also used for electrons. The mobility model used in the device simulation is according to Mathiessen's rule, expressed as

$$\frac{1}{\mu} = \frac{D}{\mu_{\rm surf\_aps}} + \frac{D}{\mu_{\rm surf\_rs}} + \frac{1}{\mu_{\rm bulk\_dop}} \quad (2)$$

where $D = \exp(x/l_{\rm crit})$, with x as the distance from the interface and $l_{\rm crit}$ as a fitting parameter. The mobility consists of three parts: surface acoustic phonon scattering ($\mu_{\rm surf\_aps}$), surface roughness scattering ($\mu_{\rm surf\_rs}$), and bulk mobility with doping-dependent modification ($\mu_{\rm bulk\_dop}$); the details are described in [13] and [15]. The SRH recombination and band-to-band tunneling are also considered in the simulation. However, due to the JL devices using high-concentration p-type doping in the channel, the band bending in vertical direction is much smaller compared to the inversion-mode PMOS with n-type channel doping. Therefore, the gate-induced drain leakage effect is not significant in JL devices.

III. Characteristics of Device

Fig. 2 shows the I_d–V_g curves of the standard p-type JLGAA device of interest: The threshold voltage ($V_{\rm th}$) is approximately -300 mV, and the on current ($I_{\rm on}$) and off current ($I_{\rm off}$) are 238 μA/μm and 0.3 nA/μm, respectively, without the use of any channel engineering or strain technology. A subthreshold slope (SS) of 62 mV/dec approaches the ideal value, and drain-induced barrier lowering (DIBL), defined as the difference in $V_{\rm th}$ between $V_d = -0.05$ V and $V_d = -1$ V, equals only 24.8 mV. The results of the simulation indicate that JLGAA devices have excellent short-channel characteristics for device scaling because their channels have a high doping concentration and a small depletion region. Fig. 3 shows the hole density (top) and electric field (bottom) distributions in the middle of the channel when the devices are operated in the OFF ($V_g = 0$ V) and ON ($V_g = -1$ V) states. The positions of A and A' are shown in Fig. 1; the electric field in the oxide region is not shown. The holes are concentrated in the middle of the channel region when the device is either off or on, because they are repelled by the electric field at the channel/oxide interface [2]–[4]. When the device is in the OFF state, the GAA structure and the narrowness of the channel cause the channel region to be almost completely depleted, creating a relatively uniform electric field, and the bulk conduction of holes is reduced. However, when the device is operated in the ON state, the electric field is reduced in the middle of the channel and increased close to the surface of the channel, promoting the conduction of the holes. Accordingly, the JL transistor has a high on/off current ratio.

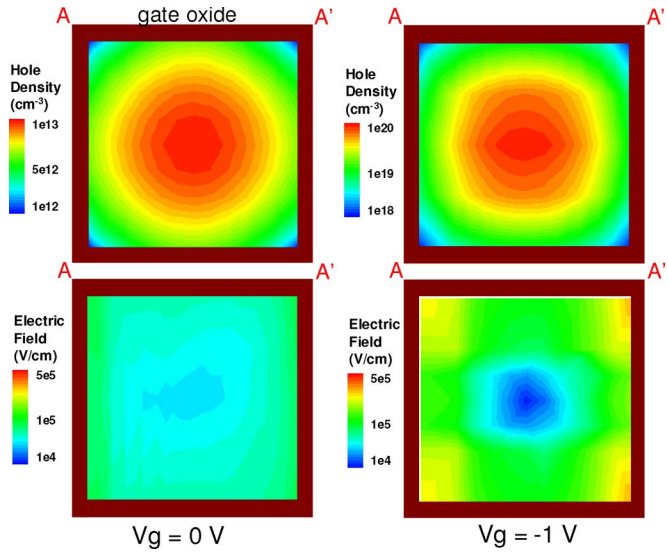

Fig. 3. (Top) Hole density and (bottom) electric field distributions in the channel at the device OFF ($V_g = 0$ V) and ON states ($V_g = -1$ V). The positions of A and A' in the figure are shown in Fig. 1.

IV. Sensitivities of Device

Fig. 4 shows the sensitivities of the devices to changes of $\pm 10\%$ and $\pm 20\%$ in gate length (L), oxide thickness (T), and channel thickness (W) and with RDF. The $\Delta V_{\rm th}/V_{\rm th}$, $\Delta I_{\rm on}/I_{\rm on}$, and ΔSS/SS summarized in Table I are defined as the difference between the respective maximum and minimum values divided by the performance of the standard JLGAA transistor with no variation in L, T, W, and RDF. In Fig. 4(a), a change in L only slightly affects $\Delta V_{\rm th}/V_{\rm th}$, $\Delta I_{\rm on}/I_{\rm on}$, and ΔSS/SS, indicating excellent control of the short-channel effect because of the GAA structure. In Fig. 4(b), changing the

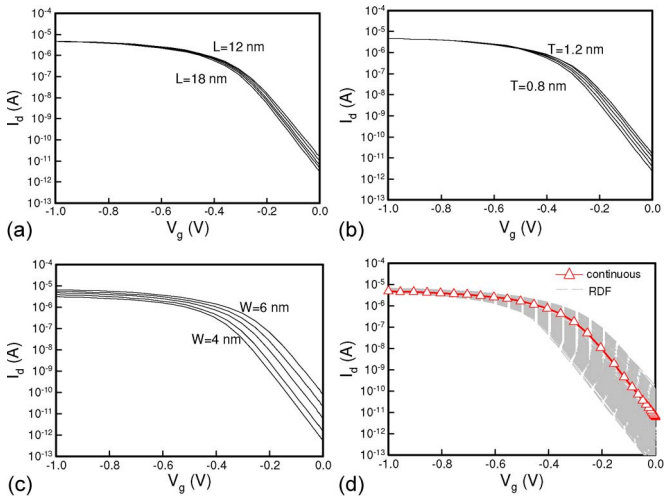

Fig. 4. Sensitivity analyses for (a) gate length L, (b) oxide thickness T, and (c) channel thickness W changes of $\pm 10\%$ and $\pm 20\%$ and (d) considering RDF.

TABLE I
SUMMARY OF THE DEVICE PERFORMANCE DEVIATIONS FOR DIFFERENT SOURCE OF DEVIATIONS

p-type JL GAA	Gate Length (L)	Oxide Thickness (T)	Channel Thickness (W)	Random Dopant Fluctuation
$\Delta V_{th}/V_{th}$	10.5%	16.3%	45.3%	71%
$\Delta I_{on}/I_{on}$	3.6%	1.5%	77.1%	22%
$\Delta SS/SS$	4.6%	7.3%	11.8%	15.1%

oxide thickness has a greater effect on $V_{\rm th}$ but a weaker effect on the device $I_{\rm on}$ than does changing L; it also shows less impact on the device performance. Since the depletion region of the channel dominates the characteristics of a JL device [4], the $I_{\rm on}$ is observed to be highly sensitive to W because of the full depletion condition of the channel. The $\Delta V_{\rm th}/V_{\rm th}$, $\Delta I_{\rm on}/I_{\rm on}$, and ΔSS/SS of such a transistor are 45%, 77%, and 12%, respectively. Fig. 4(d) shows the IV characteristics with RDF, in which the red symboled line is the standard device with continuous doping concentration. The RDF significantly affects the device $V_{\rm th}$ and SS more than other systematic process variations. However, for device operation at high gate bias, the high concentration of carriers screens the influence of impurities, resulting in a smaller deviation of $I_{\rm on}$.

V. CONCLUSION

In this letter, the characteristics and sensitivities of p-type JL-GAA nanowire transistors have been explored for potential use in nano-CMOS technology. The simulation results demonstrate that p-type JLGAA transistors can be fabricated from a midgap gate material and have a high on/off current ratio and excellent short-channel characteristics. The electric field distribution when the device is on differs considerably from that when the device is off, explaining the excellent switching current ratio. In systematic process variation, since the depletion region of the channel of a JL device is important, the channel thickness significantly influences the device performance. The RDF has the greatest effect on the threshold voltage and subthreshold slope but a limited influence on ON-state current. This is due to the screening effect of carriers at high gate voltage bias.

REFERENCES

[1] P. Singh, N. Singh, J. Miao, W.-T. Park, and D.-L. Kwong, "Gate-all-around junctionless nanowire MOSFET with improved low-frequency noise behavior," *IEEE Electron Device Lett.*, vol. 32, no. 12, pp. 1752–1754, Dec. 2011.

[2] N. D. Akhavan, I. Ferain, P. Razavi, R. Yu, and J.-P. Colinge, "Improvement of carrier ballisticity in junctionless nanowire transistors," *Appl. Phys. Lett.*, vol. 98, no. 10, pp. 103 510-1–103 510-3, Mar. 2011.

[3] C.-W. Lee, I. Ferain, A. Afzalian, R. Yan, N. D. Akhavan, P. Razavi, and J.-P. Colinge, "Performance estimation of junctionless multigate transistors," *Solid State Electron.*, vol. 54, no. 2, pp. 97–103, Feb. 2010.

[4] J. P. Colinge, C.-W. Lee, I. Ferain, N. D. Akhavan, R. Yan, R. Razavi, R. Yu, A. N. Nazarov, and R. T. Doria, "Reduced electric field in junctionless transistors," *Appl. Phys. Lett.*, vol. 96, no. 7, pp. 073510-1–073510-3, Feb. 2010.

[5] C.-Y. Pai, J.-T. Lin, S.-W. Wang, C.-H. Lin, Y.-S. Kuo, Y.-C. Eng, P.-H. Lin, Y.-H. Fan, C.-H. Tai, H.-H. Chen, C.-H. Chen, and K.-Y. Lu, "Numerical study of performance comparison between junction and junctionless thin-film transistors," in *Proc. IEEE Int. Conf. Solid-State Integr. Circuit Technol.*, 2010, pp. 1410–1412.

[6] R. Rios, A. Cappellani, M. Armstrong, A. Budrevich, H. Gomez, R. Pai, N. Rahhal-orabi, and K. Kuhn, "Comparison of junctionless and conventional trigate transistors with L_g down to 26 nm," *IEEE Electron Device Lett.*, vol. 32, no. 9, pp. 1170–1172, Sep. 2011.

[7] Y. Li, C.-H. Hwang, T.-Y. Li, and M.-H. Han, "Process variation effect, metal-gate work-function and random-dopant fluctuations in emerging CMOS technologies," *IEEE Trans. Electron Devices*, vol. 57, no. 2, pp. 437–447, Feb. 2010.

[8] Y. Li, S.-M. Yu, J.-R. Hwang, and F.-L. Yang, "Discrete dopant fluctuations in 20-nm/15-nm-gate planar CMOS," *IEEE Trans. Electron Devices*, vol. 55, no. 6, pp. 1449–1455, Jun. 2008.

[9] C. L. Alexander, G. Roy, and A. Asenov, "Random impurity scattering induced variability in conventional nano-scaled MOSFETs: *Ab initio* impurity scattering Monte Carlo simulation study," in *Proc. Int. Electron Devices Meeting*, 2006, pp. 1–4.

[10] M. Aldegunde, A. Martinez, and J. R. Barker, "Study of discrete doping-induced variability in junctionless nanowire MOSFETs using dissipative quantum transport simulations," *IEEE Electron Device Lett.*, vol. 33, no. 2, pp. 194–196, Feb. 2012.

[11] H.-C. Lin, C.-I. Lin, and T.-Y. Huang, "Characteristics of n-type junctionless poly-Si thin-film transistors with an ultrathin channel," *IEEE Electron Device Lett.*, vol. 33, no. 1, pp. 53–55, Jan. 2012.

[12] S. Gundapaneni, S. Ganguly, and A. Kottantharayil, "Bulk Planar Junctionless Transistor (BPJLT): An attractive device alternative for scaling," *IEEE Electron Device Lett.*, vol. 32, no. 3, pp. 261–263, Mar. 2011.

[13] *User's Manual for Synopsys Sentaurus Device*, Synopsys, Inc., Mountain View, CA, 2007.

[14] M. G. Ancona and G. J. Iafrate, "Quantum correction to the equation of state of an electron gas in a semiconductor," *Phys. Rev. B, Condens. Matter*, vol. 39, no. 13, pp. 9536–9540, May 1989.

[15] S. Reggiani, M. Valdinoci, L. Colalongo, M. Rudan, G. Baccarani, A. D. Stricker, F. Illien, N. Felber, W. Fichtner, and L. Zullino, "Electron and hole mobility in silicon at large operating temperatures—Part I: Bulk mobility," *IEEE Trans. Electron Devices*, vol. 49, no. 3, pp. 490–499, Mar. 2002.