Metal-Gate/High-κ/Ge nMOS at Small CET With Higher Mobility Than SiO_2/Si at Wide Range Carrier Densities

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***Abstract*—High-performance TaN/TiLaO/La_2O_3/SiO_2/(111)-Ge nMOSFETs show high mobility of 432 $cm^2/V \cdot s$ at 10^{13} cm^{-2} carrier density (N_s), good 1.05 junction ideality factor, and small subthreshold swing of 101 mV/dec, at a small 1.1-nm capacitance-equivalent thickness (CET). This is the first report of higher mobility in the Ge nMOSFET than SiO_2/Si universal mobility at wide medium–high N_s range and small CET of 1.1 nm, which is attributed to using the (111)-Ge substrate, 30-ns laser annealing, SiO_2 interfacial layer, and $YbGe_x$/n-Ge contact.**

***Index Terms*—Annealing, Ge, high-κ, laser, YbGe, (111).**

I. Introduction

Low power operation at < 0.5-V drain voltage (V_D) is the most important criterion for advanced IC. To reach this goal, high-mobility new-channel CMOS and small source–drain contact resistance are needed for highly scaled < 10 nm CMOS. Thus, high-mobility InGaAs-nMOS/Ge-pMOS was proposed, but the epitaxial InGaAs on Si is still a challenge due to the lattice mismatch and antiphase boundaries. Alternatively, Ge has both higher bulk electron and hole mobility than Si for new-channel CMOS [1]–[17]. The integration of Ge on Si can be realized by using a Ge-on-insulator (GOI or GeOI) structure [1], where defect-free Ge was realized. This GeOI structure can also suppress the leakage current of small energy band-gap Ge and useful for device-level 3-D IC [5]. The all-Ge CMOS offers major merits of simpler process, lower cost, and potentially higher yield, but the Ge nMOSFET suffers from Fermi-level pinning, poorer source–drain contact, and faster mobility rolloff than universal SiO_2/Si data. The mechanism of fast mobility degradation is still unclear, although high peak mobility was reported for the GeO_2/Ge nMOSFET [14].

It was reported that the electron and hole mobility can be improved in (111) [14] and (110) [5] oriented Ge substrate. Here, we report higher mobility of Ge nMOSFET than SiO_2/Si data over wide medium–high carrier density (N_s) range and a small 1.1-nm capacitance-equivalent thickness (CET). Good device characteristics of better ideality factor and subthreshold swing (SS) were achieved, which is attributed to the (111)-Ge [14], 30-ns laser annealing (LA) [7], [16]–[20], SiO_2 interfacial layer to prevent electron wave-function penetration, and $YbGe_x$ contact.

Manuscript received November 2, 2012; revised November 16, 2012; accepted November 19, 2012. Date of publication January 4, 2013; date of current version January 23, 2013. This work was supported by the National Science Council of Taiwan. The review of this letter was arranged by Editor J. Schmitz.

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Digital Object Identifier 10.1109/LED.2012.2230241

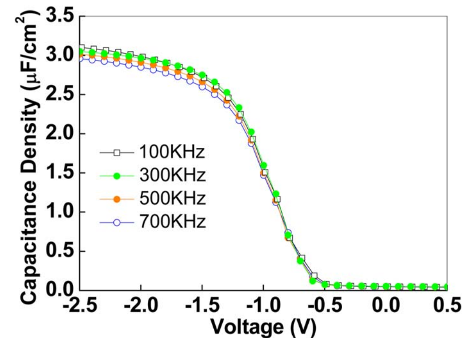

Fig. 1. $C-V$ characteristics of TaN/TiLaO/La_2O_3/SiO_2/(111)-Ge nMOS capacitors after LA.

II. Experiment Procedure

Standard 2-in p-type (111)-oriented Ge wafers with 10-$\Omega \cdot$cm resistivity were used in this study. In contrast to a previous *gate-last* process [16], the Ge nMOSFET was fabricated by a *gate-first* process. After cleaning, the samples were immersed into diluted HF $(1:10)$ to remove the native oxide, dipped in deionized water, dried and loaded immediately into a deposition chamber. Then, ultrathin 0.7-nm SiO_2, 1-nm high-κ La_2O_3, and 4-nm high-κ TiLaO were deposited by physical vapor deposition [16], followed by O_2 postdeposition anneal (PDA) at 400 °C for 5 min and the first KrF LA. The LaTiO was deposited by mixed $La_2O_3 : TiO_2 = 1:1$, where a high κ of 58 was obtained in TiO_2 from a thick layer [21]. The LA has a short $\sim$30-ns pulsewidth at a 248-nm wavelength. After that, the TaN gate was formed and self-aligned P was implanted at 35 keV and 5×10^{15} cm^{-2}, and the second KrF LA was applied for source–drain activation [16]. Finally, 30-nm Yb covered by SiO_2 was deposited to the source–drain and annealed at 500 °C to form the Ge nMOSFET. All the devices were measured at room temperature.

III. Result and Discussion

Fig. 1 shows the $C-V$ characteristics of TaN/TiLaO/La_2O_3/SiO_2/(111)-Ge nMOS capacitors formed by PDA and LA. A CET of 1.1 nm is obtained, which is one of the lowest CET for Ge nMOS. Such small CET is due to the higher κ TiLaO and 30-ns LA, to improve the oxide/Ge with lower

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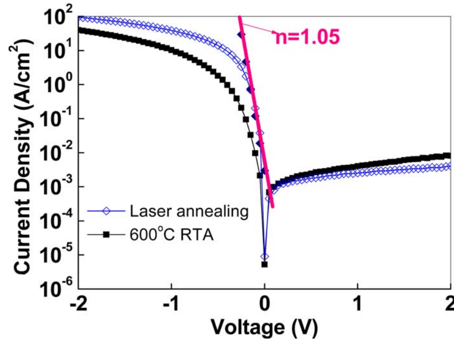

Fig. 2. $J-V$ characteristics of $YbGe_x$/LA n^+-Ge/p-Ge junction.

interface reaction and Ge out-diffusion, from previous cross-sectional transmission electron microscopy and secondary ion mass spectrometry study [12]. The slightly lower capacitance at higher frequency may be related to the gate stack leakage current. The negative flat-band voltage (V_{fb}) is important for low threshold voltage (V_t) nMOSFET, due to the interface dipole of La_2O_3 gate dielectric [22].

It was reported that the LA is an important technology to improve the source–drain junction characteristics for both Ge and Si MOSFETs [7], [16]–[20]. Fig. 2 shows n^+/p junction characteristics of P^+-implanted p-Ge after 0.25-J/cm^2 LA and $YbGe_x$ contact. Small junction ideality (n) factor of 1.05, a low reverse leakage current, and $> 10^5$ on/off current ratio were obtained, where the n-factor is better than the previous 1.10 value using the same LA condition but Al contact [17]. This is the first report of better contact for the n^+/p Ge junction using low work-function metal [6]. A low specific contact resistivity of $4.4 \times 10^{-7}\ \Omega \cdot \mathrm{cm}^2$ was obtained by the transfer length method, due to LA and $YbGe_x$ contact.

Fig. 3(a) and (b) shows the I_d-V_g and mobility-N_s data of TaN/TiLaO/La_2O_3/SiO_2/(111)-Ge nMOSFETs. Standard split C–V at 100 kHz was used for mobility extraction [17]. A low V_t of 0.13 V, a small SS of 101 mV/dec, and an interface trap density of $1.3 \times 10^{13}\ \mathrm{eV}^{-1} \cdot \mathrm{cm}^{-2}$ were obtained. The low V_t near ideal $4kT/q$ (0.11 V) is due to the negative V_{fb} measured from the C–V characteristics shown in Fig. 1, and the small SS is attributed to higher gate capacitance and relatively good interface. From the mobility-N_s plot, good mobility of 432 cm^2/V · s at 10^{13} cm^{-2} N_s were obtained at 1.1-nm CET. The higher mobility than universal SiO_2/Si data at wide medium N_s is the important factor for low power operation toward $<$ 0.5-V V_D operation.

For comparison, other reported high mobility data were also plotted in Fig. 3(b) [8], [14]–[16]. It is important to notice that the mobility rolloff with increasing N_s in this letter is slower than the reported high-κ/GeO_2/Ge nMOS [8], [14], [15]. One possibility of fast mobility degradation in the high-κ/GeO_2/Ge nMOSFET at higher N_s is due to the interface roughness. The RMS surface roughness of control GeO_2/Ge grown at 400 °C is 0.24 nm but becomes much poor to 6.6 nm at 500 °C oxidation. In sharp contrast, the RMS roughness of TiLaO/La_2O_3/SiO_2/Ge after LA is only 0.17 nm. Such very poor roughness may also degrade the mobility at low field.

Another possibility may be related to the small ΔE_C of the GeO_2/Ge interface [23], [24]. We further simulated the electron wave-function distributions in TaN/high-κ/GeO_2/Ge and TaN/high-κ/SiO_2/Ge nMOS at N_s of 10^{11} and 10^{13} cm^{-2}.

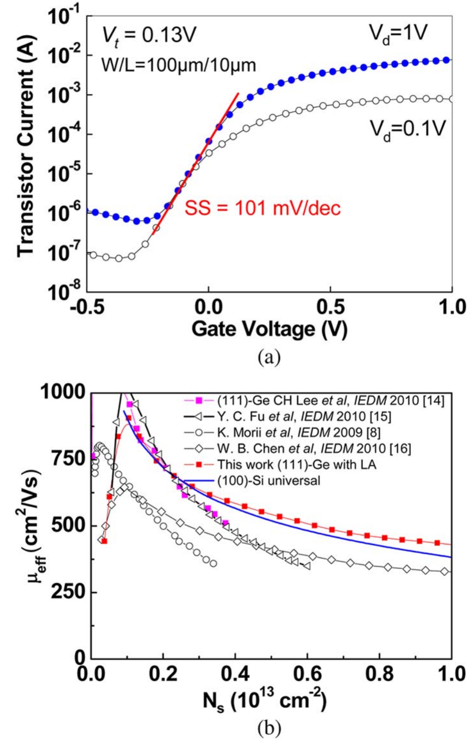

Fig. 3. (a) I_d-V_g and (b) mobility-N_s characteristics of TaN/TiLaO/La_2O_3/SiO_2/(111)-Ge nMOSFETs using LA and $YbGe_x$ contact.

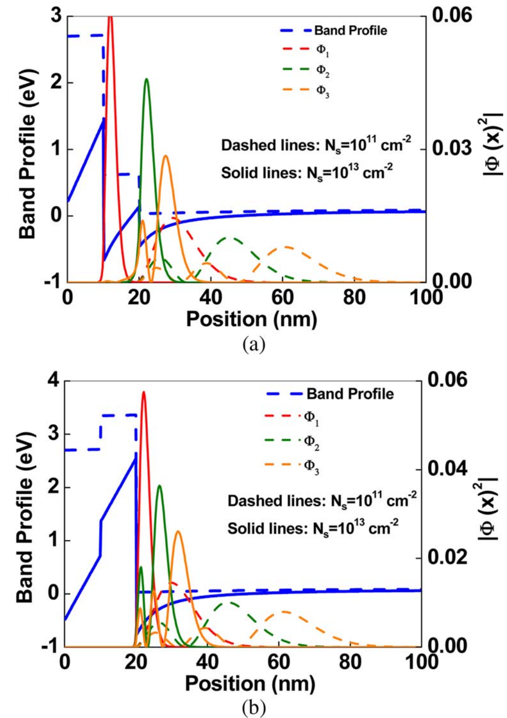

Fig. 4. Electron wave-function distributions in nMOS at inversion. (a) TaN/10-nm Al_2O_3/10-nm GeO_2/Ge. (b) TaN/10-nm Al_2O_3/10-nm SiO_2/Ge. The ΔE_C of 0.8 and 3.2 eV were used for GeO_2/Ge [23], [24] and SiO_2/Ge.

As shown in Fig. 4(a), severe penetration of ground-state electron wave function (Φ_1) in GeO_2 is found at higher N_s. In contrast, slight electron wave-function penetration in TaN/high-κ/SiO_2/Ge is observed due to the large ΔE_C [see Fig. 4(b)]. Thus, the very high peak mobility and smooth interface, but having fast mobility rolloff, may be attributed to

the electron wave-function penetration into low-mobility GeO_2: the electron wave functions are in high-mobility Ge at lower N_s but pulled closer to the GeO_2/Ge interface with Φ_1 distribution in low-mobility GeO_2 at higher N_s.

IV. Conclusion

Higher mobility over wide N_s range than SiO_2/Si data, low SS of 101 mV/dec, small junction n-factor of 1.05, and small CET of 1.1 nm were reached in the TaN/TiLaO/La_2O_3/SiO_2/(111)-Ge nMOSFET.

References

[1] C. H. Huang, M. Y. Yang, A. Chin, W. J. Chen, C. X. Zhu, B. J. Cho, M.-F. Li, and D. L. Kwong, "Very low defects and high performance Ge-on-insulator p-MOSFETs with Al_2O_3 gate dielectrics," in *VLSI Symp. Tech. Dig.*, 2003, pp. 119–120.

[2] C. Chui, H. Kim, D. Chi, B. B. Triplett, P. C. McIntyre, and K. C. Saraswat, "A sub-400 °C Ge MOSFET technology with high-κ dielectric and metal gate," in *Proc. IEDM*, Dec. 2002, pp. 437–440.

[3] W. P. Bai, N. Lu, J. Liu, A. Ramirez, D. L. Kwong, D. Wristers, A. Ritenour, L. Lee, and D. Antoniadis, "Ge MOS characteristics with CVD HfO_2 gate dielectrics and TaN gate electrode," in *VLSI Symp. Tech. Dig.*, 2003, pp. 121–122.

[4] N. Wu, Q. Zhang, C. Zhu, D. S. H. Chan, A. Du, N. Balasubramanian, M. F. Li, A. Chin, J. K. O. Sin, and D. L. Kwong, "A TaN$-HfO_2-$Ge pMOSFETs with novel SiH_4 surface passivation," *IEEE Electron Device Lett.*, vol. 25, no. 9, pp. 631–633, Sep. 2004.

[5] D. S. Yu, A. Chin, C. C. Laio, C. F. Lee, C. F. Cheng, W. J. Chen, C. Zhu, M.-F. Li, S. P. McAlister, and D. L. Kwong, "3D GOI CMOSFETs with novel IrO_2(Hf) dual gates and high-κ dielectric on 1P6M-0.18 μm-CMOS," in *IEDM Tech. Dig.*, 2004, pp. 181–184.

[6] S. Zhu, R. Li, S. J. Lee, M. F. Li, A. Du, J. Singh, C. Zhu, A. Chin, and D. L. Kwong, "Germanium pMOSFETs with Schottky-barrier germanide S/D, high-κ gate dielectric and metal gate," *IEEE Electron Device Lett.*, vol. 26, no. 2, pp. 81–83, Feb. 2005.

[7] Q. Zhang, J. Huang, N. Wu, G. Chen, M. Hong, L. K. Bera, and C. Zhu, "Drive-current enhancement in Ge n-channel MOSFET using laser annealing for source/drain activation," *IEEE Electron Device Lett.*, vol. 27, no. 9, pp. 728–730, Sep. 2006.

[8] K. Morii, T. Iwasaki, R. Nakane, M. Takenaka, and S. Takagi, "High performance GeO_2/Ge nMOSFETs with source/drain junctions formed by gas phase doping," in *Proc IEEE IEDM*, 2009, pp. 681–684.

[9] D. Kuzum, T. Krishnamohan, A. Nainani, Y. Sun, P. A. Pianetta, S-.P. Wong, and K. C. Saraswat, "Experimental demonstration of high mobility Ge NMOS," in *Proc. IEEE IEDM*, 2009, pp. 453–456.

[10] C. H. Lee, T. Nishimura, N. Saido, K. Nagashio, K. Kita, and A. Toriumi, "Record-high electron mobility in Ge n-MOSFETs exceeding Si universality," in *Proc. IEEE IEDM*, 2009, pp. 457–460.

[11] H.-Y. Yu, M. Kobayashi, W. S. Jung, A. K. Okyay, Y. Nishi, and K. C. Saraswat, "High performance n-MOSFETs with novel source/drain on selectively grown Ge on Si for monolithic integration," in *Proc. IEEE IEDM*, 2009, pp. 685–688.

[12] W. B. Chen and A. Chin, "Interfacial layer dependence on device property of high-κ TiLaO Ge/Si n-type metal–oxide–semiconductor capacitors at small equivalent-oxide thickness," *Appl. Phys. Lett.*, vol. 95, no. 21, pp. 212105-1–212105-3, Nov. 2009.

[13] W. B. Chen and A. Chin, "High performance of Ge n-MOSFETs using SiO_2 interfacial layer and TiLaO gate dielectric," *IEEE Electron Device Lett.*, vol. 31, no. 1, pp. 80–82, Jan. 2010.

[14] C. H. Lee, T. Nishimura, T. Tabata, S. K. Wang, K. Nagashio, K. Kita, and A. Toriumi, "Ge MOSFETs performance: Impact of Ge interface passivation," in *Proc. IEEE IEDM*, 2010, pp. 416–419.

[15] Y. C. Fu, W. Hsu, Y. T. Chen, H. S. Lan, C. H. Lee, H. C. Chang, H. Y. Lee, G. L. Luo, C. H. Chien, C. W. Liu, C. Hu, and F. L. Yang, "High mobility high on/off ratio C–V dispersion-free Ge n-MOSFETs and their strain response," in *Proc. IEEE IEDM*, 2010, pp. 432–435.

[16] W. B. Chen, B. S. Shie, A. Chin, K. C. Hsu, and C. C. Chi, "Higher κ metal-gate/high-κ/Ge n-MOSFETs with $<$ 1 nm EOT using laser annealing," in *Proc. IEEE IEDM*, 2010, pp. 420–423.

[17] W. B. Chen, B. S. Shie, and A. Chin, "Higher gate capacitance Ge n-MOSFETs using laser annealing," *IEEE Electron Device Lett.*, vol. 32, no. 4, pp. 449–451, Apr. 2011.

[18] T. Yamamoto, T. Kubo, T. Sukegawa, E. Takii, Y. Shimamune, N. Tamura, T. Sakoda, M. Nakamura, H. Ohta, T. Miyashita, H. Kurata, S. Satoh, M. Kase, and T. Sugii, "Junction profile engineering with a novel multiple laser spike annealing scheme for 45-nm node high performance and low leakage CMOS technology," in *Proc. IEEE IEDM*, 2007, pp. 143–146.

[19] C. C. Liao, A. Chin, N. C. Su, M.-F. Li, and S. J. Wang, "Low V_t gate-first Al/TaN/$[Ir_3Si\text{-}HfSi_{2-x}]$/HfLaON CMOS using simple laser annealing/reflection," in *VLSI Symp. Technol.*, 2008, pp. 190–191.

[20] C. Ortolland, L.-A. Ragnarsson, P. Favia, O. Richard, C. Kerner, T. Chiarella, E. Rosseel, Y. Okuno, A. Akheyar, J. Tseng, J.–L. Everaert, T. Schram, S. Kubicek, M. Aoulaiche, M. J. Cho, P. P. Absil, S. Biesemans, and T. Hoffmann, "Optimized ultra-low thermal budget process flow for advanced high-κ/metal gate first CMOS using laser-annealing technology," in *VLSI Symp. Technol.*, 2009, pp. 38–39.

[21] S. H. Lin, K. C. Chiang, A. Chin, and F. S. Yeh, "High density and low leakage current MIM capacitor using stacked TiO_2/ZrO_2 insulators," *IEEE Electron Device Lett.*, vol. 30, no. 7, pp. 715–717, Jul. 2009.

[22] K. Kita and A. Toriumi, "Origin of electric dipoles formed at high-κ/SiO_2 interface," *Appl. Phys. Lett.*, vol. 94, no. 13, pp. 132902-1–132902-3, Mar. 2009.

[23] M. Perego, G. Scarel, M. Fanciulli, I. L. Fedushkin, and A. A. Skatova, "Fabrication of GeO_2 layers using a divalent Ge precursor," *Appl. Phys. Lett.*, vol. 90, no. 16, pp. 162115-1–162115-3, Apr. 2007.

[24] L. Lin, K. Xiong, and J. Robertson, "Atomic structure, electronic structure, and band offsets at Ge:GeO:GeO_2 interfaces," *Appl. Phys. Lett.*, vol. 97, no. 24, pp. 242902-1–242902-3, Dec. 2010.