Performance Comparison Between Bulk and SOI Junctionless Transistors

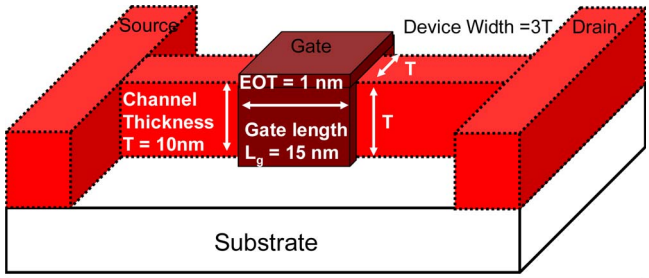
Ming-Hung Han, Chun-Yen Chang, *Life Fellow, IEEE*, Hung-Bin Chen, Jia-Jiun Wu, Ya-Chi Cheng, and Yung-Chun Wu, *Member, IEEE*

***Abstract*—The design and characteristics of a junctionless (JL) bulk FinFET were compared with the silicon-on-insulator (SOI) JL nanowire transistor (JNT) using 3-D quantum transport device simulation. The JL bulk FinFET exhibits a favorable ON/OFF current ratio and short-channel characteristics by reducing the effective channel thickness that is caused by the channel/substrate junction. The drain-induced barrier lowering and the subthreshold slope are about 40 mV and 73 mV/dec, respectively, with an ON/OFF current ratio of 10^5 at $W = 10$ nm. The JL bulk FinFET is less sensitive to the channel thickness than the SOI JNT. Furthermore, the threshold voltage $V_{\rm th}$ of the JL bulk FinFET can be easily tuned by varying substrate doping concentration $N_{\rm sub}$. The modulation range of $V_{\rm th}$ as $N_{\rm sub}$ changes from 10^{18} to 10^{19} cm^{-3}, which is around 30%.**

***Index Terms*—Fin-shaped field-effect transistor (FinFET), junctionless (JL), 3-D simulation.**

I. Introduction

As CONVENTIONAL MOSFETs shrink to the point that their channel lengths are of the order of nanometers, several critical challenges, such as the need to reduce short-channel effect (SCE), to deliver a higher ON-state current, to reduce power consumption, and to eliminate intrinsic parameter fluctuations, must be addressed [1], [2]. Numerous approaches for addressing these issues have been introduced in the past ten years. These include the use of high-k/metal-gate technique to suppress the direct tunneling current in gate oxides, to enhance mobility using strain, and to develop multigate structure such as FinFET and nanowire structures to reduce SCEs [3], [4]. Recently, the concept of the junctionless (JL) nanowire transistor (JNT), which contains a single-doping species at the same level in its source, drain, and channel, has been investigated [5]–[12]. The advantages of JL devices include: 1) avoidance of the use of an ultrashallow source/drain junction, which greatly simplifies the process flow; 2) low thermal budgets owing to implant activation anneal after gate stack formation is eliminated; and 3) the current transport being in the bulk of the semiconductor, which reduces the impact of imperfect semiconductor/insulator interfaces. However, the JNT devices require a silicon-on-insulator (SOI) wafer and a uniform ultrathin channel to turn the device off, making them technologically difficult and expensive to produce.



Device Structure	JL Bulk FinFET	SOI JNT
Gate Workfunction	N: 4.76 eV P: 4.52 eV	N: 5.0 eV P: 4.3 eV
Source/Drain/Channel Doping Concentration	N: 1.5×10^{19}cm^{-3} P: 1.5×10^{19}cm^{-3}	N: 1.5×10^{19}cm^{-3} P: 1.5×10^{19}cm^{-3}
Substrate Material	Silicon with N: 5×10^{18}cm^{-3}, P-type P: 5×10^{18}cm^{-3}, N-type	SiO_2

Fig. 1. Device structure and parameters of simulated JL bulk FinFET and SOI JNT.

This letter compares JL bulk FinFET performances to that of the existing SOI JNT by using 3-D quantum transport device simulation. The advantages of the JL bulk FinFET are as follows. First, the absence of an SOI wafer lowers the cost and improves scalability. Second, it is fully compatibility with the industry standard bulk FinFET CMOS process flow. Third, an additional design parameter, i.e., substrate doping concentration, helps tune the device performance. This letter is organized as follows. In Section II, the simulation method and the setting of the parameters of the devices are introduced. In Section III, the characteristics of different devices are compared, and design of the JL bulk FinFET device is presented. Finally, conclusions are drawn.

II. Simulation Methodology

Fig. 1 presents the structure of the simulated devices and the relevant parameters. The devices have an HfO_2 high-k gate oxide with an equivalent oxide thickness (EOT) of 1 nm, a gate length (L_g) of 15 nm, and a channel thickness (T) of 10 nm. The gate material is TiN with a work function of 4.76 and 4.52 eV (can be tuned by Al incorporation) for n-channel and p-channel JL bulk FinFET [2], [13], [14]. The doping concentrations in the source/drain/channel in both n-channel and p-channel JL Bulk FinFET and SOI JNT are all set to

Manuscript received November 5, 2012; revised November 26, 2012; accepted November 26, 2012. Date of publication January 9, 2013; date of current version January 23, 2013. This work was supported in part by the Taiwan National Science Council under Contract NSC 101-2221-E-007-088-MY2. The review of this letter was arranged by Editor E. A. Gutiérrez-D.

M.-H. Han, C.-Y. Chang, H.-B. Chen, and J.-J. Wu are with the Department of Electronics Engineering and Institute of Electronics, National Chiao Tung University, Hsinchu 300, Taiwan.

Y.-C. Cheng and Y.-C. Wu are with the Department of Engineering and System Science, National Tsing Hua University, Hsinchu 300, Taiwan (e-mail: ycwu@ess.nthu.edu.tw).

Color versions of one or more of the figures in this letter are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/LED.2012.2231395

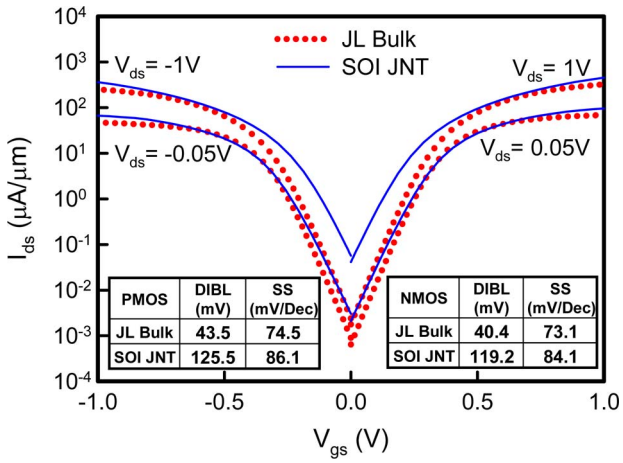


Fig. 2. I_{ds}–V_{gs} curves of the n-channel and p-channel transistors with gate length $L_g = 15$ nm, channel thickness $T = 10$ nm, and EOT $= 1$ nm. The SS and DIBL are shown in the inset.

1.5×10^{19} cm^{-3}, as listed in Fig. 1. The substrate doping is an opposite type with 5×10^{18} cm^{-3} in the JL bulk FinFET, which can be obtained easily by the typical well-implantation process. To adjust threshold voltage $V_{\rm th}$, the work functions of n-channel and p-channel SOI JNTs are tuned to 5 and 4.3 eV, respectively. To obtain accurate numerical results for a nanometer-scale device, the device is simulated by solving 3-D quantum transport equations using the commercial tool Synopsys Sentaurus Device [15]. In quantum transport equations, a density gradient model is used in the simulation. The bandgap narrowing model, the band-to-band tunneling model, and Shockley–Read–Hall recombination with the doping-dependent model are also considered. The direct tunneling model is not utilized because high-k/metal-gate technology is used. The mobility model used in device simulation is according to Mathiessen rule, which is expressed as

$$\frac{1}{\mu} = \frac{D}{\mu_{\rm surf\_aps}} + \frac{D}{\mu_{\rm surf\_rs}} + \frac{1}{\mu_{\rm bulk\_dop}} \qquad (1)$$

where $D = \exp(\mathrm{x/l_{crit}})$, x is the distance from the interface, and $L_{\rm crit}$ is a fitting parameter. The mobility consists of three parts: surface acoustic phonon scattering $\mu_{\rm surf\_aps}$, surface roughness scattering $\mu_{\rm surf\_rs}$, and bulk mobility with doping-dependent modification $\mu_{\rm bulk\_dop}$; the details are described in [15].

III. Results and Discussions

Fig. 2(a) plots the I_{ds}–V_{gs} curves of the n-channel and p-channel devices of interest, in which the linear threshold voltage is adjusted to approximately ±300 mV to enable a fair comparison. Without applying channel engineering or strain technology, the n-channel JL bulk FinFET has an ON-state current of 322 μA/μm (at $V_{gs} = 1$ V and $V_{ds} = 1$ V) and an OFF-state current of 1.7 nA/μm (at $V_{gs} = 0$ V and $V_{ds} = 1$ V), respectively, which is normalized to the device width ($W = 3$T, including top, left, and right sides). The subthreshold slope (SS) is 73.1 mV/dec, and drain-induced barrier lowering (DIBL), which is defined as the difference in $V_{\rm th}$ between $V_{ds} = 0.05$ V and $V_{ds} = 1$ V, is only 40.4 mV. These simulation

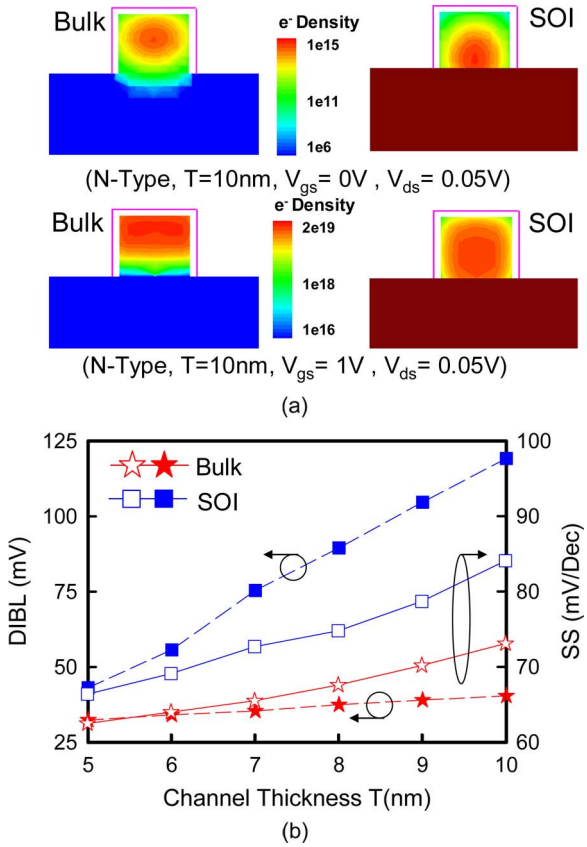


Fig. 3. (a) Electron density distributions in the middle of the channel at OFF-state ($V_{gs} = 0$ V) and ON-state ($V_{gs} = 1$ V) for $L_g = 15$ nm, $T = 10$ nm, and EOT $= 1$ nm. (b) DIBL and SS comparison with different channel thicknesses T between the n-channel JL Bulk FinFET and the SOI JNT with $L_g = 15$ nm and EOT $= 1$ nm.

performances are comparable with similar JL devices in recent years [5], [8], [9]. Additionally, the extracted mobility is about 90 cm^2/V $\cdot$ s at $V_{gs} = 0.5$ V, which are also confirmed with experimental mobility data [16]. The p-channel JL bulk FinFET performs similarly. The comparison of the simulated DIBL and SS in the inset in Fig. 2(a) reveals that the JL bulk devices outperform the SOI devices for channel thickness $W = 10$ nm. To examine thoroughly the phenomena that are evident in JL devices, the electron density distributions in the center of the channel region is determined for both OFF-state ($V_{gs} = 0$ V) and ON-state ($V_{gs} = 1$ V), as shown in Fig. 3(a). The electrons are concentrated in the middle of the channel region in both the JL bulk FinFET and the SOI JNT because they are repelled by the electric field at the channel/oxide interface [5]–[8]. Hence, the JL devices exhibit bulk conduction, which prevents surface scattering of the current. Moreover, as presented in Fig. 3(a), the electrons are more concentrated on the top of the channel in JL bulk FinFET. Since the channel/substrate junction produces an additional depletion region, the effective channel thickness is reduced, improving the controllability of the gate over that in the SOI JNT. Fig. 3(b) compares the DIBL and SS characteristics of the JL bulk FinFET and the SOI JNT with different channel thicknesses T. As T is reduced, although SS and DIBL approach to their ideal values (60 mV/dec and 0 mV) for both devices, the DIBL in the JL bulk FinFET remains almost constant as T varies, indicating that its performance is less sensitive to process variation. In addition, since the JL bulk

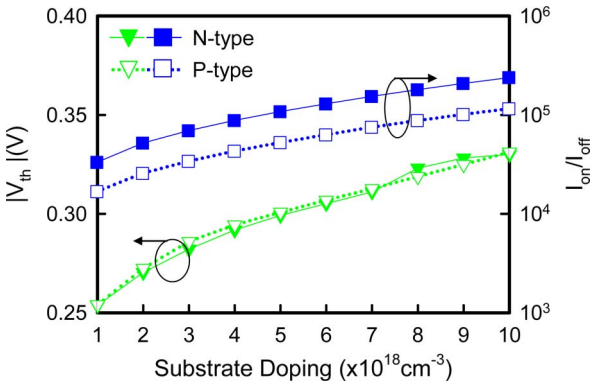


Fig. 4. Threshold voltages and ON/OFF current ratios of JL bulk FinFET for different substrate doping concentration.

FinFET with a large T perform similar short-channel control as compared with SOI JNT with smaller T, the large channel volume in JL bulk FinFET may have a small random dopant fluctuation (RDF) effect. However, the RDF is still a crucial problem and further comprehensive analysis of the characteristics fluctuation caused by the RDF is required. Fig. 4 displays the $V_{\rm th}$ and ON/OFF current ratio of the JL bulk FinFET versus substrate doping concentration. Similar to the channel doping concentration, the channel thickness, gate oxide thickness, and gate work function [1], [4]–[9], the $V_{\rm th}$ can also be easily tuned by controlling the substrate doping concentration. The range of modulation of $V_{\rm th}$ is about 30% as the substrate doping concentration varies from 10^{18} to 10^{19} cm^{-3}.

IV. Conclusion

In this letter, the electrical and physical characteristics of JL bulk FinFET and SOI JNT have been explored. The results of a 3-D quantum transport device simulation demonstrate that the JL bulk FinFET has a higher ON/OFF current ratio and better short-channel characteristics than that of the existing SOI JNT. The electron density distributions indicate that the JL bulk FinFET exhibited bulk conduction and did not suffer from surface scattering. Additionally, the reduction in the effective channel thickness by the channel/substrate junction helps to reduce the SCE and the OFF-state current, and the sensitivity to the physical thickness of the channel. With respect to device design, the JL bulk FinFET offers an additional design parameter, i.e., the substrate doping concentration, for controlling device performance.

References

[1] C. Hu, "Device challenges and opportunities," in *VLSI Symp. Tech. Dig.*, Jun. 2004, pp. 4–5.
[2] Y. Li, C.-H. Hwang, T.-Y. Li, and M.-H. Han, "Process variation effect, metal-gate workfunction and random dopant fluctuations in emerging CMOS technologies," *IEEE Trans. Electron Devices*, vol. 57, no. 2, pp. 437–447, Feb. 2010.
[3] G. D. Wilk, R. M. Wallace, and J. M. Anthony, "High-k gate dielectrics: Current status and materials properties considerations," *J. Appl. Phys.*, vol. 89, no. 10, pp. 5243–5275, May 2001.
[4] D. Hisamoto, W.-C. Lee, J. Kedzierski, H. Takeuchi, K. Asano, C. Kuo, E. Anderson, T.-J. King, J. Bokor, and C. Hu, "FinFET—A self-aligned double-gate MOSFET scalable to 20 nm," *IEEE Trans. Electron Devices*, vol. 47, no. 12, pp. 2320–2325, Dec. 2000.
[5] C.-W. Lee, A. Afzalian, N. D. Akhavan, R. Yan, I. Ferain, and J. P. Colinge, "Junctionless multigate field-effect transistor," *Appl. Phys. Lett.*, vol. 94, no. 5, pp. 053511-1–053511-2, Feb. 2009.
[6] J.-P. Colinge, C.-W. Lee, A. Afzalian, N. D. Akhavan, R. Yan, I. Ferain, P. Razavi, B. O'Neill, A. Blake, M. White, A.-M. Kelleher, B. McCarthy, and R. Murphy, "Nanowire transistors without Junctions," *Nat. Nanotechnol.*, vol. 5, no. 3, pp. 225–229, Mar. 2010.
[7] J. P. Colinge, C.-W. Lee, I. Ferain, N. D. Akhavan, R. Yan, R. Razavi, R. Yu, A. N. Nazarov, and R. T. Doria, "Reduced electric field in junctionless transistors," *Appl. Phys. Lett.*, vol. 96, no. 7, pp. 073510-1–073510-3, Feb. 2010.
[8] A. Kranti, R. Yan, C.-W. Lee, I. Ferain, R. Yu, N. D. Akhavan, P. Razavi, and J. P. Colinge, "Junctionless nanowire transistor (JNT): Properties and design guidelines," *Solid State Electron.*, vol. 65/66, pp. 33–37, Nov./Dec. 2011.
[9] R. Yu, S. Das, I. Ferain, P. Razavi, M. Shayesteh, A. Kranti, R. Duffy, and J. P. Colinge, "Device design and estimated performance for p-type junctionless transistors on bulk germanium substrates," *IEEE Trans. Electron Devices*, vol. 59, no. 9, pp. 2308–2313, Sep. 2012.
[10] H.-C. Lin, C.-I. Lin, and T.-Y. Huang, "Characteristics of n-type junctionless poly-si thin-film transistors with an ultrathin channel," *IEEE Electron Device Lett.*, vol. 33, no. 1, pp. 53–55, Jan. 2012.
[11] C.-J. Su, T.-I. Tsai, Y.-L. Liou, Z.-M. Lin, H.-C. Lin, and T.-S. Chao, "Gate-all-around junctionless transistors with heavily doped polysilicon nanowire channels," *IEEE Electron Device Lett.*, vol. 32, no. 4, pp. 521–523, Apr. 2011.
[12] R. Rios, A. Cappellani, M. Armstrong, A. Budrevich, H. Gomez, R. Pai, N. Rahhal-Orabi, and K. Kuhn, "Comparison of junctionless and conventional trigate transistors with Lg down to 26 nm," *IEEE Electron Device Lett.*, vol. 32, no. 9, pp. 1170–1172, Sep. 2011.
[13] H. Dadgour, K. Endo, V. De, and K. Banerjee, "Modeling and analysis of grain-orientation effects in emerging metal-gate devices and implications for SRAM reliability," in *IEDM Symp. Tech. Dig.*, Dec. 2008, pp. 1–4.
[14] H.-C. Wen, S. C. Song, C. S. Park, C. Burham, G. Bersuker, K. Choi, M. A. Q. Lopez, B. S. Ju, H. N. Alshareef, H. Niimi, H. B. Park, P. S. Lysaght, P. Majhi, B. H. Lee, and R. Jammy, "Gate first metal-aluminum-nitride PMOS electrodes for 32 nm low standby power applications," in *VLSI Symp. Tech. Dig.*, Jun. 2007, pp. 160–161.
[15] User's Manual for Synopsys Sentaurus Device.
[16] K.-I. Goto, T.-H. Yu, J. Wu, C. H. Diaz, and J. P. Colinge, "Mobility and screening effect in heavily doped accumulation-mode metal-oxide-semiconductor field-effect transistors," *Appl. Phys. Lett.*, vol. 101, no. 7, pp. 073503–073503-2, Aug. 2012.