Solution-Processed Vertical Organic Transistors Fabricated by Nanoimprint Lithography

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***Abstract*—In this letter, we demonstrate the first vertical-channel organic transistor using nanoimprint technology to produce a base electrode with high-density nanometer pores to well control the channel current vertically flowing through the pores. The aspect ratios of nanopores, which determine the switching performance of the vertical transistor, are greatly enhanced by transferring the nanostructure to the underlying layers. Without pore accumulation, a low leakage current can be achieved. The vertical transistor delivers an ON current of 0.35 mA/cm^2 and an ON/OFF current ratio of around 3000 at 1.8 V. The results prove the feasibility to produce low-voltage organic transistors over a large area with potentially low production cost.**

***Index Terms*—Interference lithography, nanoimprint, organic transistor, solution process, vertical transistor.**

I. Introduction

SOLUTION-processed organic transistors are promising for the development of low-cost and large-area electronic devices on flexible substrates [1]. Low field-effect mobility (i.e., lower than 2 cm^2/V · s) and high operation voltage (i.e., larger than 10 V), however, cause problems such as low driving current and high power consumption. To lower down the operation voltage and to increase the output current, organic transistors with a vertical short channel were demonstrated [2]–[4]. Previously, we also successfully demonstrated a vertical-channel solution-processed organic transistor, named space-charge-limited transistor (SCLT), to have promising transistor characteristics. Improving polymer chain ordering by using solvent annealing or self-assembled monolayer treatment, an output current high enough to drive organic light-emitting diodes (OLEDs) (12–50 mA/cm^2) was obtained at a low operation voltage ($<$ 2 V) [3], [4]. Using solution-processed transistors to drive solution-processed OLEDs [5] may become next-generation display technology. However, colloidal lithography used in our previous results is not compatible with existing commercialized tools. More importantly, the nanosphere accumulation causes leakage current through large holes [3]. It is thus difficult to have uniform leakage control when nanosphere accumulation is randomly distributed.

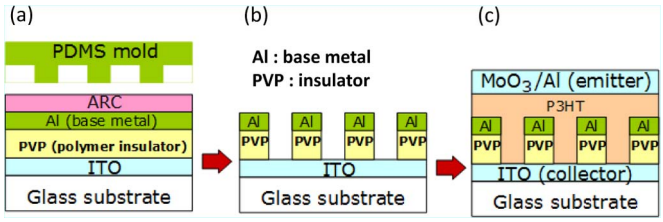

Fig. 1. Fabrication process of the *Imprint SCLT*. (a) Key step of utilizing nanoimprint. (b) After etching. (c) Final device.

Some groups demonstrated vertical-channel organic transistors with an ordered nanometer pore structure in a base/gate metal by using laser holographic lithography or a modified Langmuir–Blodgett method [6], [7]. These methods, however, are expensive or time-consuming for large-area production. Nanoimprint lithography (NIL) has been enlisted in the International Technology Roadmap for Semiconductors litho roadmap down to 11 nm for almost a decade, which confirms its capability of nanoscale fabrication [8]. Roll-to-roll NIL has been also demonstrated as a promising low-cost large-area fabrication process [9], [10].

Here, we successfully used NIL to fabricate a vertical-channel SCLT. The nanostructure was imprinted onto a layered substrate and then transferred to underlying layers. Nanometer holes with a high aspect ratio are produced to facilitate good base control over the vertical channel. No hole accumulation is observed. The proposed *Imprint SCLT* exhibits an ON current of 0.35 mA/cm^2 and an ON/OFF current ratio of around 3000 at 1.8 V. The base leakage current can be controlled below 10^{-3} mA/cm^2. A larger ON current is expected by further improving the pattern-transferring process and the polymer chain ordering in the future.

II. Experimental

As shown in Fig. 1(c), the SCLT is a three-terminal device that functions similar to the vacuum tube triode. The carrier holes are injected into the semiconducting polymer by the emitter, passing through the openings on the base, and finally collected by the collector [4]. The base metal (aluminum) control the potential barrier in the vertical channel and, hence, the ON and OFF states of the SCLT. Typically, a good switching

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swing smaller than 250 mV/dec can be achieved when the aspect ratio of the vertical channel (i.e., channel height over channel diameter) is larger than 1.5 [4].

The process to fabricate the *Imprint SCLT* is described in Fig. 1. First, the layered substrate with antireflection coating (ARC, 110 nm)/aluminum metal (40 nm)/polymer insulator (cross-linked poly(4-vinyl phenol), PVP, 200 nm) on an indium tin oxide (ITO) glass substrate is prepared, as shown in Fig. 1(a). ARC is from Nissan Chemical Industries (mode no. XHRiC-11). The cross-linkable PVP (8 wt.%) and the cross-linking agent poly(melamine-co-formaldehyde) (PMF) were dissolved in propylene glycol monomethyl ether acetate with a PVP/PMF mass ratio of 11:4. PVP was spin coated on an ITO glass substrate with 2000 Å thickness and annealed at 200 °C for 1 h. Al with 40 nm thickness was thermal deposited to serve as the base electrode. Then, we spin coated ARC on Al with 110 nm thickness without baking and then flipped a polydimethylsiloxane (PDMS) imprinting mold on the Al region without any contact by hand. The PDMS imprinting mold has a rod array pattern in one side with a period of 500 nm, a duty cycle of around 50% [10], and a height of around 220 nm. The rod array pattern was transferred from the hole array photoresist pattern, which was made using two-beam interference with two times 90° cross exposure $(25\ \text{mJ/cm}^2 \times 2)$.[1] Using two 125-$\mu$m-thick polycarbonate (PC) films to collapse the PDMS mold and the substrate in the imprinting machine with a pressure at 10 bar at 175 °C for 5 min, the hole array ARC pattern was made. Then, we used reactive ion etching to remove the residual ARC in the holes. The nanopore structure was then transferred to the aluminum metal by a simple wet etching process with a standard aluminum etchant. The PVP at the sites without Al coverage was removed by 150 W O_2 plasma, and the vertically oriented PVP cylindrical nanopores were formed. Three hundred fifty nanometers of poly(3-hexylthiophene) in chlorobenzene was coated as the active material. Finally, MoO_3 (10 nm) and Al (40 nm) were deposited to serve as the top electrode and to complete the SCLT with an active area of 1 mm^2.

III. Results and Discussion

Fig. 2(a) shows the hole array etching mask of the ARC film on the Al surface. Good uniformity is obtained over an area of $2 \times 1.5\ \text{cm}^2$. We use the nanoimprinting method within two PC films to fabricate the hole array etching mask, which provides uniform and proper pressure under the imprinting process. The air between PC films can reduce edge stress and provide tunable pressure to overcome imprinting pressure. The soft PDMS mold avoids overpressing on the Al surface. Currently, the ARC material is a thermal curing material. If we replace ARC by an ultraviolet curing material with good chemical resistance and small thickness (i.e., $<$ 130 nm), we may further reduce the process time to facilitate mass production. After imprinting, the leakage current of the underlying PVP insulating layer with 3-V bias decreases from 10^{-4} to 10^{-5} mA/cm^2 [see Fig. 2(b)], whereas the PVP thickness remains unchanged. The 5-min 175 °C high-pressure imprinting may serve as an annealing/pressing process to remove pinholes or to remove the remaining solvent in the PVP layer. Further verification in the mechanism is required in the future.

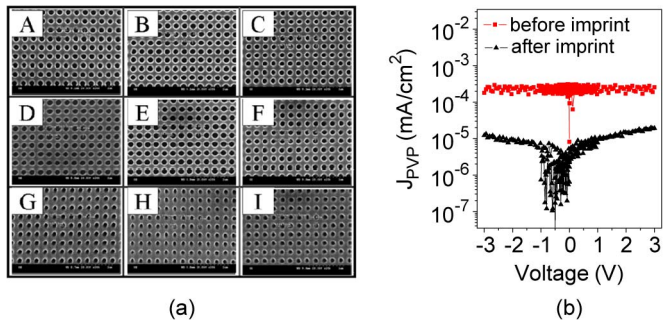

Fig. 2. (a) SEM images of the hole array etching mask (ARC) on the Al surface on different positions on the area of $2 \times 1.5\ \text{cm}^2$. (b) Leakage current density of the PVP layer before and after nanoimprinting.

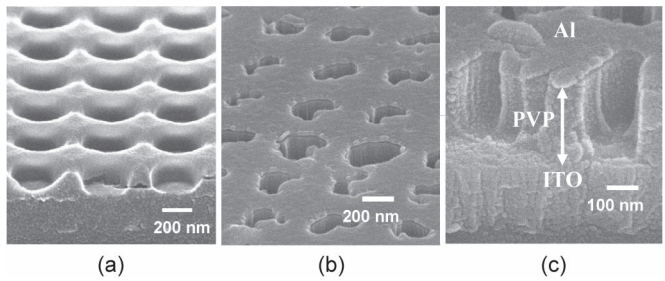

Fig. 3. SEM images of the (a) ARC pattern and Al nanopore structure after Al wet etching. (b) and (c) Vertically oriented PVP cylindrical nanopores covered by the Al hard mask.

After using reactive ion etching to remove the residual ARC in the holes and using wet etching to remove the exposed aluminum, the SEM image of the sample is shown in Fig. 3(a). A well-ordered nanopore structure remains on top of the samples with a poor aspect ratio (< 0.5). Then, after O_2 plasma etching through the 200-nm-thick PVP layer, the vertically oriented cylindrical nanopores with high aspect ratios are shown by the SEM image in Fig. 3(b) and (c). The ARC structure above the aluminum layer is removed. The aluminum (base electrode) with an ordered nanopore structure is successfully formed. The distortion of the pore shape may be due to the poor uniformity of the aluminum etching rate in the wet etching process. The commercial aluminum dry etching process is expected to significantly improve the pattern transfer in the future.

With high aspect ratios in nanopores, the *Imprint SCLT* successfully delivers normal transistor functions regardless of the distortion of the pore shape. The collector current density J_C as a function of collector voltage V_{CE} and that as a function of base voltage V_{BE} of the *Imprint SCLT* are shown by solid lines in Fig. 4(a) and (b), respectively. We obtain an ON current

[1]The photoresist hole array pattern composite with Si substrate, ARC (165 nm thick, baking for 1 min at 175 °C), and photoresist Sumitomo (250 nm thick, soft baking for 1 min at 110 °C, baking after exposure for 1 min at 110 °C, and, finally, hard baking for 1 min at 140 °C after development), the period and duty cycle are the same as the PDMS rod array. For the pattern transfer procedure, Sylgard 184 A and B were mixed together with the ratio of 10:1 and stirred well enough. After degassing, we cast the PDMS solution in the Petri dish covered on the photoresist pattern and then hold the temperature at 80 °C for 2 h. Waiting for at least two days in room temperature, we demold by hand slowly and cut a proper size, and the PDMS rod array mold was made.

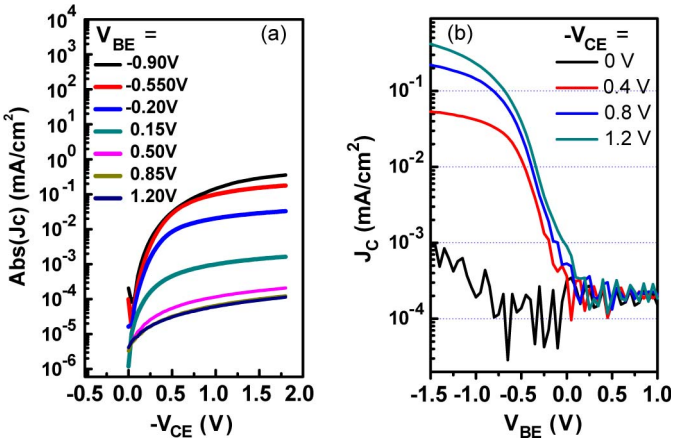

Fig. 4. (a) Output characteristics J_C–$V_{\rm CE}$ and (b) transfer characteristics J_C–$V_{\rm BE}$ of the *Imprint SCLT*. The range of the applied bias is defined by controlling J_B smaller than 10^{-3} mA/cm^2. When $V_{\rm CE} = -1.8$ V, the ON/OFF ratio is 3000 when $V_{\rm BE}$ changes from -0.9 V (ON state) to 1.2 V (OFF state).

of 0.35 mA/cm^2 and an ON/OFF current ratio of around 3000 at $V_{\rm CE}$ of 1.8 V. A base leakage current density J_B lower than 10^{-3} mA/cm^2 is obtained (not shown), verifying the feasibility of the proposed process.

IV. Conclusion

We have demonstrated the first vertical-channel solution-processed organic transistor using nanoimprint technology. The imprinting process generates an ordered nanopore structure without pore accumulation, successfully avoiding large leakage current through large holes. The high-pressure imprinting also enhances the insulating property of the underlying polymer insulator. The *Imprint SCLT* exhibits an ON current of 0.35 mA/cm^2 and an ON/OFF current ratio of around 3000 at 1.8 V. The low operation voltage facilitates the development of low-power organic electronics. The combination of interference lithography and nanoimprinting method demonstrates a potentially low-cost process of organic vertical transistors and indicates the feasibility of mass production over a large area.

Acknowledgment

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