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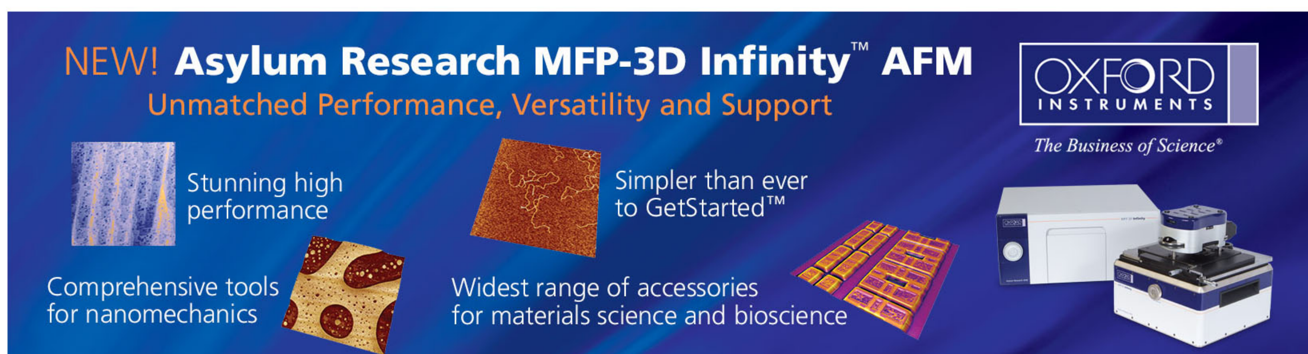

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Probing into the metal-graphene interface by electron transport measurements

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Metal-graphene contact recently attracts much attention because of its effects on the performance and the operational speed of graphene field-effect transistor. Simple two-probe graphene devices on mechanically exfoliated graphene flakes are fabricated and the temperature behavior of resistance is measured from room temperature down to liquid helium temperature for the study of electron transport in the interface. Comparing experimental data with several different transport theories, it is confirmed that the model of fluctuation-induced tunneling conduction describes precisely the electron transport and indicates the existence of a thin insulating layer in the metal-graphene interface. Through the interface probing by electron transport measurements, the way to reduce the contact resistance is suggested. © *2013 American Institute of Physics*. [http://dx.doi.org/10.1063/1.4789554]

Since the exhibition of an electric field effect on the ultrathin graphene metal in 2004,[1] the peculiar two-dimensional material has drawn a tremendous amount of attentions. Graphene is considered as one promising candidate for the development of the next-generation electronics after discoveries of its electron's linear energy-momentum dispersion[1] and ultrahigh mobility,[2] its tolerance of high current density,[3] its transparency,[4] and its flexibility.[5] On the other hand, graphene applications in gas sensors,[6] photodetectors,[7] solar cells,[8] and field-effect transistors,[9] even operated in a gigahertz frequency,[10] have been demonstrated at the preliminary stage. Recently, circuit components of transistors and inductors are integrated and made based on graphene to illustrate an integrated circuit on wafer-scale graphene for an industrial application.[11] To materialize graphene applications in electronics, the metal/graphene interface needs to be explored, thus approaching the control of an Ohmic contact.

The issue of metal contact on graphene is particularly interesting in recent years. A theoretical calculation of the graphene metalization with different metals, which causes graphene doping, a shift of the Fermi level, and the formation of the interface dipole and the potential step, was reported in 2008.[12] It was immediately corroborated in an elaborately experimental work using scanning photocurrent microscopy.[13] Thereafter, the transfer length method and the four-probe measurement were employed to examine the contact resistance in relation to the number of graphene layers.[14,15] The evaluated contact resistance revealed either a temperature independence or a temperature dependence of an insulator.[15] Additionally, the contact length and the transfer length in the metal-graphene contact were extensively studied. Through the investigations, it was inferred that the current flows preferentially through the edge of the metal electrode.[16] Further, the mean free path and the coupling length at the metal-graphene interface were explored.[17] The ballistic transport in the interface had been observed at low temperatures and, in contrast, a diffusive transport showing a metallic temperature behavior had been noted at higher temperatures.[17] The contact length and the contact resistance effects on the transconductance of the graphene transistor were addressed.[18,19] In addition to ideal contacts, other possibilities including the parasitic resistance[20] and the formation of a titanium carbide layer[21] were specified whereas a gentle oxygen etching and a thermal treatment could be implemented to reduce the contact resistance.[22]

In this work, simple two-probe devices of mechanically exfoliated graphene were fabricated for probing into the metal-graphene interface. We carried out a systematic current-voltage measurements at various temperatures down to 5 K to delineate a complete behavior of electron transport in the metal-graphene interface. We discovered that the contact resistance variation in the wide temperature range is highly in agreement with Ping Sheng's model of fluctuation-induced tunneling conduction (FITC).[23] The tunneling nature of the FITC model implies an insulating layer of either titanium oxides or titanium carbides in the interface.

Heavily doped Si wafers with a 300-nm thick, thermally grown SiO_2 capping layer were used as substrates for photolithography to make a large pattern of metal electrodes. Graphene flakes were prepared by mechanical exfoliation on the substrates which were taken as a back gate electrode. The thickness of the graphene flakes was determined by optical microscope, atomic force microscope, and scanning electron microscope (SEM, Hitachi S-3000H). After spotting thin graphene flakes, the standard electron-beam lithography and the thermal evaporation were employed to make two Ti/Au electrodes (~30/50 nm in thickness) in connection with the photolithographically patterned electrodes. The separation distance between the two source and drain electrodes on graphene flakes was purposely kept at a constant of 1 μm. The as-fabricated graphene devices were then annealed in a high vacuum at 400 °C for 10 min so as to reduce the contact resistance. These devices were loaded in an insert cryostat (Variable Temperature Insert Cryostat, CRYO Industries of

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America, Inc.) in a low vacuum at room temperature (RT) or in 1-atm He gas at low temperatures. Measurements of current-voltage (*I*–*V*) curves were performed by Keithley 6430 at a wide temperature range between RT and 5 K and the resistance was estimated from the *I*–*V* curves in the regime of a linear dependence.

Figure 1(a) displays a SEM image of a typical, simple two-probe graphene device with its corresponding design scheme presented in the inset. Graphene flakes with a thickness of ∼1-2 nm were purposely selected for our device fabrication. To reduce the high contact resistance due to the short contact length,[19] the metal electrode is intentionally patterned to several micrometers in width. RT resistance of all graphene devices is summarized in the statistical distribution in Fig. 1(b). It reveals a broad distribution of device RT resistance up to several tens of kilo-ohms. In this study, the experimental conditions of the graphene thickness, device fabrication process, and the separation distance between neighboring electrodes are kept the same, while the device RT resistance changes largely between different samples. Hence, the observed resistance variation is attributed to the contact resistance which may give a high contribution ratio to the graphene device resistance. Using the back gate electrode, the gate voltage dependence of the graphene device is presented in Fig. 1(c) in the voltage range between −50 and 50 V. The maximum resistance of about 3.9 kΩ occurs at the gating voltage of 3 V. It is noted that the gating only results in a small change of resistance variation (∼200%). Additionally, *I*–*V* curves at various temperatures are displayed in Fig. 1(d). Though the *I*–*V* curves show a linear dependence in the voltage range, the current at a fixed voltage, however, decreases with decreasing temperature. The result shows a temperature dependence similar to an insulator that is inconsistent with the metallic feature of the graphene flakes. All the clues point to the same issue of a high ratio contribution of the contact resistance.

The first rational speculation of electron transport in the metal-graphene interface is to overcome a metal-semiconductor barrier of a Schottky type contact. To check the coincidence between our data and the model of the thermionic emission for a Schottky contact,[24] the figure of $\ln(I/T^{3/2}) - 1/T$ of the graphene G1-G7 devices is plotted in Fig. 2(a). It is clear that the model cannot describe current at temperatures lower than 150 K thus we exclude the possibility of the Schottky type contact. The second speculation might be the introduction of oxides in the contact to render a disorder and an electron hopping feature.[25,26] Figure 2(b) presents data of the G1 device in comparison with the three-dimensional (3D) Mott's variable range hopping (VRH) model[27] of the expression $R(T) = R'\exp((T'/T)^{1/4})$, where $R(T)$ is the temperature dependent resistance, and R' and T' are two constants. Obviously, the 3D Mott's VRH model cannot describe the electron transport in the metal-graphene interface. Neither can the semiconductor transport model of the thermal activation be used to explain the data. The data in Fig. 2(b) reveal a saturation behavior at lower temperatures which signifies the approach of the temperature independent tunneling regime while they agree with thermal activation model at high temperatures. Consequently, the FITC model is adopted for fitting and, more surprisingly, it gives a high corresponding to the device's temperature dependent resistance in a wide temperature range between RT and 5 K. Figure 2(c) shows the fitting of FITC model to data of graphene G1-G7 devices.

The FITC model describes the temperature behavior of resistance by the equation $R(T) = R_0\exp(T_1/(T + T_0))$,[23]

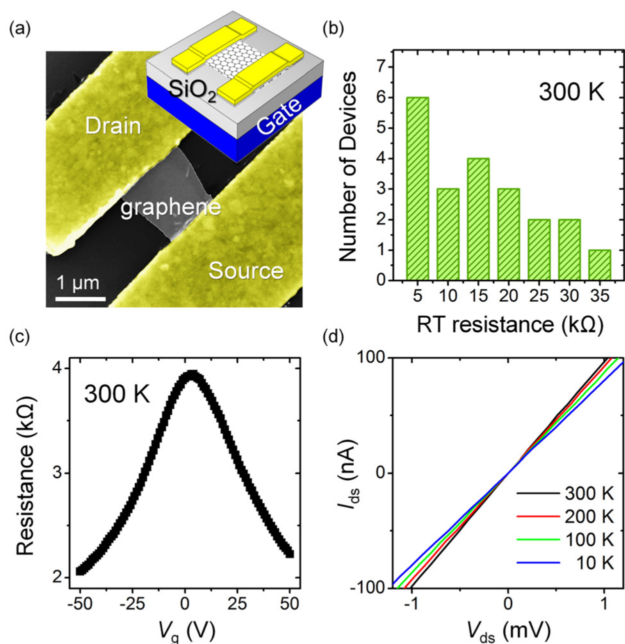

FIG. 1. (a) SEM image of the graphene device with its corresponding design scheme drawn in the inset. (b) Histogram of the RT resistances of all graphene devices at a zero gate voltage. (c) Gate voltage dependence of the graphene device at a source-drain voltage of 1 mV. (d) *I*–*V* curves of the device at various temperatures.

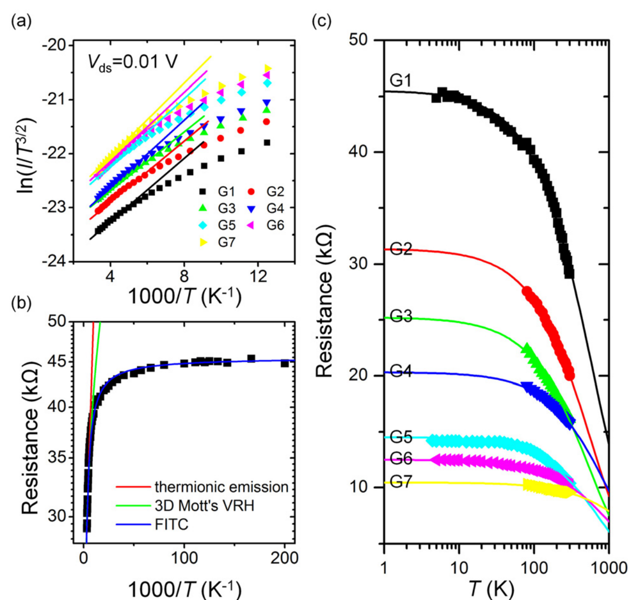

FIG. 2. (a) $\ln(I/T^{3/2})$ as a function of inverse temperature for the graphene G1–G7 devices. The solid lines present fittings to the thermionic emission theory. (b) Temperature dependent resistance of the G1 device. The solid curves in red, green, and blue are fittings to the thermionic emission, the 3D Mott's VRH, and the FITC models, respectively. (c) Temperature dependent resistance of the G1–G7 devices. The symbols and solid curves present experimental data and the best fits to the FITC model.

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where R_0 is a constant, and T_1 and T_0 are parameters of characteristic temperatures. The model proposes the formation of multiple tunneling junctions between two metal electrodes due to an ultra-thin insulating layer. The multiple tunneling junctions can be treated as one effective tunneling junction which has an effective junction width w, barrier height V_0, and junction area A. The thermal energy randomly excites electrons on one side of the metal electrode at the junction. If the junction area is small, the high density electrons on such a small area can be easily driven across the junction. The model derives the two characteristic temperatures as $T_1 = (8\varepsilon/e^2 k_B)(AV_0^2/w)$ and $T_0 = (16\varepsilon\hbar/\pi e^2 k_B (2m)^{1/2})(AV_0^{3/2}/w^2)$,[23] where ε is the dielectric constant of the thin insulator, e and m are electron's charge and mass, and k_B is the Boltzmann constant. It is noted that T_1 implies electron's required energy to cross the junction and T_0 is the temperature below which the thermal fluctuated voltage becomes negligibly small.

The two characteristic temperatures T_1 and T_0 which are estimated from data fitting in Fig. 2(c) are displayed in Figs. 3(a) and 3(b) with respect to the device RT resistance. The two characteristic temperatures do not exhibit any correlation with the device RT resistance whereas the ratio T_1/T_0 exposes a tentative dependency with regard to the device RT resistance in logarithmic scale (Fig. 3(c)). Assuming that the junction formation is owing to the correlative materials of titanium oxides or carbides, we may take, for example, the junction barrier height V_0 of $\sim$0.17 eV as the energy difference between the graphene work function ($\sim$4.5 eV)[12] and the TiO_2 electron affinity ($\sim$4.33 eV).[28] The junction width is evaluated and presented in Fig. 3(c). It points to an exponential growth of the device RT resistance with an increase of the effective junction barrier width. In addition, the effective junction area is calculated and presented in Fig. 3(d). The device of low RT resistance signifies a contracted junction area. Integrating both the junction width and the area

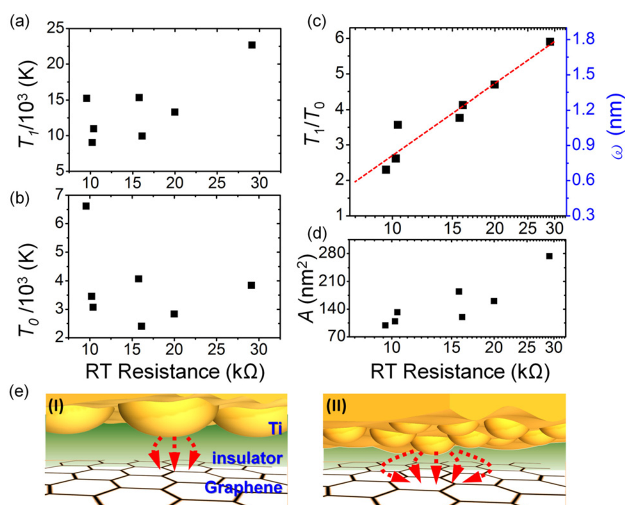

FIG. 3. Two parameters T_1 (a) and T_2 (b), extracted from curve fittings in Fig. 2(c), are displayed with respect to their device RT resistance. (c) The ratio of T_1/T_0 and the calculated value of the effective barrier width w as a function of the device RT resistance. The dashed line in red is a guide to eyes. (d) The calculated value of the effective area A as a function of the device RT resistance. (e) Schemes of electron transport in the metal-graphene interface for the two configurations of large (I) and small (II) grains of metal films. The arrows in red demonstrate possible tunneling paths for electrons.

effects on the device and contact resistance, we summarize that the metal film with smaller grains benefits to reduce the contact resistance even for the existence of an ultra-thin insulator in the metal-graphene interface. The idea is given in schemes (I) and (II) in Fig. 3(e). The smaller gains in scheme II give rise to high current as well as many electron's tunneling paths as a result of their smaller junction areas and shorter junction widths.

In summary, simple, two-probe devices with a back gate electrode are manufactured on mechanically exfoliated graphene flakes. The graphene devices exhibit high contact resistances which dominate to graphene device resistances. To probe into the metal-graphene interface, we perform measurements of temperature dependent resistance from RT down to 5 K and discover that the interfacial electrical properties can be well described by the FITC model. The result indicates a thin insulating layer between the graphene and the metal electrode. The effective barrier width and the junction area in the metal-graphene interface are estimated from fitting the temperature dependent resistances of all graphene devices. The device RT resistance increases in conjunction with an increase of the effective barrier width and the junction area, thus corroborating a reduction of contact resistance through the preparation of more flat metal thin films with very small grains as metal electrodes.

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