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Impact of strain on gate-induced floating body effect for partially depleted silicon-on-insulator p-type metal–oxide–semiconductor-field-effect-transistors

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A R T I C L E I N F O

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A B S T R A C T

This work investigates impact of mechanical strain on gate-induced-floating-body-effect (GIFBE) for partially depleted silicon-on-insulator p-type metal–oxide–semiconductor field effect transistors (PD SOI p-MOSFETs). First part, the original mechanism of GIFBE on PD SOI p-MOSFETs is studied. The experimental results indicate that GIFBE causes a reduction in oxide electric field (E_{ox}), resulting in an underestimate of negative-bias temperature instability (NBTI) degradation. This can be attributed to the electrons tunneling from the process-induced partial n^+ poly gate and anode electron injection (AEI) model, rather than the electron valence band tunneling (EVB) widely accepted as the mechanism for n-MOSFETs. And then, the second part shows that the strained FB device has less NBTI degradation than the unstrained devices. This behavior can be attributed to the fact that more electron accumulation was induced by strain-induced band gap narrowing, reducing NBTI significantly.
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1. Introduction

Even silicon-on-insulator (SOI) CMOS devices are attractive for switching application because of their high speed, lower power dissipation, and the ability to restrain latch-up, SOI devices has some critical issues leads instabilities such as floating body (FB) effect. For partially depleted (PD) SOI devices, due to their relatively thick thin films, the impact ionization mechanism near the drain will cause the ionization charges to accumulate in the neutral region, leading to the instability of body potential [1]. With aggressive scaling of the gate oxide, the floating-body (FB) potential is controlled not only by well known impact ionization mechanisms but also by a gradual increase of the tunneling current. This new FB effect, called gate-induced-FB-effect (GIFBE), has been observed in both PD SOI MOSFETs [2,3] and fully depleted transistors [4]. However, the origin of these electrons is not clear yet due to the fact that the electron concentration is insufficient in the p^+ poly gate of p-MOSFETs. To the best of our knowledge, several studies consider that the model of electron valence band (EVB) tunneling should be responsible for the GIFBE in SOI n-MOSFETs [2–4]. But, the new mechanism for SOI n-MOSFETs has been reported which demonstrates the GIFBE is due to impact ionization, named anode hole injection (AHI) [5–7]. As devices turn on, inversion layer supplies carriers to result in gate tunneling current, generating electron–hole pairs due to impact ionization within poly gate depleted region. Therefore, ionization-induced holes tunnel back toward active layer and gather at body to attribute to GIFBE.

However, there are a few studies confirming the validity of EVB-induced GIFBE for p-MOSFETs. Therefore, the aim of this work is to clarify the origin of electrons on the GIFBE in PD SOI p-MOSFETs by adopting systematical operation conditions. The experimental results reveal that the GIFBE in p-MOSFETs can be partially attributed to the process-induced partial n^+ poly gate of body tied devices. However, the major electron source generated by NBTI stress is significantly related to the inversion channel supplied from the source and drain, and then reducing NBTI due to lower oxide electric field [8–10]. Therefore, GIFBE in SOI p-MOSFET is dominated by the anode electron injection (AEI) model which is similar to the anode hole injection (AHI) [5] in this work, to explain how this main electron origin is generated during NBTI. In detail, AEI is a mechanism which is associated with S/D. As channel invert, channel holes come from S/D could leak toward gate by tunneling, and then inducing electron–hole pairs. After that, impact-induced electrons can tunnel back to channel again, leading floating body effect (FBE). In addition, strained silicon technique offers an alternative method to enhance

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the SOI performance as devices are scaled down below 90 nm, requiring increase in channel doping [11]. Therefore, the use of strained silicon technique offers an alternative method to enhance the SOI performance through an increase in channel mobility. According that, to comprehend the influence of the strain effect on GIFBE seems to be necessary and interested. In this part, the mechanical strain effect on GIFBE was observed from NBTI behavior. It can be found that the GIFBE becomes significant under mechanical strain which is obtained from a decreasing NBTI behavior. This paper investigates the GIFBE for PD SOI p-MOSFETs in first part, and discussing the impact of strain on GIFBE by analysis of NBTI behavior secondly.

2. Experiment

Using 65-nm SOI CMOS technology, partially depleted SOI p-channel metal–oxide–semiconductor field-effect transistors (PD SOI p-MOSFETs) with p^+ poly-Si gate are produced in a T-gate structure. The SOI film and buried oxide thicknesses are 75 and 145 nm, respectively. The gate oxide has a thickness of 12 Å, and the channel doping concentration is about 3×10^{18} cm^{-3}. The channel is along the <110> direction on the (100) substrate. In this letter, devices have channel lengths (L) of 0.2 μm and widths (W) of 1.0 μm. A stress gate voltage of -1.8 V$+V_{th}$ was applied to the gate electrode at 125 °C for NBTI, while the source and drain were grounded. The threshold voltage (V_{th}) was defined as the maximum of transconductor (G_{mmax}) in the linear region. All electrical characteristics were measured using an Agilent B1500 semiconductor parameter analyzer.

3. Result and discussion

3.1. Part I: gate-induced-floating-body-effect (GIFBE) on PD SOI p-channel MOSFETs

Fig. 1 shows the NBTI-induced threshold voltage (V_{th}) shift versus time for the PD SOI p-MOSFET FB (floating body) and GB (grounded body) devices. It can be seen that the FB device has less shift than GB device significantly. This is because electrons accumulate at body terminal to make the oxide electric field (E_{ox}) lowering effectively during stress, therefore reducing NBTI degradation. The gate current is shown in the inset of Fig. 1, which also decreases simultaneously, evidencing the restrain of E_{ox}. To examine these additional carriers, Fig. 2(a) shows the I_D–V_G and G_m–V_G at $V_D=-0.05$ V. It can be observed that the V_{th} shifts toward left and G_m enhances under linear region which seems FB effect behavior. We suggest that the accumulation of elections result from gate-induced-floating-body-effect (GIFBE), since the thickness of gate oxide as thin as inducing the leakage current by tunneling.

Furthermore, Fig. 2(b) shows the gate current (I_G) and the body current (I_B) versus the gate voltage (V_G) for different areas of p^+ poly gate (1–0.2 μm^2), while the source/drain (S/D) and body are grounded. It can be seen that I_B enhances as I_G increases, which means the original source of I_B is associated with I_G strongly. In addition, regardless of the different areas of poly gate, I_B always shows a linear increase until $V_G=-1$ V, after that shows an exponential increase as $V_G<-1$ V. This phenomenon exhibits that the mechanisms closely related to the gate leakage current should be the attribution for these two stages of I_B, leading the GIFBE. In order to analyze those body current, it has been reported that gate leakage consists of the following three components as shown in the inset of Fig. 2, including 1) hole tunneling from the valence band (HVB), 2) electron tunneling from the valence band (EVB) and 3) electron tunneling from the conduction band (ECB). Both components of ECB and EVB can be observed from the body terminal, which seem to contribute on the two stages of I_B, respectively. The ECB first occurs as a gate bias is applied. And then, as the V_G is large enough, the EVB should induce additional electrons, resulting in the second stage of I_B. Additional, due to the negligible electron concentration in the p^+ poly gate, there are insufficient electrons to supply since the doped type of gate is p^+. Therefore, it is impossible for ECB to occur from poly-gate and result in the significant increase in I_B as V_G is applied. The possible region providing sufficient electrons can be attributed to the partial n^+ poly gate area of body-tied SOI devices. By cutting the T-gate structure along A–A′, a cross-sectional structure can be obtained and is shown in the inset of Fig. 3. It can be observed that part of the poly gate near the body contact has been covered by an n^+ doped. Therefore, the ECB becomes significant between the n^+ section of the poly gate and the n substrate when V_G applying,

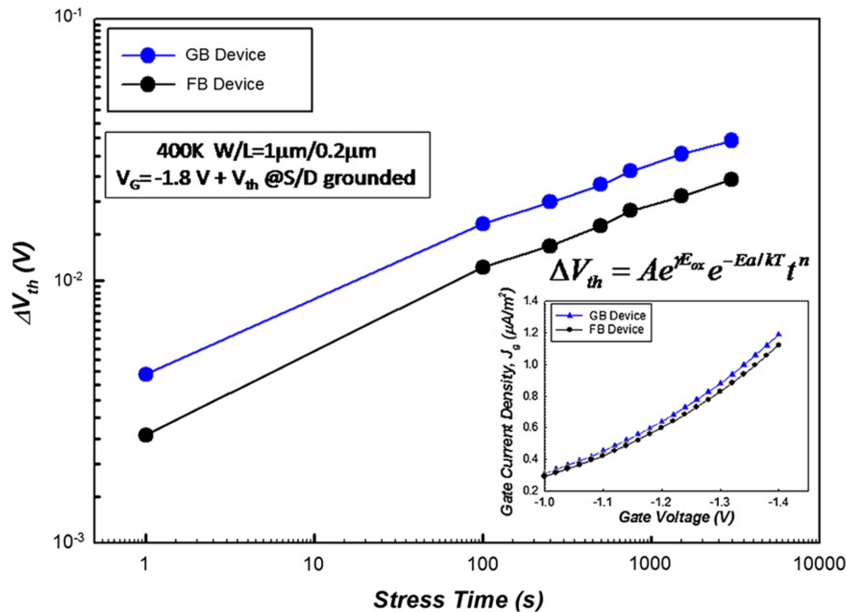

Fig. 1. NBTI-induced threshold voltage shift versus stress time for SOI p-MOSFETs under GB and FB operations. The inset shows the gate current comparison of GB and FB devices.

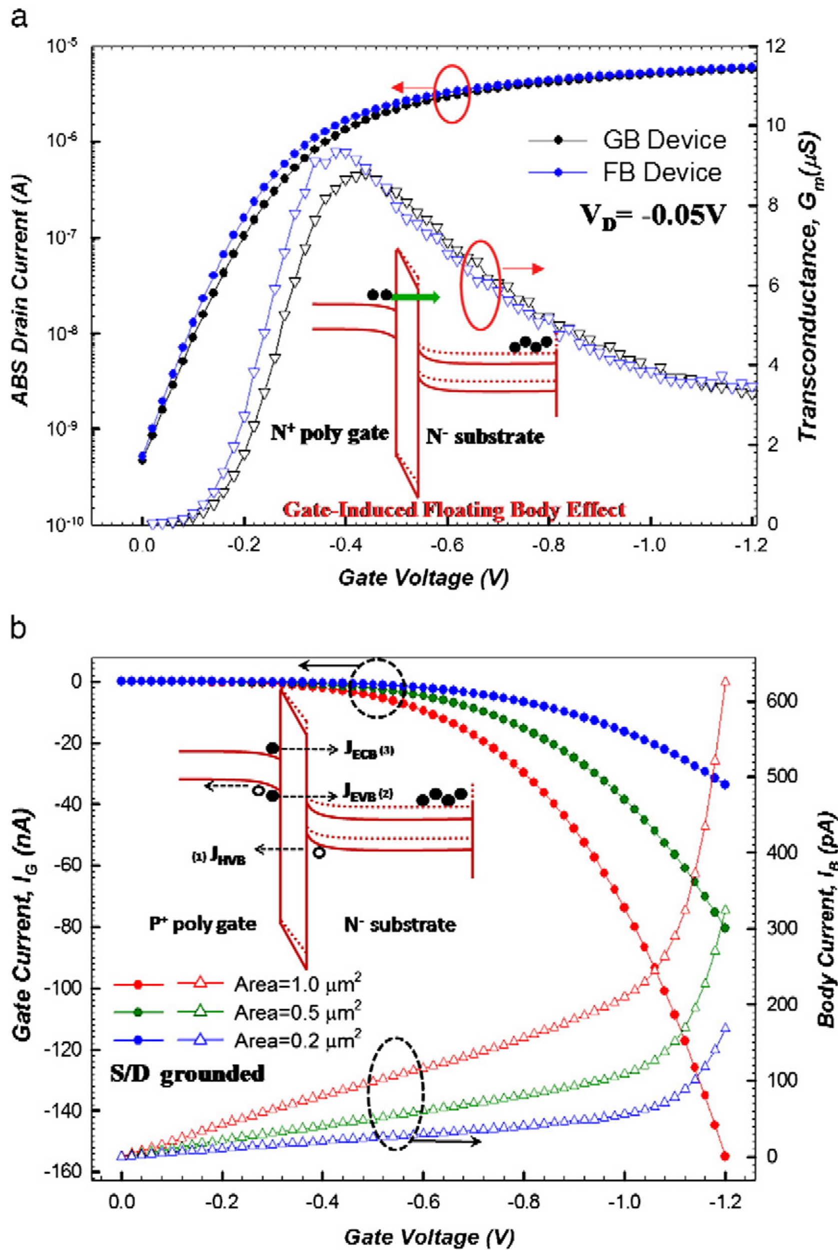

Fig. 2. (a) I_D–V_G characteristic and corresponding G_m–V_G under GB and FB operations. (b) I_G–V_G and I_B–V_G curves for different p^+ poly gate areas. The inset shows the schematic diagrams of the different gate tunneling mechanisms in ultra thin gate oxide p-MOSFETs.

resulting in a gradual increase of I_B. This can be demonstrated completely by variation the device of widths (W) and lengths (L) during I_B and I_G measurement, since the amount of current density should be related to cross section of current flux, meaning the area of n^+ poly gate. Fig. 3 shows the I_B and I_G at $V_G = -0.5$ V with different W/L for PD SOI p-MOSFETs. The experimental data indicates that the first stage of I_B illustrates only linear dependence with L, rather than W. On the other hands, the cross section of current flux does change with L, instead of W, which proves that these electrons are tunneling from the n^+ poly gate, corresponding to the green area in the top view of PD SOI p-MOSFETs with a T-gate structure. After that, there is another origin to cause the FB effect at linear region which indicates the exponentially increasing I_B at $V_G < -1$ V (second stage of I_B). According to the I_G tunneling model we mentioned, this could be caused by the EVB mechanism, as shown in the inset of Fig. 2(b). Under a sufficiently large vertical electric field (V_G), electrons tunnel from the valence band (E_V) of the poly-Si gate to the conduction band (E_C) of channel (Si substrate). However, it has been reported that EVB only occurs as the V_G applying exceeds -1.1 V to separate the band structure with ultra thin insulator. Thus, carriers have a probability to conduct by tunneling. Nevertheless, we would like to propose another possible that is similar to the AHI model, i.e., that of AEI, shown in Fig. 4(a), to explain the second stage of I_B. The AEI mechanism comes if the gate oxide is thin enough, holes can still tunnel from the inversion layer to the poly gate (anode) and generate hot electrons by impact ionization in the poly gate depletion region under higher V_G. Then, these hot electrons could tunnel insulator directly or overcome the barrier height of oxide to traverse toward the body (cathode). To confirm the strength of this mechanism, there are two operations are introduced into

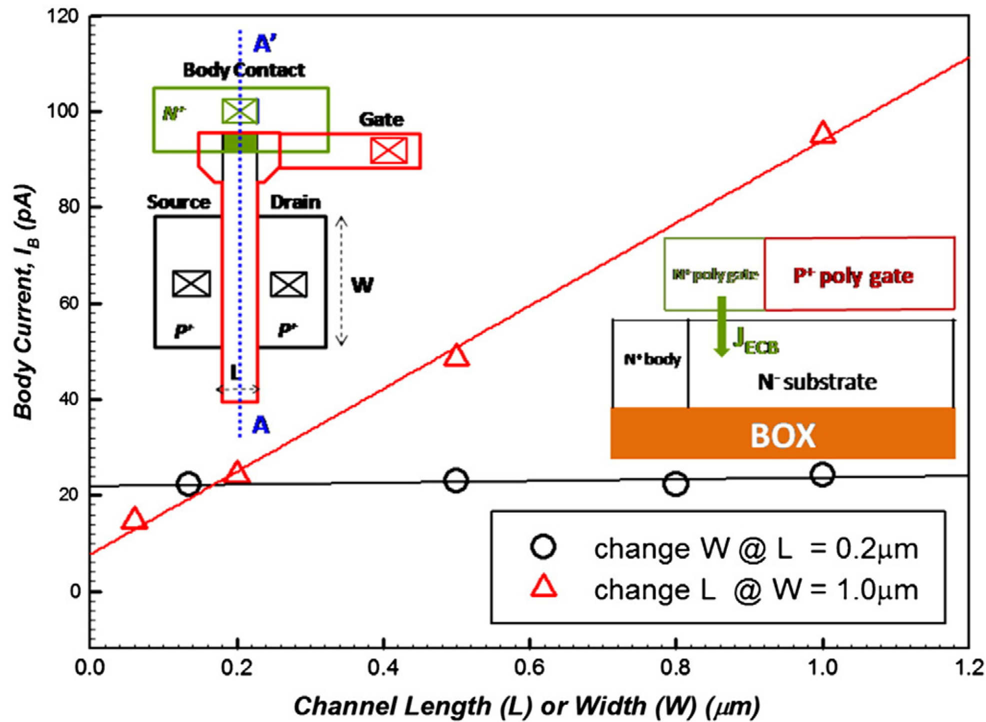

Fig. 3. I_B for various W and L dimensions. I_B is obtained from the gate voltage of −0.5 V while S/D is grounded. The inset shows the cross-sectional view taken from line A–A′ in the top view of the T-gate structure, illustrating the p^+ poly gate, the partial n^+ poly gate, and the n^- substrate, and it's top view of the T-gate structure.

distinguishing the different origins of I_G, resulting in the accumulation of electron. The I_G and I_B versus V_G of the device under floating and grounded S/D operations have been measured. In Fig. 4(b), the results show the I_B and I_G are insignificant with S/D floating, but I_B is increasing related to I_G as S/D ground. It can be clearly seen that the gate leakage current becomes deficient because the S/D cannot supply sufficient minority carriers (holes) to the inversion layer. Additional, the I_B exhibits only the linear component (first stage) of the ECB as discussed previous. On the contrary, under grounded S/D operation, I_G shows an obvious increase, and the second stage of I_B occurs simultaneously. This proves that the exponential increase of I_B can be attributed to the holes comes from the S/D as inversion layer produces rather than the electron–hole pair separated in the E_V of the p^+ poly gate. This relationship is consistent with that in the AHI model, which implies that AEI indeed exists and is the dominant mechanism of the GIFBE in PD SOI p-MOSFETs.

3.2. Part II: influence of mechanical strain on gate-induced-floating-body-effect (GIFBE) in PD SOI p-channel MOSFETs through NBTI reliability

Furthermore, to introduce the mechanical strain into the investigation of GIFBE on PD SOI p-MOSFETs, the second part will discuss the impact of strain on GIFBE by NBTI analysis. Fig. 5 shows the NBTI-induced threshold voltage (V_{th}) shift versus time for the PD SOI p-MOSFET FB and GB devices with strain and unstrain and the illustration of bending sample as shown in the inset of Fig. 5. For unstrained devices, it can be seen that the FB device has more insignificant degradation than the GB devices, which has been explained early. For strained devices, the NBTI reliabilities of FB and GB devices are all improved under strained operation. In addition, Fig. 5(b) shows a nearly unchanged thermal activation energy (E_a) of NBTI with strain (~0.085 eV). Also, it can be observed that the V_{th} shift versus time shows a similar slope under logarithmic scale, meaning the time-power law owns a close exponential value (n~0.24). This suggests that the strain does not change the NBTI mechanism itself, but only change the degradation level of NBTI. Therefore, the reduction of NBTI under strained operation should be attributed from effectively E_{ox} lowering. However, there are two different physical mechanisms to reduce E_{ox} during NBT stress for FB and GB devices as strain was introduced. Fig. 6(a) shows the I_G for GB device with strained and unstrained operations. The slight decrease of I_G is found under compressive strain, showing that the compressive strain can reduce E_{ox} effectively. As compressive strain is applied, the light hole band (LH) is separated from two-fold degeneration and transfers a lower energy state of hole. Therefore, there are amounts of hole that tend to stay with the LH band which result to a larger barrier height of E_V, leading to a reduction of tunneling probability, and the illustration of band diagram is shown on the inset of Fig. 6(a). Additionally, the results of theoretical calculations have shown that the effective mass of hole indeed becomes large under uniaxial compressive strain [12]. According to those, the reduction of I_G under uniaxial compressive strain due to higher barrier height and larger effective mass can diminish the penetration probability of hole [13], suppressing the generation of interface states during NBTI. However, it can be seen that the FB device has a significantly less degradation than GB device under compressive strain. This is because the GIFBE becomes more obvious since I_B increase under compressive strain as shown in Fig. 6(b). As the result, it can be seen that the I_B curve of strained device is larger than the unstrained one not only in the first stage where is the tunneling current from n^+ poly gate by ECB but also within the second stage which is result from AEI. In order to comprehend the increase in I_B under first stage, the I_B with S/D floating for strained and unstrained GB devices is measured as shown in Fig. 7(a). The strained I_B with S/D floating enhances as V_G increases, since strain-induced band gap narrowing results more electron–hole pairs. As electrons tunnel form n^+ poly gate to channel, the potential difference can make electrons to gain enough energy, ionizing the stable Si-bond, therefore generating electron–hole pairs. Further

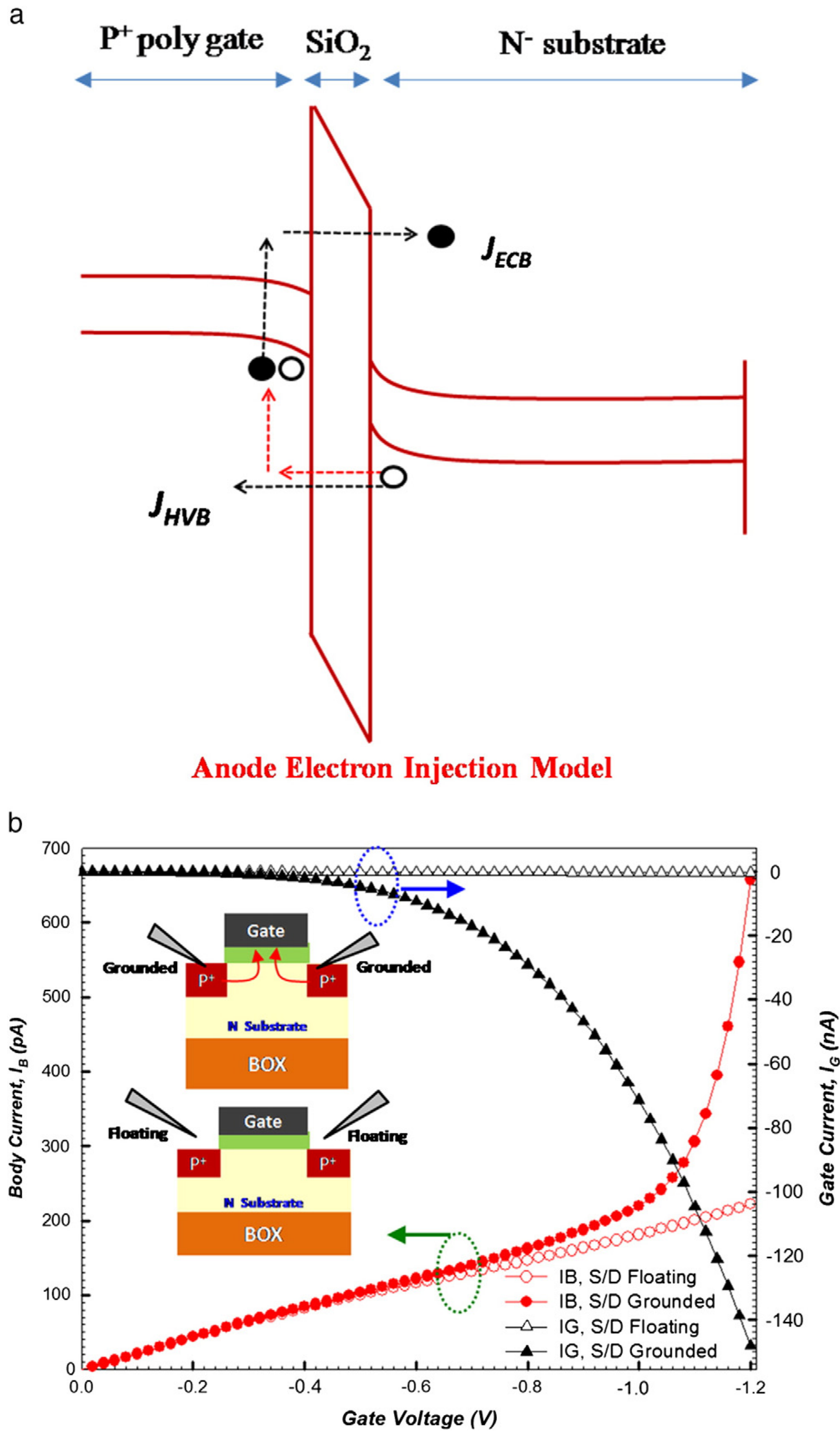

Fig. 4. (a) The energy diagram of the AEI model for an ultrathin gate oxide in PD SOI p-MOSFETs. (b) I_G–V_G and I_B–V_G characteristics for PD SOI p-MOSFETs under S/D floating and grounded operations. The inset shows the corresponding measurement method.

then, the second stage I_B also increases under strain operation as shown in Fig 6(b). As we mentioned, the second stage I_B is attributed to the AEI model which is associated with the amount of channel carriers and tunneling current. Generally, I_G is decreased since higher barrier height and larger effective mass as shown in Fig. 6(a), therefore the AEI-induced I_B current should be suppressed. However, the

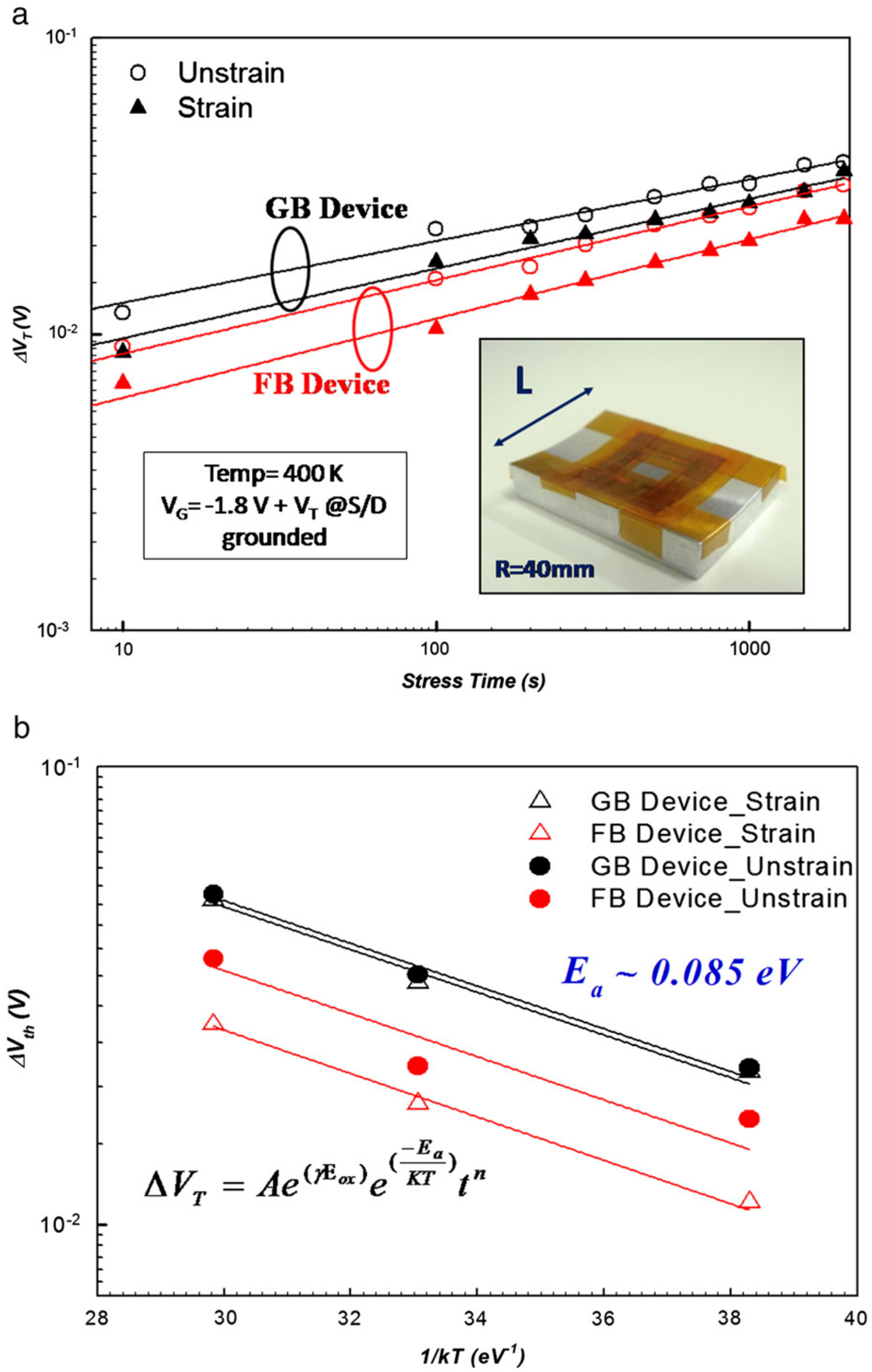

Fig. 5. (a) Time evolution of threshold voltage shift in SOI PD p-MOSFETs for FB and GB devices with unstrained and strained. The inset shows an illustration of bending sample and a body current comparison of devices with compressive strain and unstrained. (b) Temperature dependence of threshold voltage shift of devices with compressive strain and unstrained, with activation energy extracted from the power law with time under NBTI.

strain effect increases the effective I_B, especially over $V_G = -1$ V, which may be related to the first stage increase of I_B. To clearly distinguish the contribution of the strain effect on the second stage of I_B, the pure AEI-induced electron current (effective I_B) was also obtained, as shown in Fig. 7(b), by subtracting the ECB tunneling component from the second increase of I_B. This unusual phenomenon is caused by the band gap narrowing induced by the mechanical strain effect. Because the impact ionization rate is exponential to the energy band gap, the narrowing band gap induces more additional electron generation in the poly depletion region by impact ionization even though I_G decreases. Moreover, the decrease in penetration probability of hole, the additional improvement on NBTI reliability for strained FB device can be attributed to the significant GIFBE, lowering the oxide electric field by more electrons accumulate at body.

4. Conclusion

This work investigates the impact of mechanical strain on GIFBE for partially depleted silicon-on-insulator p-type metal–oxide–

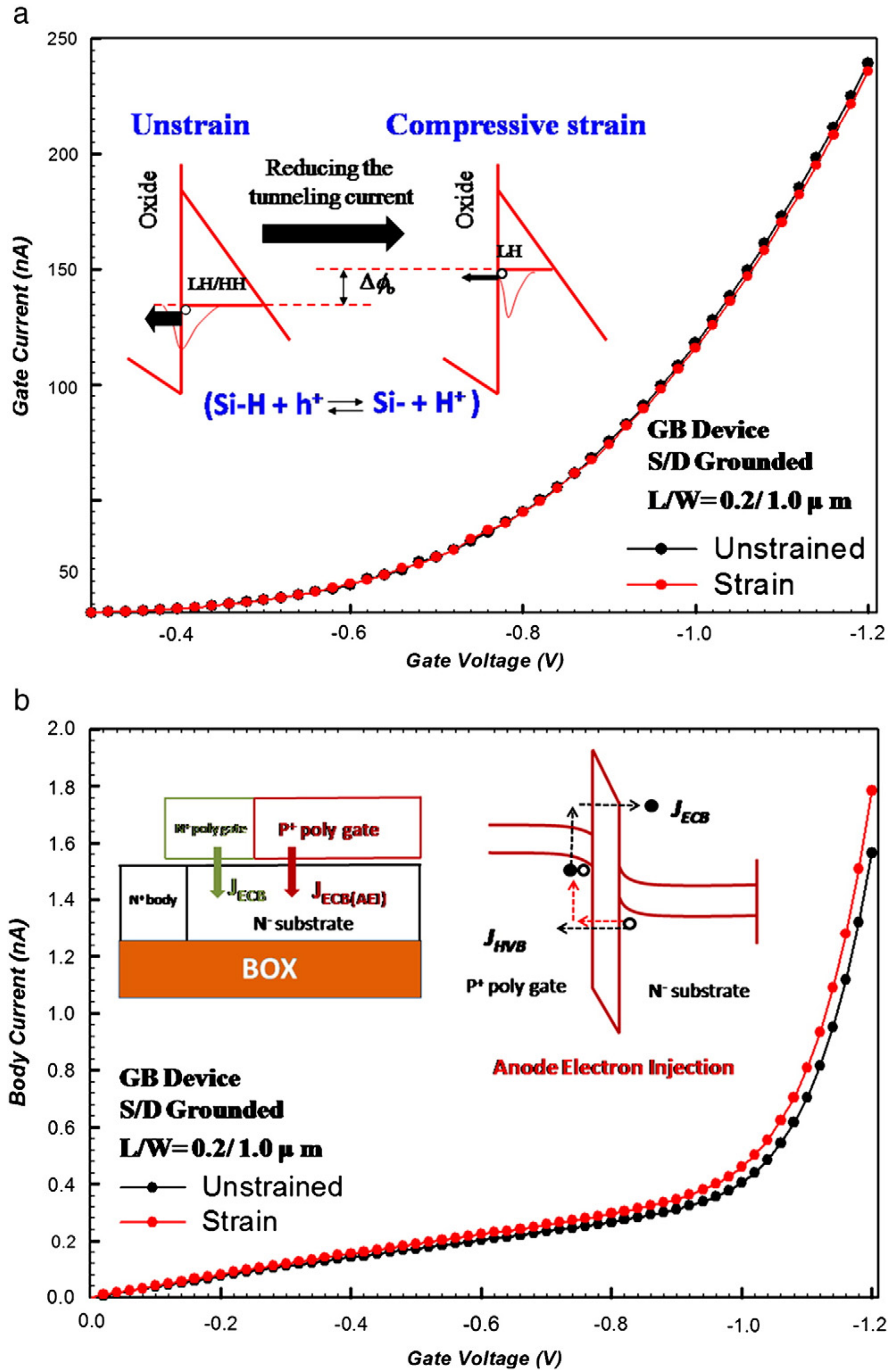

Fig. 6. (a) I_G–V_G characteristics for PD SOI p-MOSFETs with compressive strain and unstrained. The inset shows an illustration of variation of valance band diagram before and after compressive strain. (b) The body current with S/D grounded for GB devices with compressive strain and unstrained. The inset shows the gate current (source current + drain current) for GB devices with compressive strain and unstrained.

semiconductor field effect transistors (PD SOI p-MOSFETs). First part, we demonstrate the original mechanism of GIFBE on PD SOI p-MOSFETs results from the electrons tunneling from the process-induced partial n^+ poly gate and AEI model, rather than the EVB. In addition to, the second part shows that the strained FB device has less NBTI degradation than the unstrained devices. This behavior can be attributed to the fact that more electron accumulation induced by strain effect reduces the E_{ox} significantly during NBTI stress. This is because strain-induced band gap narrowing increases impact ionization rate to generate additional electrons, reducing NBTI.

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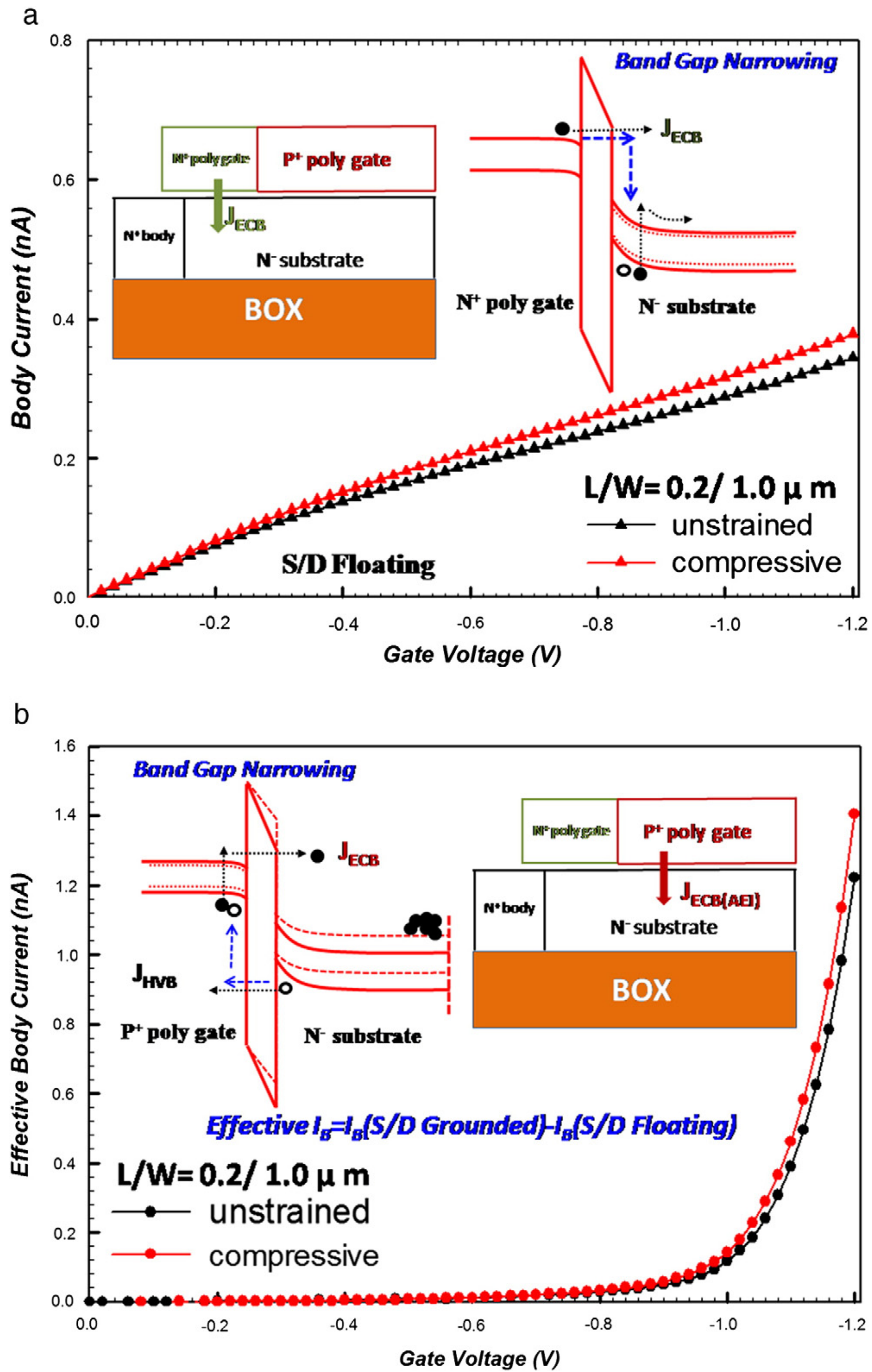

Fig. 7. (a) I_B–V_G curves with floating S/D for strained and unstrained GB devices. The inset shows the schematic diagram of electrons tunneling from conduction band (ECB) from the partial n^+ poly gate for an ultra thin gate oxide in PD SOI p-MOSFETs and a cross section of the device. (b) Comparison of effective body current versus gate voltage for compressive strained and unstrained devices. The inset shows the cross section and the schematic diagram of AEI mechanism under strain.

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