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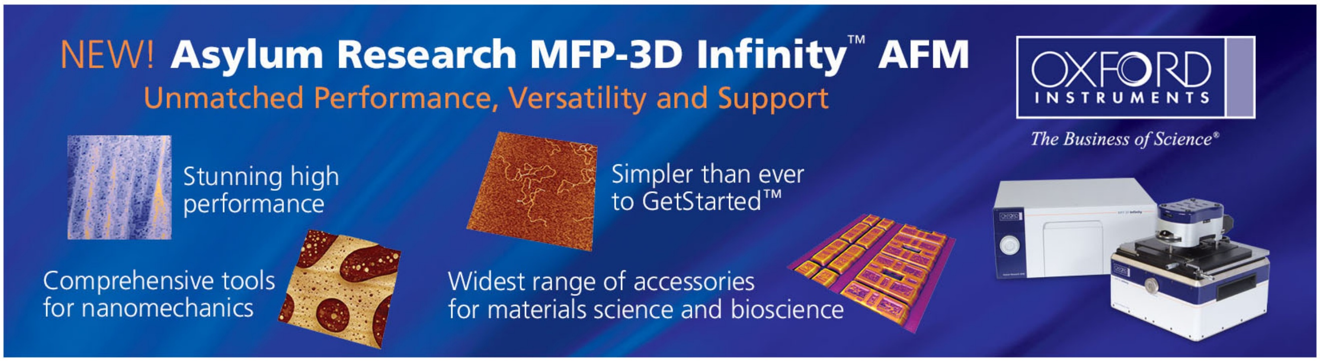

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Investigation of an anomalous hump in gate current after negative-bias temperature-instability in HfO_2/metal gate p-channel metal-oxide-semiconductor field-effect transistors

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This Letter investigates a hump in gate current after negative-bias temperature-instability (NBTI) in HfO_2/metal gate p-channel metal-oxide-semiconductor field-effect transistors. Measuring gate current at initial through body floating and source/drain floating shows that hole current flows from source/drain. The fitting of gate current (I_g)-gate voltage (V_g) characteristic curves demonstrates that the Frenkel-Poole mechanism dominates the conduction. Next, by fitting the gate current after NBTI, in the order of Frenkel-Poole then tunneling, the Frenkel-Poole mechanism can be confirmed. These phenomena can be attributed to hole trapping in high-k bulk and the electric field formula $E_{\text{high-k}}\,\varepsilon_{\text{high-k}} = Q + E_{sio2}\varepsilon_{sio2}$. *© 2013 American Institute of Physics*. [http://dx.doi.org/10.1063/1.4773479]

With the scaling down of metal-oxide semiconductor field-effect transistors (MOSFETs), conventional SiO_2-based dielectric is only a few atomic layers thick, causing gate current to rise, power dissipation to increase, and performance to degrade. Besides, conventional SiO_2-based dielectrics have approached their physical limits. Hence, replacing SiO_2-based dielectrics with high-k based dielectrics is a valid solution to these problems. In addition, high-k/metal gates can be integrated with techniques, such as silicon on insulator (SOI),[1–3] strained-silicon,[4,5] and multi-gate to improve device characteristics. As recommended in the International Technology Roadmap for Semiconductors, Hf-based dielectrics have been heavily studied to replace SiO_2-based dielectrics in recent years.[6–9] In reliability, negative-bias temperature-instability (NBTI) is still a significant concern for digital and analog circuits in current generation CMOS technology. In the past, NBTI degradation was dominated by an increase in the SiO_2/Si interface traps, which released hydrogen.[10–12] However, bulk traps have dominated NBTI degradation in sub-1 nm-EOT devices in recent years due to hole trapping.[13] In this paper, this phenomenon is also observed. Nevertheless, I_g-V_g simultaneously generates an unusual hump with NBTI. Thus, this study focuses mainly on an analysis of gate current for HfO_2 dielectric p-MOSFETs undergoing NBTI. The causes of the hump are explained in this Letter.

The HfO_2/metal gate p-MOSFETs used in this study were fabricated through the gate-last process. First, high quality thermal oxide of 1 nm thickness was grown as an interfacial layer. Second, HfO_2 dielectrics were deposited in that order by atomic layer deposition (ALD). Then, after annealing, HfO_2 with thickness of 2 nm was formed. This process may be crystallized into monoclinic crystal structure.[14,15] Finally, Ti_xN_{1-x} was deposited by physical vapor deposition (PVD) due to the ability of metal gates to eliminate gate depletion and resist remote phonon scattering.[16,17] The p-MOSFETs were stressed in Vt = 1.8 V at 30 °C and 125 °C. I_d-V_g transfer curves were measured with V_d given by −50 mV and V_g given from 0 V to −1.3 V during NBTI at 30 °C and 125 °C. Then, I_g-V_g transfer curves were measured at 30 °C only with V_g given from 0 V to −1 V before and after NBTI (30 °C or 125 °C). Then, through the body floating (BF) and source/drain floating (SDF) process, the current path and carrier polarity can be confirmed. Next, the I_g-V_g curve is fitted by Frenkel-Poole mechanism and tunneling mechanism at 0 s and 1000s NBTI, respectively. All experimental curves were measured using an Agilent B1500 semiconductor parameter analyzer.

Figures 1(a) and 1(c) show the I_d-V_g transfer characteristic curves with −50 mV drain voltage under NBTI for 1000s at 30 °C and 125 °C. Clearly, on-current are both degraded and V_t shifts 87 mV and 204 mV in the negative direction at 1000s NBTI at 30 °C and 125 °C, respectively. Furthermore, subthreshold swing degradation is slight. Thus, V_t shift can be attributed mainly to hole trapping in the high-k bulk. Figures 1(b) and 1(d) shows I_g-V_g transfer characteristic curves at 30 °C before and after NBTI at 30 °C and 125 °C, respectively. Obviously, the slight gate current hump appears after NBTI in 30 °C due to a smaller degradation in Vt (87 mV), as shown in the inset of Fig. 1(b). Conversely, the gate current hump is clearer after NBTI in 125 °C owing to a larger degradation in Vt (204 mV), as

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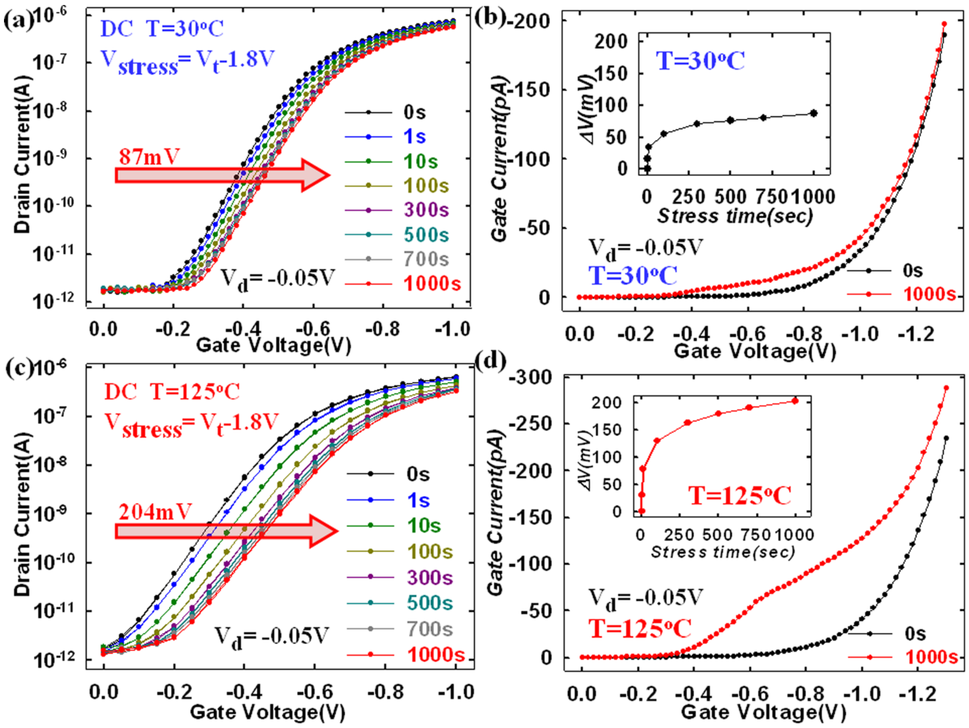

FIG. 1. (a) I_d-V_g and (c) I_d-V_g transfer characteristic curves with −50 mV drain voltage as function of stress time under NBTI at 30 °C and 125 °C. (b) $I_g–V_g$ and (d) $I_g–V_g$ transfer characteristic curves at 30 °C before and after NBTI in 30 °C and 125 °C.

shown in inset of Fig. 1(d). Therefore, the clearer the hump generated, the more hole trapping, which occurs in high-k bulk.

To further understand the causes of the hump, fitting and distinguishing gate current are necessary. Figure 2(a) shows I_g-V_g characteristics with BF, SDF, and source/drain/body all grounded (SDB). Obviously, the I_g-V_g characteristic in BF is similar to that in SDB, and the I_g-V_g characteristic in SDF is much smaller than those in either SDB or BF. These results indicate that holes transfer from source/drain to the gate, rather than electrons transferring from gate to body. Moreover, gate current is fitted under initial, shown in Fig. 2(b), where it can be observed that gate current is confirmed as Frenkel-Poole mechanism, from $V_g = -0.98$ to $V_g = -1.3$. These results show that holes transfer from source/drain to gate with the Frenkel-Poole mechanism at initial.

After confirming Frenkel-Poole mechanism at initial, the I_g-V_g characteristic is fitted after 1000s NBTI at 125 °C, as shown in Fig. 3(a). Clearly, section A indicates the Frenkel-Poole mechanism in Fig. 3(b), from $V_g = -0.50$ to $V_g = -0.62$, while section B is the tunneling mechanism in Fig. 3(c), from $V_g = -0.68$ to $V_g = -0.78$, and section C is again Frenkel-Poole mechanism in Fig. 3(d), from $V_g = -1.2$ to $V_g = -1.3$. In addition, in the $V_g < V_t = -0.83$ V situation, Frenkel-Poole mechanism transfers to tunneling mechanism with V_g increasing. On the contrary, tunneling mechanism transfers to Frenkel-Poole mechanism when $V_g > V_t$. Frenkel-Poole current and tunneling current are a series; whichever current is smaller dominates the current path. Therefore, Frenkel-Poole mechanism dominates current path because $J_{\text{Frenkel-Poole}} \ll J_{\text{Tunneling}}$ while tunneling mechanism dominates current path when $J_{\text{Frenkel-Poole}} \gg J_{\text{Tunneling}}$. Therefore, the conditions under which a hump is generated are $J_{\text{Frenkel-Poole}} \gg J_{\text{Tunneling}}$.

Figures 4(a) and 4(b) shows energy diagrams for $V_g = 0$ V without hole trapping and with hole trapping due to NBTI, respectively. Note that $E_{\text{high-k}}$ becomes large, and E_{SiO2} reduces with hole trapping. An increase in $E_{\text{high-k}}$ produces a larger Frenkel-Poole current, and a reduction in E_{SiO2} produces a larger ΔE_{trap}, causing tunneling current to decrease. ΔE_{trap} indicates the energy from the valance band in the surface to trap level. Therefore, with hole trapping increasing, $J_{\text{Frenkel-Poole}}$ is larger than $J_{\text{Tunneling}}$. In addition, since the hump generation condition is $J_{\text{Frenkel-Poole}} \gg J_{\text{Tunneling}}$, hole trapping leads to a more significant hump. In Figs. 1(b) and

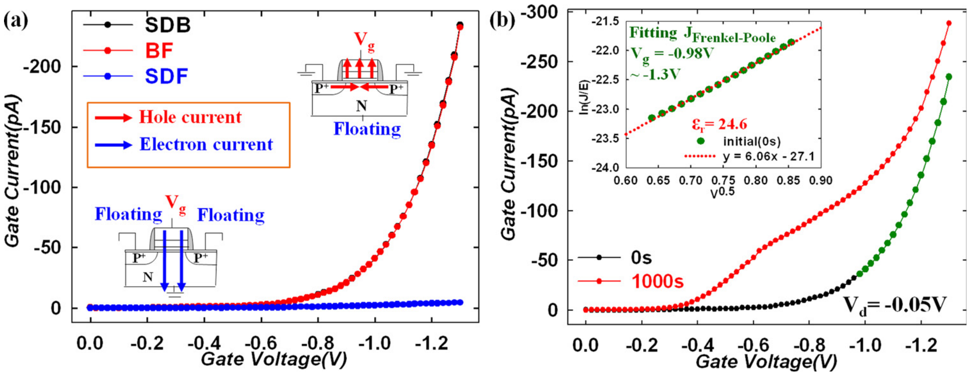

FIG. 2. (a) I_g-V_g characteristic curves in the SDB, BF, and SDF conditions. (b) I_g-V_g transfer characteristic curves of high-k/metal gate MOSFETs under initial and after NBTI at 125 °C. Inset shows gate current is fitted by Frenkel-Poole mechanism at initial.

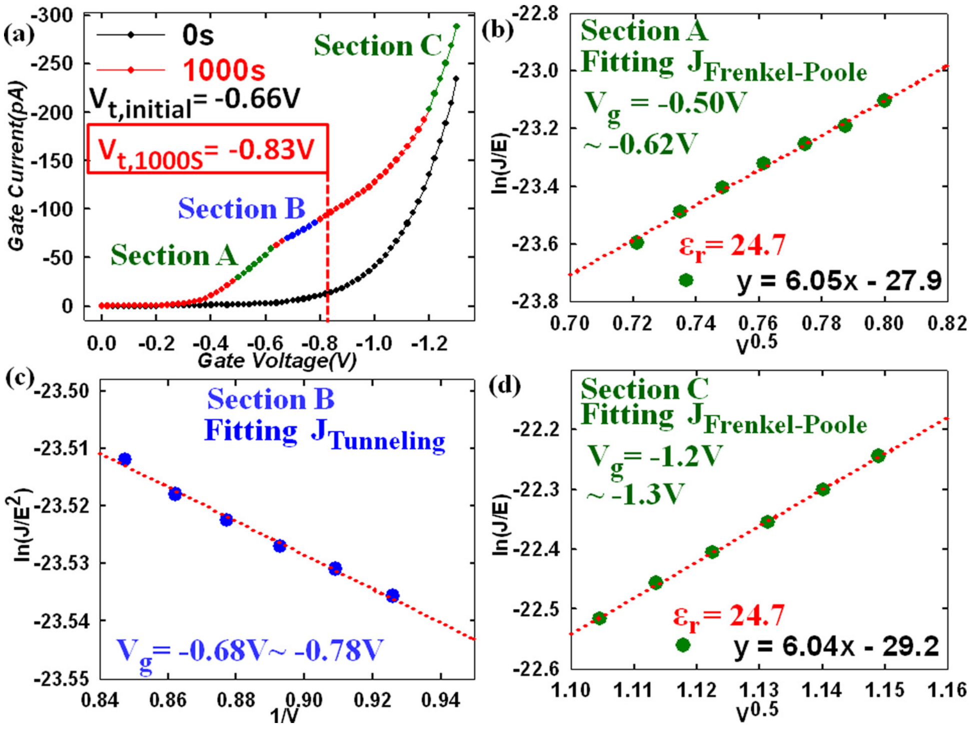

FIG. 3. (a) I_g–V_g transfer characteristic curves at initial and after NBTI in 125 °C. (b) Gate current in section A is fitted by Frenkel-Poole mechanism after NBTI at 125 °C. (c) Gate current in section B is fitted by tunneling mechanism after NBTI at 125 °C. (d) Gate current in section C is fitted by Frenkel-Poole mechanism after NBTI at 125 °C.

1(d), it can be observed that the more hole trapping that is captured in high-k bulk, the clearer the gate current hump we can observe. Figure 4(c) shows energy diagrams in the $V_g < V_t$ situation with hole trapping. The electric field must follow the formula $E_{high\text{-}k}\,\varepsilon_{high\text{-}k} = Q + E_{sio2}\,\varepsilon_{sio2} = (Q/E_{sio2} + \varepsilon_{sio2})\,E_{sio2} = \varepsilon'\,E_{sio2}$, where Q indicates the quantity of hole trapping ($Q > 0$), E_{sio2} indicates an electric field in the SiO_2, and $E_{\ high\text{-}k}$ is an electric field in the high-k bulk. The voltage across gate oxide is small when $V_g < V_t$. Hence, $Q/E_{\ sio2}$ cannot be ignored ($Q \gg E_{sio2}$). This result makes $\varepsilon_{high\text{-}k} < \varepsilon'$ and $E_{high\text{-}k} > E_{sio2}$. When V_g is swept from 0 V to V_t on the device with a large amount of hole trapping in high-k bulk, most of the applied gate voltage occurs across in the HfO_2 layer. This is the reason why $J_{Frenkel\text{-}Poole}$ after NBTI appears earlier than $J_{Frenkel\text{-}Poole}$ under initial. Nevertheless, a relatively smaller voltage occurs across in the SiO_2 layer, leading to a slight rise in $J_{Tunneling}$ due to a small variation in ΔE_{trap}. With an increase in V_g, $J_{Frenkel\text{-}Poole}$ increases significantly while $J_{Tunneling}$ changes only slightly. This causes $J_{Frenkel\text{-}Poole}$ to change to $J_{Tunneling}$. At the beginning stages, $J_{Frenkel\text{-}Poole}$ appears in section A (Fig. 3(a)) owing to the supply of holes exceeding the demand ($J_{Tunneling} \gg J_{Frenkel\text{-}Poole}$). Next, $J_{Tunneling}$ appears in section B (Fig. 3(a)) because the supply of holes is unable to meet the demand ($J_{Tunneling} \ll J_{Frenkel\text{-}Poole}$). Figure 4(d) shows energy diagrams in the $V_g > V_t$ condition with hole trapping. The electric field should also obey the formula $E_{high\text{-}k}\,\varepsilon_{high\text{-}k} = Q + E_{sio2}\,\varepsilon_{sio2} = (Q/E_{sio2} + \varepsilon_{sio2})\,E_{sio2}$. On the contrary, V_g applied to SiO_2 and HfO_2 in the $V_g > V_t$ condition is large, causing Q/E_{sio2} to be ignored ($Q \ll E_{sio2}$). This result leads to $\varepsilon_{high\text{-}k} > \varepsilon_{sio2}$ and $E_{high\text{-}k} < E_{sio2}$. Therefore, with V_g increasing, ΔE_{trap} decreases, and $J_{Tunneling}$ increases sharply due to the exponential dependence on ΔE_{trap}. This is the reason why $J_{Tunneling}$ changes to $J_{Frenkel\text{-}Poole}$. Finally, $J_{Frenkel\text{-}Poole}$ appears in section C (Fig. 3(a)), since the supply of holes exceeds the demand ($J_{Tunneling} \gg J_{Frenkel\text{-}Poole}$).

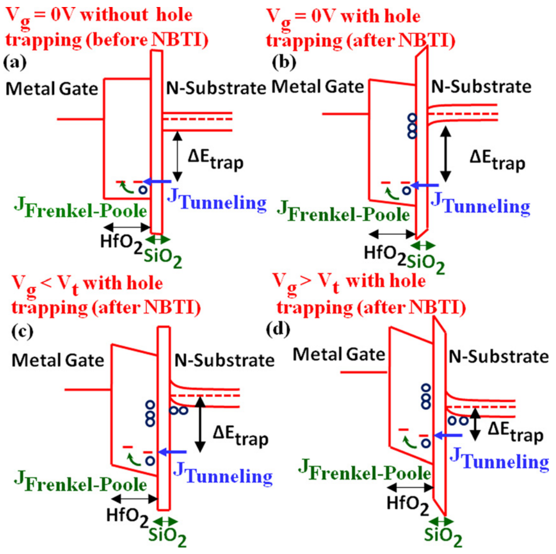

FIG. 4. The energy band diagram of high-k/metal gate MOSFETs in the $V_g = 0$ V condition (a) without hole trapping before NBTI and (b) with hole trapping due to NBTI. (c) The energy band diagram of high-k/metal gate MOSFETs in the $V_g < V_t$ condition with hole trapping due to NBTI. (d) The energy band diagram of high-k/metal gate MOSFETs in the $V_g > V_t$ condition with hole trapping due to NBTI.

In summary, the V_t shifts 204 mV and 87 mV in the negative direction, and a hump is generated in the $I_g - V_g$ transfer characteristic curves after NBTI in 30 °C and 125 °C, respectively. These are results of hole trapping in high-k bulk. Through fitting and distinguishing gate current under initial, holes are determined to transfer through the Frenkel-Poole mechanism from the source and drain. Gate current fitting after NBTI at 125 °C indicates that $J_{Frenkel\text{-}Poole}$ changes to $J_{Tunneling}$ when $V_g < V_t$ owing to the influence of $E_{high\text{-}k} > E_{sio2}$, while $J_{Tunneling}$ changes to $J_{Frenkel\text{-}Poole}$ while $V_g > V_t$ due to the influence of $E_{high\text{-}k} < E_{sio2}$. These phenomena can be attributed to the fact that the electric field must follow the formula $E_{high\text{-}k}\,\varepsilon_{high\text{-}k} = Q + E_{sio2}\,\varepsilon_{sio2}$.

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