J Mater Sci: Mater Electron (2013) 24:376–381
DOI 10.1007/s10854-012-0761-2

Room temperature self-organized gold nanoparticles materials for embedded electronic devices

Chun-Chi Chen · Hsin-Chiang You · Edward Yi Chang · Fu-Hsiang Ko

Received: 26 March 2012 / Accepted: 12 May 2012 / Published online: 26 May 2012
© Springer Science+Business Media, LLC 2012

Abstract In this study, we synthesize two different sizes of gold nanoparticles (NPs) with uniform size distribution. A novel technique of fabricating gold NPs embedded capacitor devices utilizing chemical self-assembled gold NPs has been developed. Room temperature process and uniform size distribution of gold NPs device are built and characterized. These electronic devices have lower leakage current, no metal diffusion problem, larger memory window, better charge retention time and following Fowler–Nordheim tunneling model. This method enables the possibility of future memory applications to fabricate devices with this simple and versatile technique based on the NPs assembly.

1 Introduction

Metal materials shrinkage to nanostructures, especially noble metal nanoparticles (NPs) including gold, silver platinum and palladium, are of considerable interest for their applications in catalysis, batteries, fuel cells, capacitors and sensors. NPs, i.e. particles with structures approximately 1–100 nm in size, have significant impact in many scientific fields, including chemistry, material sciences, biology, medicine, and electronics [1]. The material, physical, and chemical properties of NPs are directly related to their intrinsic compositions, apparent sizes, and extrinsic surface structures; therefore, the design, synthesis, characterization, and applications of nanostructures are critical aspects for the emerging field of nanomaterials. A great deal of attention has been attracted for applications of nanoparticles or NPs-based composites as building blocks to electronics, optoelectronics and bio-sensing [2–6]. One of the most feasible applications in recent year is related to the nanocrystal memory. It utilizes the nanoparticles as charge-trapped center in the gate dielectric for the metal–oxide–semiconductor devices [7, 8]. The charge-trapped center, which electron can be injected in or out, will alter device threshold voltage, i.e., device can be controlled in two or more different gate voltages [9].

Sharma and coworkers have used copper NPs and atomic layer deposition (ALD) of aluminum oxide to fabricate high density capacitors [5]. However, the method uses very expensive tool of ALD to achieve devices. In contrast, the self-organization to assemble uniform NPs directly from solution is relatively simple and easy to fabricate electronic capacitor. As to the fabricated devices, Coulomb blockade effects have been shown only below about 77 K due to the random size distribution of the nanocrystals [7]. The nanocrystal memory operates at low voltage compared to conventional flash memory due to thinner tunneling dielectrics since the spacing between the quantum dots suppresses the charge loss through lateral paths. For practical application, however, room temperature operation capability is required, which is made possible by assembling small and uniform dots. It also has been proposed [10] that metal nanocrystal is a good candidate for the memory due to the engineering possibility of the metal work function, adjustable barrier height up to 2 eV, and much flexibility for device optimization. The depth of the potential well for the storage nodes can be engineered to create an asymmetrical barrier between

C.-C. Chen · E. Y. Chang (✉) · F.-H. Ko (✉)
Department of Material Science and Engineering, National Chiao Tung University, Hsinchu 30050, Taiwan
e-mail: edc@mail.nctu.edu.tw

F.-H. Ko
e-mail: fhko@mail.nctu.edu.tw

H.-C. You
Department of Electronic Engineering, National Chin-Yi University of Technology, Taichung 41170, Taiwan

the substrate and the storage nodes, i.e. a small barrier for writing and a large barrier for retention. This aim can be achieved if the storage nodes are fabricated from the metal nanocrystals. However, this device of metal nanoparticle (crystal) memory still considers a couple of issues. The critical problem needs concerning the metal diffusion, leading to the poor yield. The device of gold/SiO_2/Si structure is annealed at 500–800 °C, and the Au is found to diffuse through the silicon dioxide layer [11, 12]. The occurrence will induce the unpredictable leakage path. Furthermore, the process of writing and erasing will suffer from non-uniform charging on nanoparticles.

In this study, we firstly synthesize gold NPs materials from the solution preparation method to ensure the uniform size distribution, and then self-assemble NPs onto the device under room temperature. Then, we evaluate the device leakage current and leakage model for two sizes of gold nanoparticles. The capacitance–voltage of the gold embedded device is also measured to extract the threshold voltage shift. The endurance for the device reliability is also evaluated.

2 Experimental

All reagent and solvent are of reagent-grade quality, purchased commercially, and used without further purification unless otherwise noted. In this experiment, there are three major procedures including of preparation of gold nanoparticles in aqueous solution, room temperature self-assembly of nanoparticles onto gate oxide, and fabrication of nanoparticles embedded MOS capacitor.

2.1 Preparation of gold NPs materials in aqueous solution

Dispersed gold nanoparticles are prepared in aqueous solution by using a chemical reduction method. We synthesize two sizes of nanoparticles, i.e. 3.5 and 13.2 nm. The procedure for the preparation of 3.5 nm nanoparticles is described below [13]. A 20 mL aqueous solution containing 0.25 mM $HAuCl_4$ and 0.25 mM trisodium citrate is added into a conical flask. Then, a 0.6 mL of 0.1 M $NaBH_4$ solution (ice-cold, freshly prepared) is gradually added into the flask during the stirring condition. The solution turns pink immediately after adding $NaBH_4$, indicating the formation of gold nanoparticle. The particles will denature after ca. 2–5 h and is suggested to use immediately after preparation. The citrate ion serves as a capping agent for the reaction because it cannot reduce the gold salt under room temperature (25 °C). The size of the nanoparticles is estimated to be 3.5 $\pm$ 0.7 nm (Fig. 1a). The synthetic procedure for the 13.2 nm gold nanoparticles is similar with the published paper [14]. Briefly, 1 mM $HAuCl_4$ (100 mL) is heated near its boiling point under the vigorous magnetic stir, and then 35 mM sodium citrate solution (10 mL) is added. The resulting solution is maintained at a reflux condition for 30 min. The color of the solution changes from yellow to brownish-red upon the chemical reduction of $HAuCl_4$ mediated by citrate; this color change indicates the successful synthesis of the gold nanoparticles. An SEM image indicates that the gold nanoparticles we have synthesized is spherically shaped; we estimates the particle diameters is about 13.2 $\pm$ 1.9 nm.

2.2 Room temperature self-organization of nanoparticles onto gate oxide

The first step in manufacturing metal–oxide–semiconductor capacitor is to sandwich a p-type Si(100) wafer (Phoenix, San Jose, CA) with 40 Å tunneling SiO_2 thin films using furnace (ASM/LB45 Furnace system) at 925 °C. The substrates are cleaned and immersed into concentrated HCl acid for 5 min, followed by rinsing with deionized water. The substrates are then immersed in concentrated H_2SO_4 solution for 5 min and rinsed with

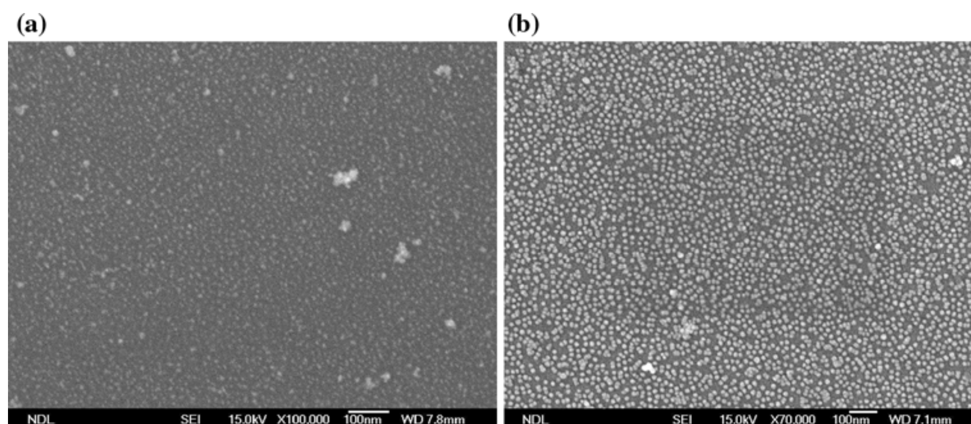

Fig. 1 SEM images of **a** 3.5 nm gold nanoparticles, and **b** 13.2 nm gold nanoparticles self-assembly onto the tunneling oxide

water again, followed by boiling in deionized water for several minutes prior to chemical functionalization. A 3-aminopropyl trimethoxysilane (APTMS) is prepared as 5 mM solution in ethanol. The substrate is immersed into the APTMS solution for 1 min at room temperature, followed by rinsing with ethanol and dried under N_2. The functionalized substrate is immersed in the gold nanoparticles solution (3.5 and 13.2 nm, respectively) for 15 min, then rinsed with deionized water and dried under N_2. The nanoparticles/APTMS/SiO_2 sandwich structures are stabilized through specific Au-NH_2 interactions [15]. The resulting nanoparticle images on wafers are illustrated in Fig. 1. The deposited densities of size of 3.5 and 13.2 nm gold nanoparticles are 6.2×10^{11} and 3×10^{11} pieces/cm^2, respectively.

2.3 Processing of NPs materials for embedded MOS capacitor

Prior to deposition of the controlling silicon oxide film on the nanoparticles, the NPs/APTMS/SiO_2 structure is fabricated. A plasma-enhanced chemical vapor deposition system (STS Multiplex Cluster System) is used to deposit control silicon dioxide layer of 100 Å at 250 °C. Subsequently, aluminum film of 5,000 Å is deposited on both wafer sides by sputter system (MRC Primus 2500TM) at 300 °C. After fabricating the stack Al/control oxide/nanoparticles/tunneling oxide structure, a G-line photoresist layer (Fuji FH6400L) is spin-coating onto the stack layers, and exposed to obtain the square pattern at various sizes from the ASML G-line stepper (Model PAS 2500). Then, the wafer is immersed in the 2.38 % Tetramethylammonium hydroxide (TMAH) solution to achieve the photoresist pattern. After the photoresist patterning, Anelva ILD-4100 helicon wave etcher is used to etch the unprotected aluminum and the silicon dioxide layers. The etch process stops at the bulk Si. The final device is illustrated in Fig. 2a. The cross-sectional transmission electron microscope (TEM) image of the device is shown in Fig. 2b. We can clearly obtain from the TEM image that the thickness of tunneling oxide layer is ~40 Å and the diameter of gold nanoparticles is ~3.5 nm. The fabrication process of the stacking structure, except for the tunneling silicon dioxide layer, is under 350 °C. The critical process of nanoparticle self-assemble layer is conducted at room temperature. The device electrical performance for capacitance–voltage data is measured with the Keithley C–V system, and current–voltage measurement is with HP 4156 semiconductor parameter system.

3 Results and discussion

As to evaluate the device leakage current and leakage model, the current density with respect to electric field is shown in Fig. 3. The leakage current for the room temperature gold nanoparticles embedded devices is lower than 10^{-5} A/cm^2. The leakage current for these devices is similar with the literatures [10], while the literature method requires 550 °C temperature to form the nanocrystal. One of most important injection mechanism used in floating gate device is the so-called Fowler–Nordheim (FN) tunneling, which in fact, is a field-assisted electron tunneling mechanism. In order to find the favorable device mechanism, FN tunneling Wentzel-Kramers-Brillouin (WKB) approximation is first used to fit these devices [16]. Figure 4 shows the relationship of $\log\left(\frac{J}{E^2}\right)$ versus (1/E), where J is current density and E is electric field. These devices assembled with 3.5 or 13.2 nm gold nanoparticles follow with the prediction of Fowler–Nordheim tunneling model for 4 nm tunneling oxide. This observation suggests the room temperature surface immobilization of gold nanoparticles is a possible means to fabricate the devices with lower leakage current. The nonuniformity (20 % for 3.5 nm Au, and 14.4 % for 13.2 nm Au) from particle size also has no damage effect on the leakage current.

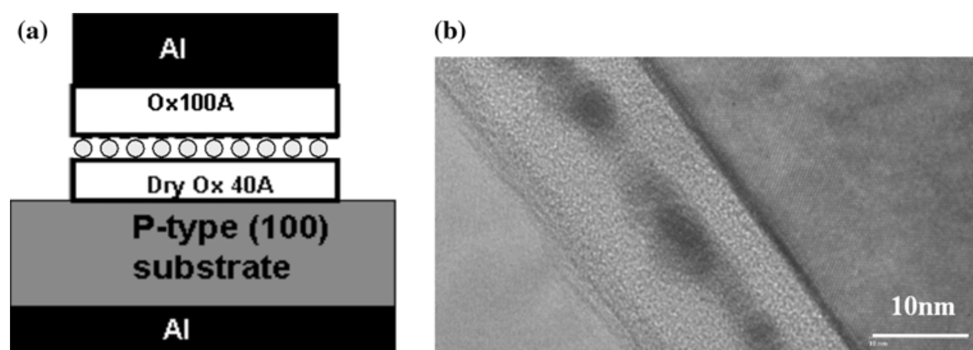

Fig. 2 **a** The gold nanoparticles embedded capacitor with 4 nm tunneling oxide and 10 nm control oxide, and **b** TEM image of 3.5 nm gold nanoparticles embedded capacitor

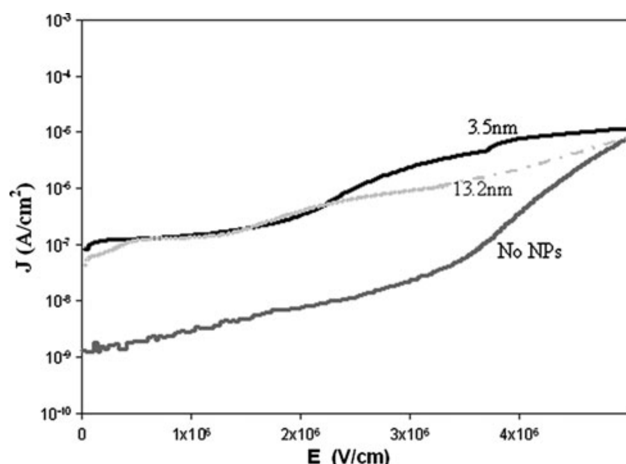

Fig. 3 The current density–electric field plot (J–E) for various nanoparticles sweeping the voltage from 0 to 5 MV/cm^2

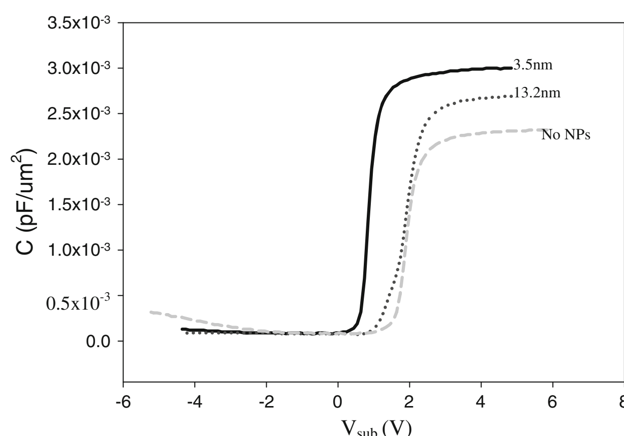

Fig. 5 The capacitance–voltage plot (C–V) for various nanoparticles sweeping the voltage from 5 to −5 V

The capacitance–voltage curve of the fabricated MOS capacitor exhibits the distinct accumulation, depletion and inversion regions, as depicted in Fig. 5. The MOS capacitor is basically used an oxide film as the dielectric material. Assuming the silicon is a perfect conductor, the parallel-plate capacitance would be determined by the oxide capacitance as it is in the accumulation region. Three types of devices are measured in Fig. 5. The pure oxide device has the lowest capacitance than the nanoparticles embedded devices. The capacitance of oxide is 2.3×10^{-3} pF/μm^2, which is smaller than 3.5 and 13.2 nm nanoparticles embedded devices. This figure also suggests the smaller size of nanoparticles exhibits the higher capacitance. This phenomenon is related to the nanoparticles density that the smaller one has the higher dense charge center. The C–V curves of 3.5 and 13.2 nm nanoparticles are also shift from the pure oxide devices. As the Figs. 1 and 3 mention, the high density of 3.5 nm nanoparticles will demonstrate higher capacitance as well as more threshold voltage shift with respect to no embedded nanoparticles. The observation is attributed to the effect of density on the charge storage site. This shift confirms the phenomenon of charge storage for nanoparticles embedded devices. From the basic theory of MOS capacitor, the threshold voltage (V_{TH}) is given by $V_{TH} = 2\Phi_F + \Phi_{MS} - \frac{Q_i}{C_i} - \frac{Q_d}{C_i} - \frac{Q_T}{E_i} d_i$. Thus, the threshold voltage shifts, caused by storage of the charge Q_T is given by $\Delta V_{TH} = -\frac{Q_T}{E_i} d_i$, where Q_T is the charge stored in the gate insulator at a distance d_i from the gate; E_i is the dielectric constant of the insulator; Φ_F is the potential difference between the Fermi level and the intrinsic Fermi level; Φ_{MS} is the work function difference between Al electrode and Si [16].

As to the memory device, the shift of threshold voltage indicates the device can be operated at two different voltages, i.e. memory window. The window can be evaluated by using the forward and reverse bias stressing on the nanoparticles embedded devices. The threshold voltage shifts for nanoparticle embedded devices are very significant from Fig. 6. The threshold voltage shifts for 3.5 and 13.2 nm nanoparticle devices are 1.5 and 1 V, respectively. In contrast, the pure oxide device has no shift on threshold voltage. The charges of 3.5 and 13.2 nm nanoparticles embedded capacitors are estimated to be 5.18×10^{-8} and 3.45×10^{-8} C/cm^2, respectively. The threshold voltage shift for both the nanoparticle embedded devices is higher than 1 V, and is better than the literature report [10]. This observation is attributed to the suitable work function for metal nanoparticles, uniform size distribution of gold

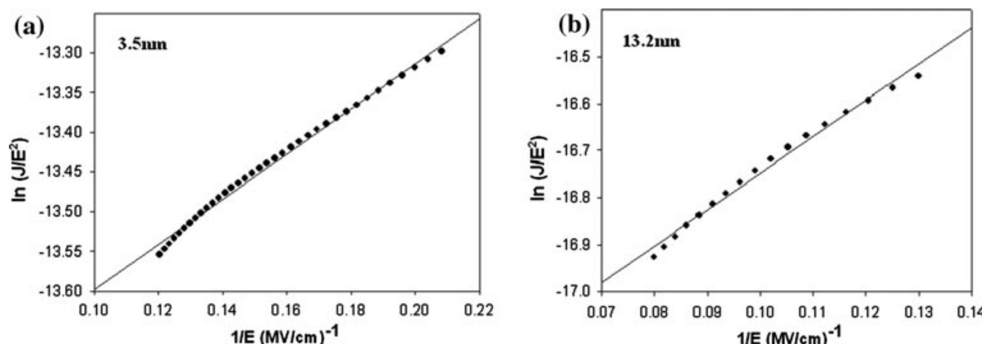

Fig. 4 Fowler–Nordheim tunneling plot of **a** 3.5 nm nanoparticles embedded capacitor, and **b** 13.2 nm nanoparticles embedded capacitor

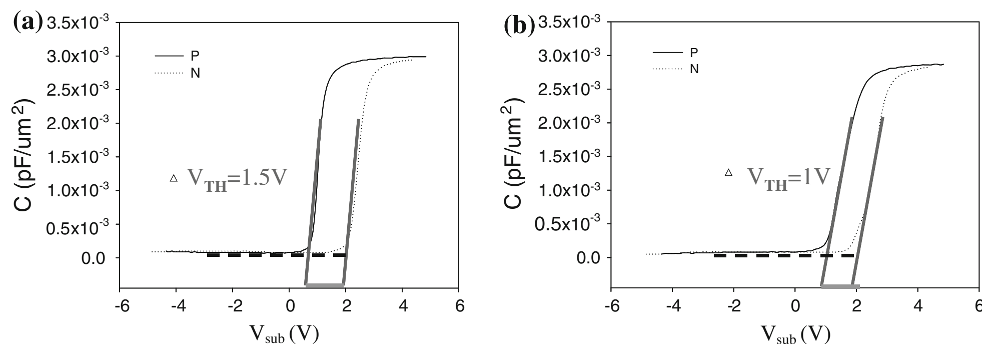

Fig. 6 The capacitance–voltage plot (C–V) of **a** 3.5 nm nanoparticles embedded capacitor, and **b** 13.2 nm nanoparticles embedded capacitor. Forward and reverse sweeping of the voltage from 5 to −5 V for P-type, and −5 to 5 V for N-type

nanoparticles, and relative low temperature process. Although it is not illustrated here, the capacitance of the obtained devices is strictly proportional to the area of electrode. This trend ensures the reliability of nanoparticles embedded devices.

Another important test, i.e. the charge retention time for the capacitor, is also evaluated. The charge retention time is a performance indicator for the nonvolatile memory. The pure oxide capacitor has no shift of threshold voltage. On the contrary, the nanoparticles embedded capacitors have more than 1 V shift of threshold voltage for at least 2 months. These devices are heated to 100 °C to accelerate the degeneration of devices. Figure 7 illustrates, after 50 h heating on 13.2 nm device, the shift of threshold voltage drop to 0.7 V. The thermal stressing process induces the leakage path occur more easily. For 3.5 nm device, the shift of threshold voltage begins to drop after 60-h heating. This result shows smaller sized nanoparticles have better endurance to current leakage. Because nanoparticles are discrete charge-trapped centers in oxide layer, if a leakage path occurs, only the local charge leaks out. The leakage current of local charge is inverse proportional to density of discrete charge-trapped centers. In addition, the uniform size distribution of nanoparticles in Figs. 1 and 2b also suppresses the leakage problem. This developed gold NPs materials and self-organization method for embedded electronic devices can be applied for future room temperature device operation. In comparison with our previous report on devices from sol–gel film processing method [17], these NPs-based devices also demonstrate stable and reliable property under room temperature operation. The intended reliability evaluation under 100 °C operation also suggests the reliability performance for 40-h duration.

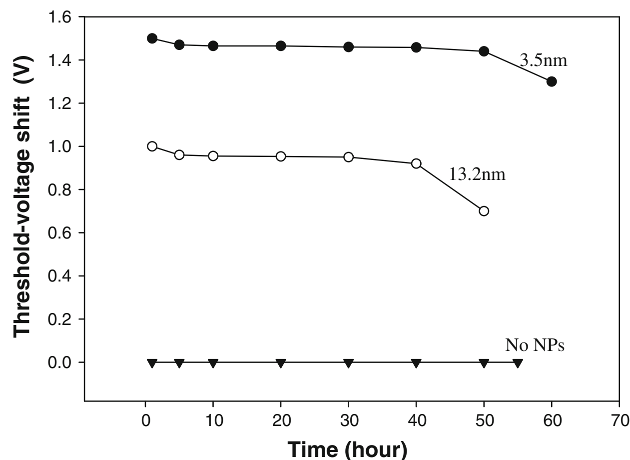

Fig. 7 The endurance of charge retention time for various sizes of nanoparticles at 100 °C up to 60 h

4 Summary

The gold nanoparticles embedded capacitors have successfully fabricated through the chemical synthesis, nanoparticles self-assembly, and semiconductor process. The advantages of the developed method include room temperature process, and uniform size distribution of nanoparticles. The leakage current of nanoparticle devices is low, and electrons transfer mechanism is following with Fowler–Nordheim tunneling model, of which is a standard mechanism for memory writing and erasing. The devices have large memory windows over 1 V for 13.2 nm and 1.5 V for 3.5 nm, respectively. Endurance of charge retention time is also a plus for the 3.5 nm nanoparticle embedded device even in high temperature stressing. The resulting geometry and electronic characteristics can be extended to fabricate future semiconductor memory devices.

Acknowledgment This work was supported by the NSC-funded project (NSC 98-2113-M-009-017). The semiconductor fabrication processes and measurements were carried out using the facilities located in the National Nano Device Laboratories.

References

1. C.-S. Wu, F.-K. Liu, F.-H. Ko, Anal. Bioanal. Chem. **399**, 103 (2011)
2. C.-C. Chen, F.-H. Ko, E.Y. Chang, F.-C. Chang, S.-W. Kuo, J. Vac. Sci. Technol. **B22**, 2572 (2008)
3. Y.M. Chen, Y.S. Huang, K.Y. Lee, D.S. Tsai, K.K. Tiong, J. Mater. Sci. Mater. Electron. **22**, 890 (2011)

4. C.-C. Chen, F.-H. Ko, C.-T. Chen, T.-F. Liu, E.Y. Chang, Y.-S. Yang, S.-J. Yan, T.-C. Chu, Appl. Phys. Lett. **91**, 253103 (2007)
5. H. Sharma, K. Sethi, P. Markondeya Raj, R. Tummala, J. Mater. Sci. Mater. Electron. **23**, 528 (2012)
6. C.C. Chen, C.Y. Tsai, F.H. Ko, C.C. Pun, H.L. Chen, P.H. Chen, Jpn. J. Appl. Phys. **43**, 3611 (2004)
7. S. Tiwari, F. Rana, H. Hanafi, A. Hartstein, E.F. Crabbe, K. Chan, Appl. Phys. Lett. **68**, 1377 (1996)
8. C.-C. Wu, F.-H. Ko, W.-L. Yang, H.-C. You, F.-K. Liu, C.-C. Yeh, P.-L. Liu, C.-K. Tung, C.-H. Cheng, IEEE Electron Device Lett. **31**, 746 (2010)
9. F.-H. Ko, H.-C. You, C.-M. Chang, W.-L. Yang, T.-F. Lei, J. Electrochem. Soc. **154**, H268 (2007)
10. Z. Liu, C. Lee, V. Narayanan, G. Pei, E.C. Kan, IEEE Trans. Electron Devices **49**, 1606 (2002)
11. E.I. Alessandrini, D.R. Campbell, K.N. Tu, J. Appl. Phys. **45**, 4888 (1974)
12. K.N. Tu, S. Libertini, J. Appl. Phys. **48**, 420 (1977)
13. N.R. Jana, L. Gearheart, C.J. Murphy, Langmuir **17**, 6782 (2001)
14. K.C. Grabar, R.G. Freeman, M.B. Hommer, M.J. Natan, Anal. Chem. **67**, 735 (1995)
15. F.K. Liu, Y.C. Chang, F.H. Ko, T.C. Chu, B.T. Dai, Microelectron. Eng. **67**, 702 (2003)
16. W.D. Brown, J.E. Brewer, *Nonvolatile Semiconductor Memory Technology* (IEEE Press, NY, 1998)
17. C.-C. Wu, Y.-J. Tsai, M.-C. Chu, S.-M. Yang, F.-H. Ko, P.-L. Liu, W.-L. Yang, H.-C. You, Appl. Phys. Lett. **92**, 123111 (2008)