Reduction of Equivalent Series Inductor Effect in Delay-Ripple Reshaped Constant On-Time Control for Buck Converter With Multilayer Ceramic Capacitors

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***Abstract*—The stability of conventional constant on-time control buck converter is constrained by the time constant, which is the product of the output capacitor and its equivalent series resistance (ESR). Specialty polymer capacitor which is mostly used as output capacitor for such a consideration although it limits the performance of converter. On the other hand, the multilayer ceramic capacitors are widely used in commercial power management ICs due to the advantages of low cost and ESR. However, the stability often confronts with the subharmonic problem caused by small time constant. A differential-zero compensator with the noise margin enhancement (DZC-NME) technique in constant on-time control buck dc–dc converter with output ceramic capacitor is proposed in this paper. Thus, the proposed DZC-NME technique not only eliminates the limit of large time constant but also tolerates the existence of equivalent series inductor (ESL) effect. Experiment results demonstrate small output ripple of 10 mV and high efficiency of 91% when ESR is smaller than 1 mΩ and large interference from ESL effect is 40 mV.**

***Index Terms*—Constant on-time control for buck converter, equivalent series inductor (ESL), multilayer ceramic capacitors (MLCC), power management.**

I. Introduction

POWER management module plays an important role in portable products to extend the battery life and provide the high-quality power supply [1]–[4]. There are various kinds of topology for meeting different required specifications and applications [5]–[11]. As a result, the constant on-time (COT) control has been widely used due to its high efficiency, good transient response, and simple control mechanism [12], [13]. As illustrated in Fig. 1, conventional COT control in the buck converter is constructed by comparator, on-time timer, MOSFETs as switches, and the energy storage components, inductor, and capacitors. Once the feedback voltage $V_{\rm FB}$ falls below the reference voltage $V_{\rm REF}$ and is detected by the comparator, the one-shot timer is triggered to increase the inductor current until a predefined on-time $T_{\rm ON}$ expires. To ensure system stability, the inductor current information derived from the output ripple is used as the ramp signal in the pulsewidth modulation (PWM) to determine duty cycle. Basically, in Fig. 2, the output voltage ripple caused by the inductor current ripple contains three major terms, which are $V_{\rm ESL}$, $V_{\rm ESR}$, and $V_{\rm COUT}$ contributed by the parasitic effect on the equivalent series inductance (ESL), the equivalent series resistance (ESR), and the output capacitor $C_{\rm OUT}$, respectively.

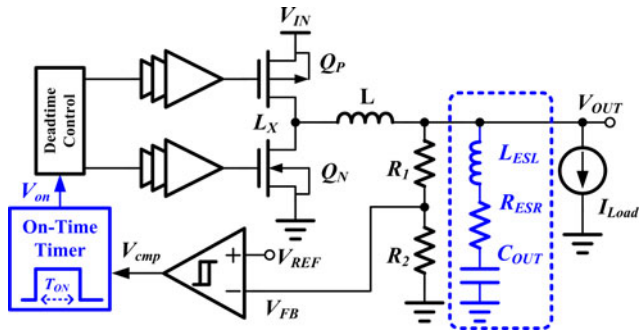

Fig. 1. Architecture of the COT control in conventional dc–dc buck converter.

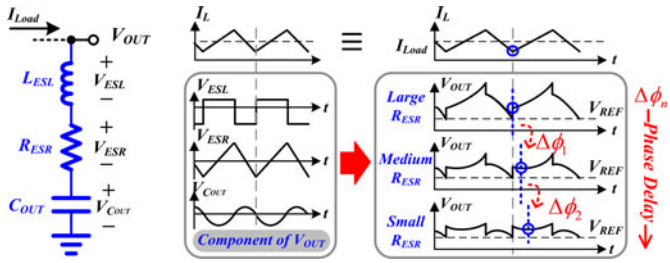

Fig. 2. Relationship between the output voltage ripple and the inductor current under different $R_{\rm ESR}$.

Under the same output capacitor value, different ESR value $R_{\rm ESR}$ results in different output ripple. It can be translated to the phase delay $\Delta\Phi$ related to the inductor current I_L owing to variable $R_{\rm ESR}$. The smaller the $R_{\rm ESR}$, the longer phase

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TABLE I
SORTS OF CAPACITOR

		Capacity	F-C	T-C	High-Voltage	High-Temp	Size	Life	Cost	R_{ESR}
Al capacitor	Electrolyte	✓✓	×	×	✓	○	✓	×	✓✓	Large
	OS-Cap	✓✓	✓	✓✓	×	×	○	✓	○	Large
	SP-Cap	✓✓	✓	✓✓	○	✓	○	✓	○	Large
TA capacitor (POS-CAP)		✓	○	✓✓	○	✓	✓	○	✓	Medium
Film capacitor		×	✓✓	✓✓	✓✓	○	×	✓✓	○	Small
MLCC		✓	✓✓	○	✓✓	✓✓	✓	✓✓	✓	Small

×:Bad ○:Fair ✓:Good ✓✓:Excellent

delay is observed at the lowest point of the $V_{\rm OUT}$. It will worsen the system stability. In other words, the switching frequency should be kept high enough to overcome the phase delay for system stability. However, it is not practical to raise the switching frequency to higher than megahertz because the switching loss degrades the efficiency. The phase delay is basically caused by the type of the output capacitor. That is, the selection of the output capacitor will seriously affect the system stability if the COT control is used.

Table I shows various kinds of capacitor including electrolyte capacitor, OS-Cap, SP-Cap, POS-CAP, film capacitor, and multilayer ceramic capacitor (MLCC), and ranks their performance according to each characteristic. Here, *F-C* and *T-C* represent its variation of quality at different frequency and temperature, respectively. *High-Voltage* and *High-Temp* represent the limit of highest voltage and temperature, respectively. Especially, the SP-Cap is the most common choice in applications with conventional COT control buck converter since the system stability is guaranteed only with large ESR value, but the output ripple is large. The inexpensive MLCC will be excluded due to its low ESR. However, the MLCC is one of the suitable choices owing to it low cost and other superior characteristics as listed in Table I [14], [15]. Therefore, to ensure system stability and low cost, the differential-zero-compensator with the noise margin enhancement (DZC-NME) technique is proposed. In other words, the system stability is increased by the DZC-NME technique without being affected by phase delay when the MLCC is utilized.

In this paper, the structure of conventional COT control buck converter is introduced in Section II to reveal the stability criteria. Then, the proposed COT control with the DZC-NME technique is described in Section III to show the high performance with the MLCC. The circuit implementation is presented in Section IV. Experimental results are shown in Section V. Finally, the conclusion is made in Section VI.

II. Disadvantage of Conventional Adaptive COT Control in Buck Converter Structure

The derivation of the stability criteria of the adaptive COT control can reveal the idea of the DZC-NME technique to guarantee the system stability with the use of the MLCC.

The COT control does not have an internal clock in the whole system. Thus, the COT control should still keep a constant

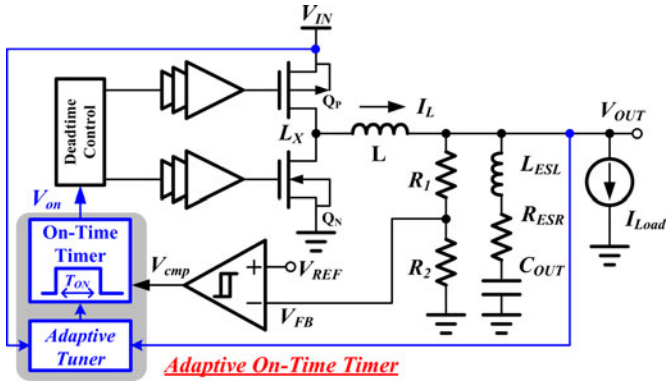

Fig. 3. DC–DC buck converter with the adaptive on-time control.

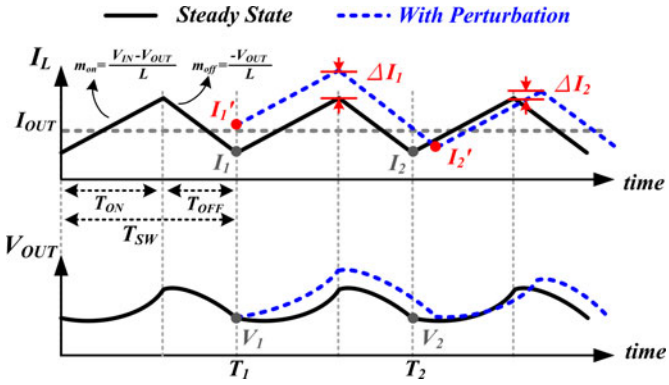

Fig. 4. Steady-state waveforms and with the insertion of the perturbation.

switching frequency at the continuous conduction mode (CCM) operation to ensure that the electromagnetic interference (EMI) can be minimized by a specific output filter. For maintaining the switching frequency constant, the adaptive on-time circuit adjusts the on-time period according to the input voltage $V_{\rm IN}$ and the output voltage $V_{\rm OUT}$, as shown in Fig. 3. As a result, the switching frequency is determined by (1) [16]. If the on-time $T_{\rm ON}$, as expressed in (2), is inversely proportional to the $V_{\rm IN}$ but directly proportional to the $V_{\rm OUT}$, the switching frequency f_{SW} will be nearly constant as shown in (3)

$$f_{\rm SW} = \frac{V_{\rm OUT}}{V_{\rm IN} T_{\rm ON}} \tag{1}$$

$$T_{\rm ON} = \frac{V_{\rm OUT}}{V_{\rm IN}} \times k_1, \quad \text{where } k_1 = \text{constant} \tag{2}$$

$$f_{\rm SW} = \frac{V_{\rm OUT}}{V_{\rm IN} \cdot ((V_{\rm OUT}/V_{\rm IN}) \cdot k_1)} = k_1. \tag{3}$$

According to the steady-state waveforms in Fig. 4 if the ESL effect is ignored, the voltage difference should be zero after one switching period as expressed in (4). The switching period T_{SW} is the summation of the $T_{\rm ON}$ and the $T_{\rm OFF}$, which are the on-time and the off-time, respectively

$$V_2 - V_1 = \frac{1}{C_{\rm OUT}} \int_0^{T_{\rm SW}} (I_L(t) - I_{\rm OUT}) dt + (I_2 - I_1) R_{\rm ESR} = 0$$

where

$$T_{\rm SW} = T_{\rm ON} + T_{\rm OFF} \quad \text{and}$$
$$\begin{cases} I_L(t) = \dfrac{V_{\rm IN} - V_{\rm OUT}}{L} t, & \text{in on-time period} \\ I_L(t) = \dfrac{-V_{\rm OUT}}{L} t, & \text{in off-time period} \end{cases} \tag{4}$$

Besides, the $T_{\rm OFF}$ can be expressed as

$$T_{\rm OFF} = \left(\frac{V_{\rm IN}}{V_{\rm OUT}} - 1 \right) T_{\rm ON}. \tag{5}$$

Substituting (5) into (4), following equation can be derived after evaluating integers and simplifying

$$\frac{V_{\rm IN}}{V_{\rm OUT}} \frac{T_{\rm ON}}{C_{\rm OUT}} (I_1 - I_{\rm OUT}) + \frac{T_{\rm ON}^2}{2C_{\rm OUT}L_1} \frac{V_{\rm IN}}{V_{\rm OUT}} (V_{\rm IN} - V_{\rm OUT}) + R_{\rm ESR} (I_2 - I_1) = 0. \tag{6}$$

To conclude the stability criteria and linearize the (6), the small perturbation signals ΔI_1 and ΔI_2 are taken into consideration in the steady-state inductor currents I_1 and I_2, which are shown in (7), at the time of T_1 and at time of T_2, respectively, according to the inductor current waveforms in Fig. 4

$$\begin{cases} I_1 = I_{\rm OUT} - \dfrac{T_{\rm ON}}{2L}(V_{\rm IN} - V_{\rm OUT}) \\ I_2 = I_{\rm OUT} - \dfrac{T_{\rm ON}}{2L}(V_{\rm IN} - V_{\rm OUT}). \end{cases} \tag{7}$$

Consequently, the inductor currents I_1' and I_2' with perturbation at the time of T_1 and at the time of T_2, respectively, can be expressed as

$$\begin{cases} I_1' = \Delta I_1 + I_{\rm OUT} - \dfrac{T_{\rm ON}}{2L}(V_{\rm IN} - V_{\rm OUT}) \\ I_2' = \Delta I_2 + I_{\rm OUT} - \dfrac{T_{\rm ON}}{2L}(V_{\rm IN} - V_{\rm OUT}) \end{cases} \quad \text{and}$$
$$I_2' - I_1' = \Delta I_2 - \Delta I_1. \tag{8}$$

Substituting (8) into (6), (9) can be derived as

$$\Delta I_1 \left(R_{\rm ESR} - \frac{V_{\rm IN}}{V_{\rm OUT}} \frac{T_{\rm ON}}{C_{\rm OUT}} \right) - \Delta I_2 R_{\rm ESR} = 0. \tag{9}$$

For increasing stability, $\Delta I_2/\Delta I_1$ must be gradually converged to zero in steady state. Thus, the inequality can be derived as (10) and simplified as (11)

$$\left| \frac{\Delta I_2}{\Delta I_1} \right| = \left| \frac{R_{\rm ESR} - (V_{\rm IN}/V_{\rm OUT})(T_{\rm ON}/C_{\rm OUT})}{R_{\rm ESR}} \right| < 1 \tag{10}$$

$$0 < \frac{1}{R_{\rm ESR} C_{\rm OUT}} < 2 \frac{V_{\rm OUT}}{V_{\rm IN} T_{\rm ON}}. \tag{11}$$

Finally, (12) is obtained to indicate that the stability is related to the relationship between the $R_{\rm ESR}$ and the $C_{\rm OUT}$ under the consideration of the switching frequency

$$f_{\rm SW} > \pi f_{\rm ESR}, \quad \text{where } f_{\rm SW} = \frac{V_{\rm OUT}}{V_{\rm IN} T_{\rm ON}},$$
$$f_{\rm ESR} = \frac{1}{2\pi \cdot R_{\rm ESR} C_{\rm OUT}}. \tag{12}$$

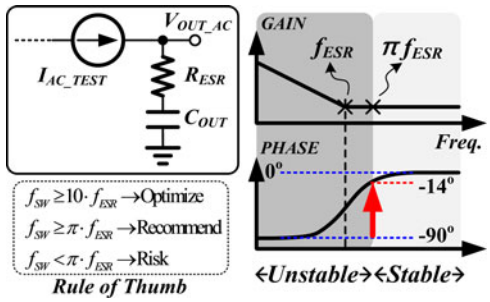

Fig. 5. Test model of the output capacitor and its frequency response with the stability criteria.

Obviously, due to this limitation, the specific material of capacitor is necessary to guarantee the system stability. Certainly, this constraint derived in this paper is more rigorous than that in the prior arts [13]. Furthermore, (12) can also correspond to the frequency response as shown in Fig. 5. The obtained ac response of output $V_{\rm OUT\_AC}$ indicates the design guideline of the COT control. The $R_{\rm ESR}$ and the $C_{\rm OUT}$ contribute a zero to reduce the phase delay between the inductor current ripple and output voltage ripple. That is, the system stability can be guaranteed since the phase is boosted from –90° to –14° at the desired operation switching frequency. Consequently, for adequate in-phase relationship between the two signals, it necessary to make sure the switching frequency is high enough.

The specialty polymer capacitor (SP-CAP) with a value of 200 μF has the ESR in tens of milliohms. It means that the $f_{\rm ESR}$ is near 50 kHz. That is, the f_{SW} needs to be great than 157 kHz for the maximum phase delay of 14°. It is easy to find some suitable SP-CAPs to increase the stability of the COT control system but the cost is high and the magnitude of output ripple is large. On the other hand, the ESR value of MLCC is only several milliohms at the same output capacitor value. It pushes the lowest allowable switching frequency to 1.4 MHz or even higher than it. However, higher switching operation will cause large switching loss and worse jitter problem. It results that the MLCC is not suitable for the conventional adaptive COT control.

Thus, the DZC-NME technique is proposed to compensate the delay of phase caused by the MLCC for increasing stability with low cost.

III. Proposed COT Control Buck Structure and System Loop Analysis

In the COT-control buck converter with low-ESR output capacitor, the low-ripple $V_{\rm OUT}$ is fed back to the controller by the voltage divider. Thus, the voltage ripple at the phase-delay $V_{\rm FB}$, which is compared to the $V_{\rm OUT}$, is smaller and has low noise immunity. Fig. 6 is the architecture of COT-control dc–dc buck converter and shows the proposed differential-zero compensator with the noise margin enhancement circuit (DZC-NME), which is composed of the differential-zero compensator (DZC) technology and the noise margin enhancement circuit (NME).

The $V_{\rm cmp}$ triggers the adaptive on-time timer (AONT) circuit to generate a COT period and thus the inductor current increases.

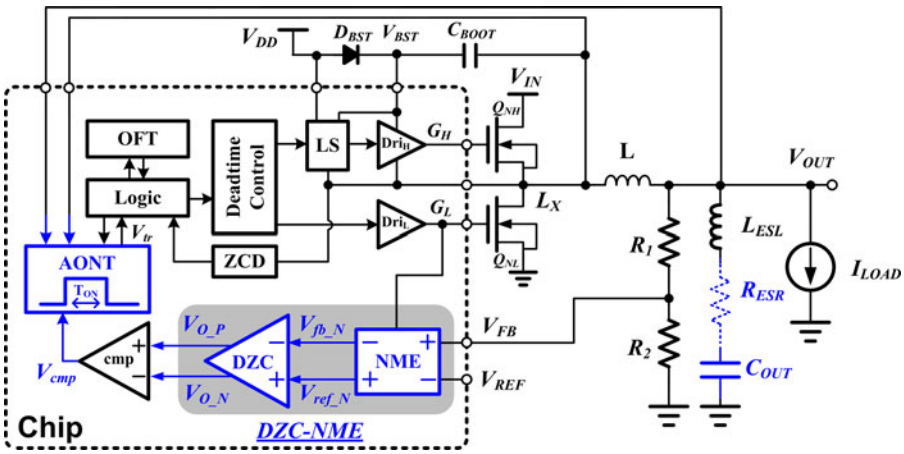

Fig. 6. Architecture of COT-control dc–dc bootstrap buck converter with the proposed DZC-NME technique.

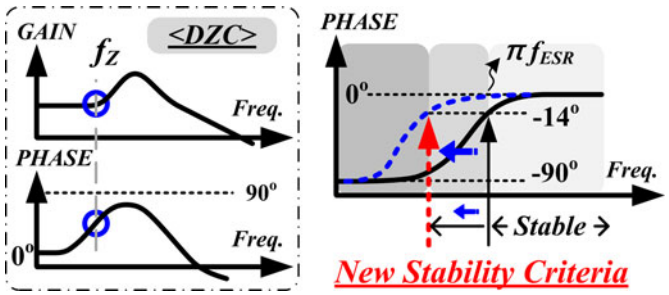

Fig. 7. Phase-lead effect caused by the proposed DZC technique can increase the system stability.

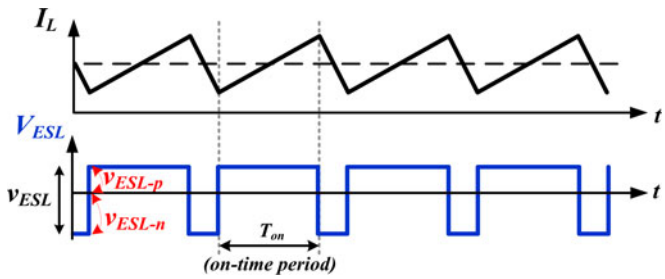

Fig. 8. ESL effect at the output voltage.

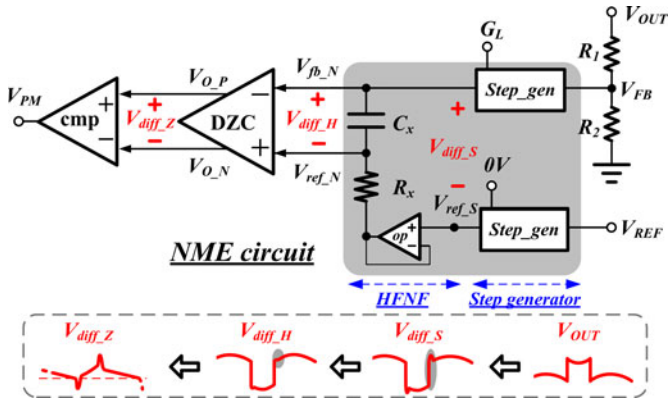

Fig. 9. Structure of the NME circuit.

On the other hand, after the end of the on-time, the inductor current decreases until the $V_{\rm FB}$ falls below the reference voltage, $V_{\rm REF}$, or the end time of minimum off-time generated by the off-time timer circuit. The minimum off-time is necessary to avoid over current or overshoot of output voltage caused by extreme duty condition during the start-up period or in case of light-to-heavy load variation. Besides, the zero-current detector (ZCD) circuit offers the function of discontinuous conduction mode (DCM) to further reduce the switching frequency for enhancing the power conversion efficiency at light loads.

When using MLCC as output capacitor with a low ESR, the output ripple voltage is mainly determined by the ESL and the charging/discharging on output capacitor $C_{\rm OUT}$. The low value of $R_{\rm ESR}$ which generates a high-frequency zero offers little assistance to increase phase margin. The instability caused by the low ESR value can be compensated by the DZC circuit, which corresponds to the proportional-differential (PD) controller with the frequency response as illustrated in Fig. 7. That is, the DZC circuit boosts the phase to meet the limited condition as 14 degrees at required frequency about 300 kHz and releases the conventional restriction without the need of large $R_{\rm ESR}$ and $C_{\rm OUT}$.

However, the existing ESL ($L_{\rm ESL}$ in Fig. 6) distorts the feedback control signal $V_{\rm FB}$ by the voltage step, $V_{\rm ESL}$, as shown in (13) and (14). It results that the on-time timer might be triggered at the incorrect time. As depicted in Fig. 8, the $V_{\rm ESL}$ is proportional to the $V_{\rm IN}$ and the $L_{\rm ESL}$. The $V_{\rm ESL}$ is as large as 42 mV when the $V_{\rm IN}$ is 21 V and the $L_{\rm ESL}$ is 1 nH if L is 2 μH

$$v_{\rm ESL} = v_{{\rm ESL}-p} + |v_{{\rm ESL}-n}| = \frac{V_{\rm IN}}{L} \cdot L_{\rm ESL} \tag{13}$$

where

$$v_{{\rm ESL}-p} = \frac{V_{\rm IN} - V_{\rm OUT}}{L} \cdot L_{\rm ESL} \text{ and } v_{{\rm ESL}-n} = \frac{-V_{\rm OUT}}{L} \cdot L_{\rm ESL}. \tag{14}$$

Therefore, the NME circuit as illustrated in Fig. 9 is proposed to alleviate the ESL effect for higher noise margin [13]. Here, the differential outputs of the step generator, the high-frequency

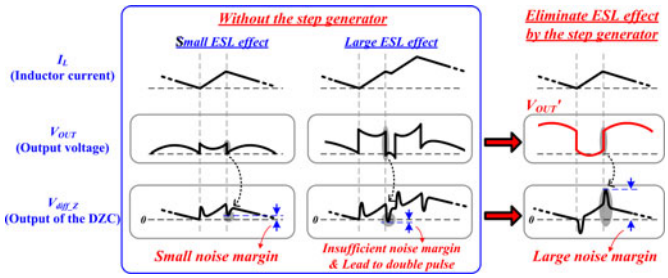

Fig. 10. Function of the step generator.

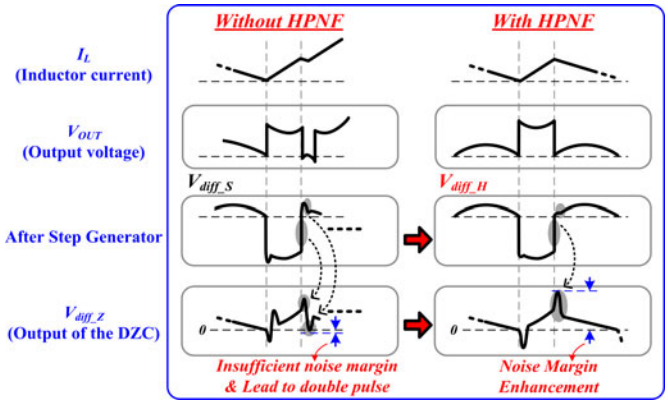

Fig. 11. Waveforms for illustrating the function of the DZC-NME technique.

noise filter (HFNF), and the DZC are the $V_{\mathrm{diff\_}S}$, the $V_{\mathrm{diff\_}H}$, and the $V_{\mathrm{diff\_}Z}$, respectively.

The V_{ESL}, one of the components of the V_{OUT}, is a step function. In Fig. 10 in case of a small ESL effect, the downstepping V_{ESL} at the beginning of off-time transfers to undershoot of the differential signal $V_{\mathrm{diff\_Z}}$ after the process of the DZC circuit but without the step generator circuit. Undershoot may drop below the 0 V caused by the ESL effect and incorrect triggering effect at the beginning of off-time instantly decreases the system stability. In other words, phenomenon of double pulse happens. To alleviate the unstable phenomenon, the proposed step generator creates an opposite step and thus the $V_{\mathrm{OUT}}{}'$ is revised from the V_{OUT}. As a result, overshoot of the $V_{\mathrm{diff\_Z}}$ at the beginning of off-time greatly enhances the noise margin. The $V_{\mathrm{diff\_Z}}$ is reshaped and is in phase with the inductor current after the overshoot. On the other hand, there is no need to take concern about the undershoot of the $V_{\mathrm{diff\_}Z}$, which is distorted drastically in the beginning of on-time, because the on-time is innately defined in the AONT circuit.

In order to eliminate the effect of the V_{ESL}, the opposite step must be generated and synchronized with the period of on-time. However, there is a limitation in bandwidth and phase margin (PM) for the step generator. If sacrificing PM to obtain enough speed, the differential output of the step generator $V_{\mathrm{diff\_}S}$ as shown in Fig. 11 will lead to double pulse after the DZC. For covering the defect of the step generator, the high-frequency noise filter circuit offers a solution to relieve it by coupling the high-frequency variation from one input terminal to the other terminal of the DZC. Consequently, the V_{FB} is preregulated by the NME circuit to enhance noise immunity at first, and then

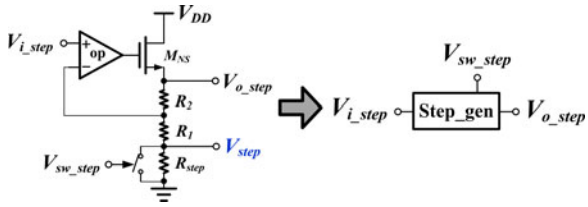

Fig. 12. Structure of the step generator.

regulated by the DZC technique. The differential output signal of the DZC, $V_{\mathrm{diff\_}Z}$, is reshaped from the phase-delay V_{FB} and thus in phase with the inductor current during the off-time period.

IV. Circuit Implementation

The proposed DZC-NME technique is implemented in the dc–dc buck converter with the bootstrap architecture as depicted in Fig. 6. It is mainly composed of two N-channel power MOSFETs (Q_{NH} and Q_{NL}) working as high-side and low-side switches. For completely turning ON the high-side switch, the level-shift circuit (LS) is used to level up the driving signal to the value of "$V_{\mathrm{DD}}+\mathrm{V_{IN}}-V_D$". The V_{DD} and the V_{IN} are supply voltages of the chip and the converting source voltage, respectively. The V_D is drop voltage of bootstrapping diode D_{BST}. Within the off-time period, the C_{BOOT} is charged to V_{DD} − V_D. The V_{IN} is pumped up to the value of "$V_{\mathrm{DD}}+\mathrm{V_{IN}}-V_D$" when the high-side power MOSFET turns ON.

A. DZC-NME Circuit

To analyze the function of the proposed DZC-NME technique, the DZC-NME technique is divided into two parts, the DZC and the NME. The NME as shown in Fig. 9 is composed of the step generator and the HFNF. The HFNF consists of the C_X, the R_X and a buffer which is to block the interference to the V_{REF}. The HFNF is used for coupling the same magnitude of instantaneous variation from the V_{FB}, such as the step of the V_{ESL} as shown in Fig. 2 or any high-frequency noise, to both two input terminals of the DZC.

The step generator is implemented as shown in Fig. 12. With the M_{NS}, the op-amp and the resistor divider, this structure forms as a negative feedback to decide the output signal, V_{o_step}, linearly depending on the input signal, V_{i_step}. The switch across the R_{step} is triggered by the control signal G_L of the low-side power MOSFET and the V_{o_step} goes toward high or low with the switch turning ON or OFF, respectively. The step magnitude can be derived as (15). Relative to the V_{ESL}, this opposite step enhances noise margin and avoids incorrect trigger caused by the step of the V_{ESL}

$$\Delta V_{o\_\mathrm{step}} = \frac{R_2 R_{\mathrm{step}}}{R_1(R_1+R_{\mathrm{step}})} V_{i\_\mathrm{step}}. \tag{15}$$

The differential zero compensator circuit is depicted as shown in Fig. 13. The P_1 and the P_2 constitute the input differential pair. The N_1 and the N_2 form active load. R_1, C_1, R_2, and C_2, are used to create low-frequency zero for the compensation. In

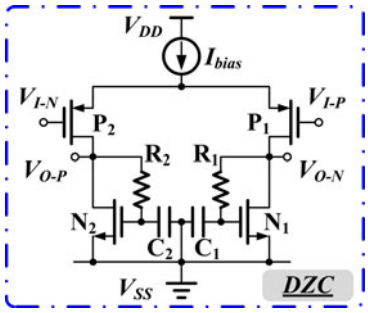

Fig. 13. Implementation of the DZC.

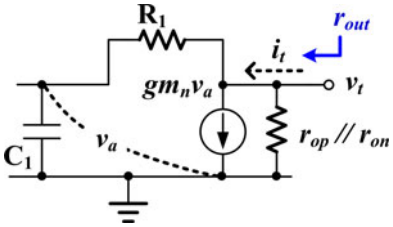

Fig. 14. Small-signal model of the DZC circuit.

the meanwhile, low-output impedance, which is generated by the pseudo-diode connection of the N_1 and the N_2, will result in high-frequency pole and lead to the function of phase lead of this compensator.

Fig. 14 indicates the corresponding small signal model of the DZC circuit. Setting the test voltage source v_t at the output of the DZC circuit, the output current i_t flows into the circuit.

By the KCL theorem, the i_t is expressed as

$$i_t = \frac{v_t}{r_{\rm on} /\!/ r_{\rm op}} + \frac{v_t}{R + (1/sC)} + gm \cdot v_a. \tag{16}$$

Neglecting the r_o caused by channel length modulation, the output impedance $r_{\rm out}$ is derived as (17) and the transfer function is shown in (18) with the pole and the zero locating at *gm_n/C* and *1/RC*, respectively

$$r_{\rm out} = \frac{v_t}{i_t} = \frac{1 + sRC}{gm_n + sC} \tag{17}$$

$$A_{\rm DM} = \left| \frac{V_{O-P} - V_{O-N}}{V_{\rm IN-P} - V_{\rm IN-N}} \right| = \frac{gm_p}{gm_n} \left(\frac{1 + sRC}{1 + s(C/gm_n)} \right). \tag{18}$$

Consequently, if $R \gg 1/gm_n$, the location of zero is at lower frequencies than that of the pole. Thus, the differential input signal $(V_{IN-P} - V_{\rm IN-N})$ will have phase lead compared to the differential output signal $(V_{O-P} - \mathrm{V}_{O-N})$. The R and C are set as 500 kΩ and 5 pF, respectively, to cause the zero is located about 63.6 kHz. The frequency response is depicted in Fig. 7. The compensated zero contributes that the maximum phase delay of 14° locates at about 200 kHz. Consequently, the system is allowed to operate at a lowest frequency 200 kHz without the need of large $R_{\rm ESR}$. In the meanwhile, the differential structure enhances the noise immunity and decreases the Jitter and the EMI effects. In this paper, the proposed technique ensures the stability although the 200 μF MLCC with only 1 mΩ ESR is used as the output capacitor.

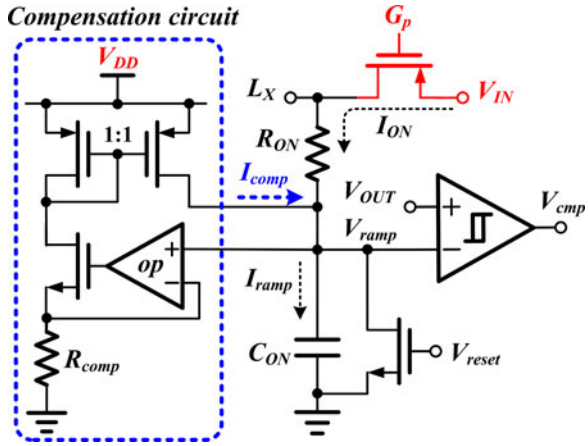

Fig. 15. Proposed AONT circuit for reliable switching frequency without being affected by the input voltage $V_{\rm IN}$.

B. AONT Circuit

Without an internal fixed frequency oscillator, an adaptive period of on-time is the solution to compensate the perturbations of $V_{\rm IN}$, $V_{\rm OUT}$, and $I_{\rm LOAD}$. Therefore, the reliable on-time timer is necessary to avoid frequency variation in steady state and thus stabilize the system without being affected by process, voltage, and temperature (PVT) variations.

The adaptive on-time circuit proposed in [17] derives a nonlinear on-time value if the input voltage changes because of the superfluous parameter from the gate–source voltage $V_{\rm GS}$ of diode-connected MOSFET. For a wide range of input voltage, the existing inaccuracy caused by the $V_{\rm GS}$ should be carefully removed. Besides, the ripple-based regulator can also be in accordance with an external clock, either directly or with a phase-locked loop (PLL) [18] and [19]. Unfortunately, it will need additional complicated circuits at the sacrifice of silicon area and cost. Here, Fig. 15 shows the proposed adaptive on-time timer. The charging current $I_{\rm ramp}$ including both $I_{\rm ON}$ and $I_{\rm comp}$ flows into the $C_{\rm ON}$ during the on-time period and thus the on-time value is independent of the $V_{\rm IN}$ as expressed in (19) since the $R_{\rm ON}$ can be equal to the $R_{\rm comp}$ by good matching methods in chip layout with a little influence of process variations

$$T_{\rm ON} = (R_{\rm ON} \cdot C_{\rm ON}) \cdot \frac{V_{\rm OUT}}{V_{\rm IN}}. \tag{19}$$

The (19) shows that the $T_{\rm ON}$ is simply determined by the $R_{\rm ON}$ and the $C_{\rm ON}$ without being affected by the $V_{\rm GS}$. The desired switching frequency can be obtained by trimming the capacitor $C_{\rm ON}$.

Substituting (19) into (1), the $f_{\rm SW}$ can be kept constant, irrespective of the $V_{\rm OUT}$ and the $V_{\rm IN}$. Comparing with prior arts, this circuit provides more accurate and linear solution to correctly minimize the variation of frequency. Therefore, the proposed COT control works as the function of the PWM operation even without the internal clock.

Furthermore, connecting the $R_{\rm ON}$ to the node L_X instead of the $V_{\rm IN}$ directly, the $I_{\rm ON}$ is only generated at the on-time period. The advantages include that the $V_{\rm ramp}$ is always lower than the

TABLE II
PERFORMANCE OF THE COT CONVERTER

Process	UMC 0.35μm BCD 40V
Input voltage (V_{IN})	5~21V
Output voltage(V_{OUT})	0.75 – 3.3V
Supply voltage for chip(V_{DD})	5V
Load range (I_{LOAD})	0.1A – 8A
Inductor	1 μH
Output Capacitor (MLCC)	220 μF (22μF*10)
R_{ESR}	1mΩ
L_{ESL}	2.6nH
Operation frequency	100 KHz – 600 KHz
Output ripple	8mV – 10mV
Maximum efficiency	91%

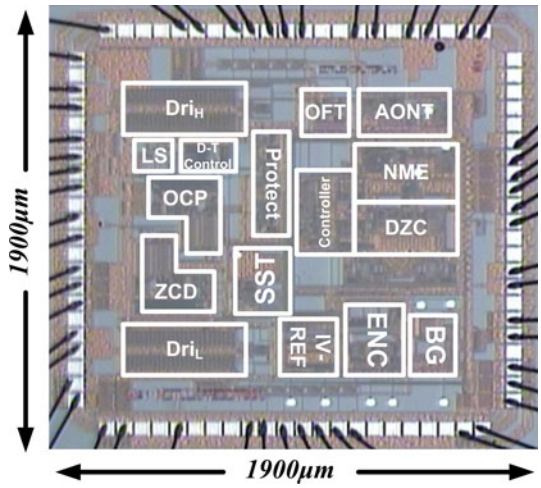

Fig. 16. Chip micrograph.

$V_{\rm OUT}$ and the concern of high-voltage damage caused by the $V_{\rm IN}$ and wasting power consumption can be avoided. Besides, the number of high-voltage devices can be reduced for low cost due to the proposed method.

V. EXPERIMENTAL RESULTS

A. Chip Micrograph

The COT buck converter with the DZC-NME technique was fabricated in UMC 0.35 μm BCD 40 V process. For application of high-conversion ratio and heavy driving current of 8 A, power MOSFETs are selected as discrete components. The high-side and the low-side power MOSFETs are the AOL1414 and the AOL1412, respectively. The off-chip inductor and the capacitor are selected as 1 μH and 220 μF (22 μF $\times$ 10), respectively. The specifications of the proposed converter are listed in Table II.

The nominal switching frequency is near 300 kHz. The output voltage ranges from 0.75 to 3.3 V with the input voltage defined by the laptop adapter or the desktop power supply. That is, the highest input voltage can be 21 V. Fig. 16 shows the chip micrograph with the active silicon area about 3.61 mm^2 including test circuits. Table III describes the function of the subcircuits.

TABLE III
DESCRIPTION OF SUBCIRCUITS

DZC	Differential-Zero Compensator	ZCD	Zero-Current Detector
NME	Noise Margin Enhancement	OCP	Over-Current Protector
AONT	Adaptive On-Time Timer	PROTECTOR	Protect Circuit
OFT	Minimum Off Time Timer	SST	Soft-Start
LS	Level Shift	BG	Bandgap
D-T Control	Deadtime Control	ENC	Enable Controller
Dri_H	High Side Driver	IV-REF	Biasing Current / Reference Voltage Generator
Dri_L	Low Side Driver		

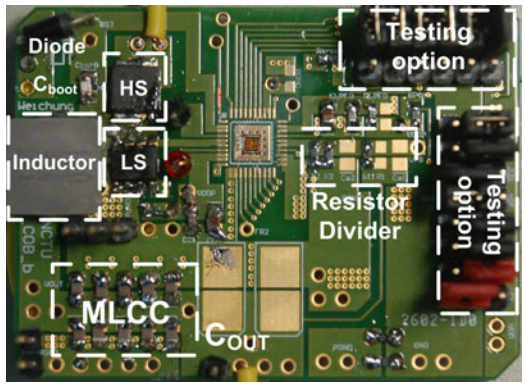

Fig. 17. Prototype of the proposed COT buck converter.

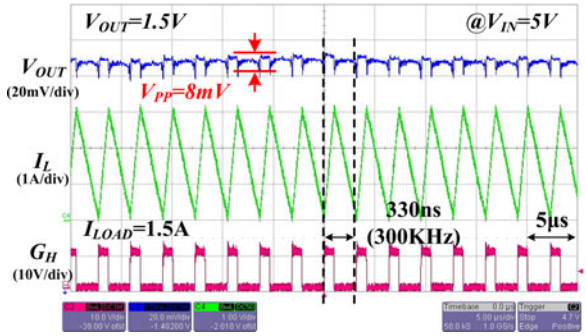

Fig. 18. Waveforms in steady-state with the proposed DZC-NME technique.

Fig. 17 shows the prototype of the COT buck converter with the proposed DZC-NME technique. Here, the MLCC is used as the output capacitor. Simply, the equivalent of the $R_{\rm ESR}$ value can be calculated as almost 1 mΩ only according to the estimated output ripple $V_{\rm pp}$ and (20) [16]

$$V_{\rm pp} = V_{C_{\rm OUT}} + V_{\rm ESR} = \frac{V_{\rm OUT}(1-D)}{8f_{\rm SW}^2 LC} + \frac{R_{\rm ESR} V_{\rm OUT}(1-D)}{f_{\rm SW} L}$$

$$\Rightarrow R_{\rm ESR} = \left(V_{\rm pp} - \frac{V_{\rm OUT}(1-D)}{8f_{\rm SW}^2 LC}\right) \cdot \frac{f_{\rm SW} L}{V_{\rm OUT}(1-D)}. \quad (20)$$

B. Steady-State and Load Transient Response

Fig. 18 shows the steady state of experimental results as the $V_{\rm IN}$ is 5 V and the output voltage $V_{\rm OUT}$ is 1.5 V when the $I_{\rm LOAD}$ is 1.5 A and the switching frequency is 300 kHz. The I_L is the inductor current. The G_H is the driving signal for the high-side MOSFET. Here, the $R_{\rm ESR}$ is about 1 mΩ and the $C_{\rm OUT}$ is

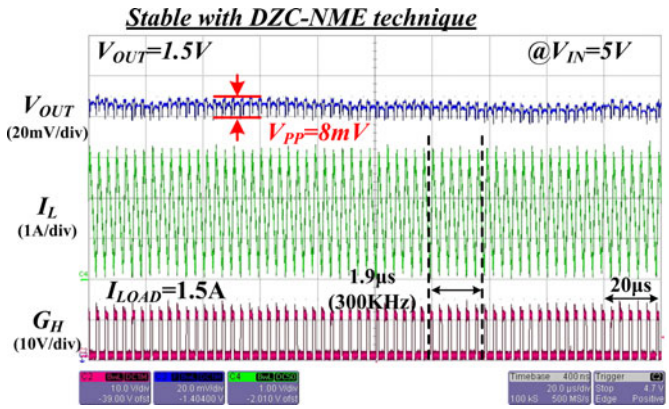

Fig. 19. Regulated waveforms due to the implementation of the DZC-NME technique at $V_{\mathrm{IN}} = 5$ V and $V_{\mathrm{OUT}} = 1.5$ V.

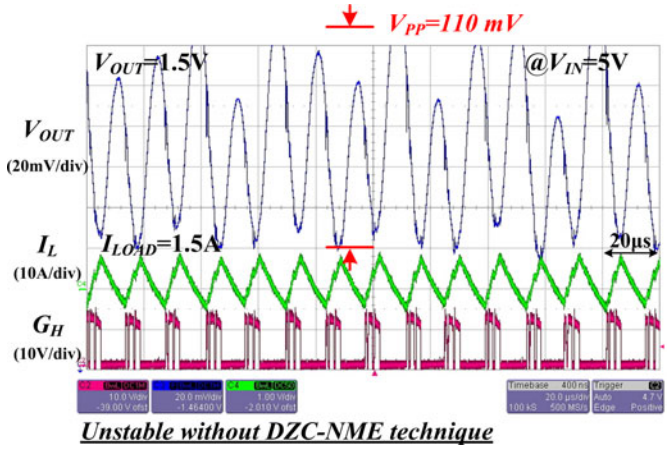

Fig. 20. Unstable waveforms in the COT buck converter without the DZC-NME technique at $V_{\mathrm{IN}} = 5$ V and $V_{\mathrm{OUT}} = 1.5$ V.

220 μF (22 μF $\times$ 10) owing to the use of MLCC. According to the conventional stability criteria shown in (12), the switching frequency should be higher than 2 MHz. However, experimental results show that the system stability is guaranteed even under the low-switching frequency of 300 kHz since the DZC-NME technique can reduce the limitation of the stability criteria. Thus, the switching loss can be greatly reduced. Specially, the voltage ripple at the V_{OUT} can be smaller than 8 mV when the V_{IN} is 5 V. Moreover, the output ripple and the inductor current are out of phase due to the usage of the MLCC.

Figs. 19 and 20 can demonstrate the function of the DZC-NME technique when V_{IN} is 5 V and V_{OUT} is 1.5 V. Fig. 19 shows the stable operation due to the implementation of the DZC-NME technique. Contrarily, with external option set by testing circuit, the subharmonic oscillation waveform happens when the DZC-NME is disabled as shown in Fig. 20. The proposed DZC technique contributes the phase lead to the feedback signal and results in the similar performance that utilizes the output capacitor with large ESR.

Furthermore, if the R_{ESR} is about 1 mΩ, the effect of ESL is more considerable when the V_{IN} is higher than 15 V. The V_{ESL} is 40 mV as shown in Figs. 21 –23. It shows the contribution of the

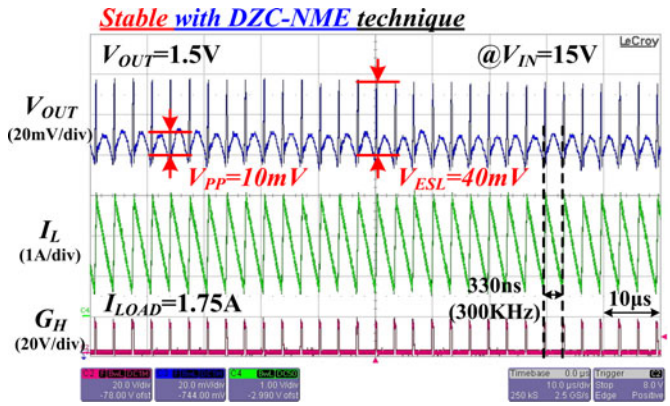

Fig. 21. Regulated waveforms due to the implementation of the DZC-NME technique at $V_{\mathrm{IN}} = 15$ V and $V_{\mathrm{OUT}} = 1.5$ V.

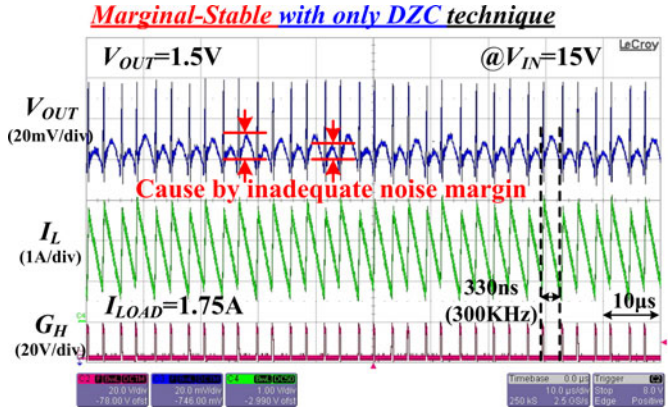

Fig. 22. Marginal stable waveforms with the DZC technique only when the V_{IN} is 15 V and the V_{OUT} is 1.5 V.

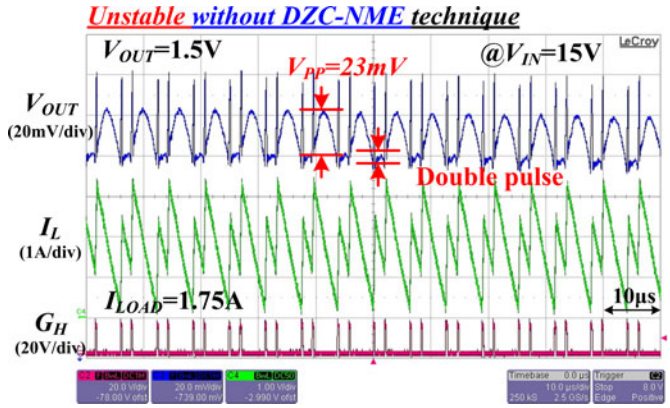

Fig. 23. Unstable waveforms in the COT buck converter without the DZC-NME technique when the V_{IN} is 15 V and the V_{OUT} is 1.5 V.

NME circuit if comparing Fig. 21 with Fig. 22. The system with only the DZC circuit has not enough noise margins so that the V_{OUT} is marginally stable. Fig. 23 shows the seriously unstable waveforms without the aid of the DZC-NME technique.

Fig. 24 shows the waveforms of the V_{OUT} and the inductor current I_L operating at the CCM operation when the load current I_{LOAD} steps from 1 to 8 A, or vice versa. Here, the V_{IN} is 15 V and the V_{OUT} is 1.5 V. Consequently, the switching frequency is

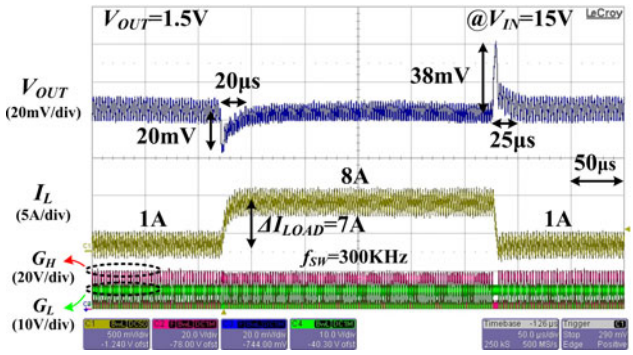

Fig. 24. Load transient response at the CCM operation with the proposed DZC-NME technique.

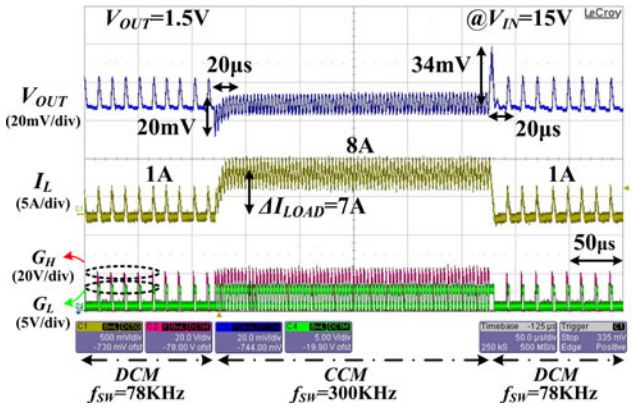

Fig. 25. Load transient response at the DCM operation at light loads with the proposed DZC-NME technique.

TABLE IV
COMPARISONS OF THE PRIOR ARTS

	This work	[15]	[20]
Technology	**0.35µm**	N/A	N/A
Controller Methodology	**Constant on-time**	Constant on-time	V^2C control
Input Voltage (V_{IN})	**15V**	25V	12V
Output Voltage (V_{OUT})	**1.5V**	1.05V	5V
Inductor (L)	**1µH**	N/A	8.6µH
Capacitor (C_O)	**220µF**	220µF	4880µF
Switching Frequency (f_{SW})	**300 KHz**	300 KHz	95.3 KHz
equivalent series resistance (R_{ESR})	**1mΩ**	1mΩ	12 mΩ
Output Voltage Ripple (ΔV_{PP})	**10mV**	17mV	50mV
Highest Efficiency	**91%**	N/A	N/A
Load transient (ΔI_{LOAD})	**7A (1A→8A)**	8A (1A→9A)	14.2A (5A-19.2A)
Recovery Time (T_R)	**25µs**	30µs	80µs

300 kHz. The undershoot voltage and the overshoot voltage are 20 and 38 mV, respectively. The transient recovery time is 20 and 25 μs, respectively. Fig. 25 shows the waveforms operating at DCM at light loads. The switching frequency $f_{\rm SW}$ is scaled down to 78 kHz to enhance efficiency. It is the advantage of the COT control for high efficiency at light loads. Obviously, the system stability can be guaranteed when the output operates under different load condition owing to the implementation of the DZC-NME technique.

C. Comparison With Other Techniques

Table IV lists the comparison result with the prior arts in the design of COT control dc–dc converters. Obviously, the output ripple has been effectively reduced because of using MLCC. The system can also operate at a lower switching frequency when using small ESR. It can demonstrate the high performance achieved by the DZC-NME technique.

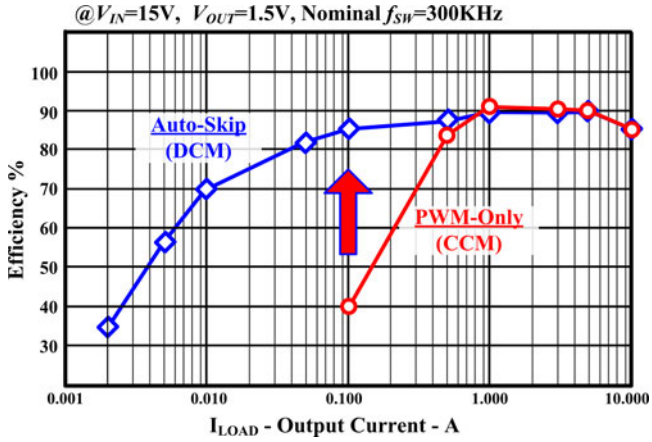

Fig. 26. Power conversion efficiency of the dc–dc converter with the proposed DZC-NME technique.

D. Power Conversion Efficiency and Power Consumption

Fig. 26 shows the power conversion efficiency of the proposed dc–dc converter with the DZC-NME technique. The efficiency can be kept at 91% at medium to heavy loads. The light-load efficiency is deteriorated since the switching loss dominates the total power consumption. However, the efficiency at light loads can be improved by COT control when the converter enables the ZCD circuit and operates at the Auto-Skip mode compared to the converter simply operates the normal PWM-only mode. The proposed buck converter not only works at nearly constant frequency similar to PWM operation but also decreases the switching frequency according to the loading like the PFM operation for high efficiency at light loads.

VI. CONCLUSION

The DZC-NME technique is proposed in this paper to conquer the small ESR value and large ESL effect in the COT buck converter. Even though the MLCC is used as the output capacitor if without conventional ESR compensation, the DZC technique still can increase the system stability since the compensator contributes phase lead similar to the PD controller. Besides, the differential structure can benefit the noise margin to decrease the Jitter and the EMI effects. On the other hand, the NME technique eliminates the effect of ESL to enhance the noise immunity. Furthermore, using the reliable on-time timer with an improved linear function, the near-constant switching frequency, which is adjusted to accommodate to variable input voltage, can further confirm the system stability. Because of MLCC with extremely small $R_{\rm ESR}$ value for general applications, the output ripple can be greatly reduced and thus switching power loss can be decreased in corresponding to large $R_{\rm ESR}$ used to compensate conventional ripple-based control. Experiment results verify the correct and effective functions of the DZC and the NME

techniques at the strict case when small R_{ESR} of 1 mΩ and large V_{ESL} of 40 mV. Without scarifying the inherent advantages of the COT control, the DZC-NME technique for the MLCC applications can ensure low ripple of 10 mV and high efficiency of 91%.

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