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Novel packaging design for high-power GaN-on-Si high electron mobility transistors (HEMTs)

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ABSTRACT

This study describes the development of packaging for high-power AlGaN/GaN high electron mobility transistors (HEMTs) on a silicon substrate. A transistor is attached to a V-grooved copper base, and mounted on a TO-3P lead-frame. Unlike flipchip or copper-molybdenum-copper (CMC)-based packaging technology, which is popular in the GaN HEMT industry, the proposed packaging structure is implemented on the periphery of the surface of the device to promote thermal dissipation from the Si substrate. The various thermal paths from the GaN gate junction to the case dissipate heat by spreading it to a protective coating; transferring it through bond wires; spreading it laterally throughout the device structure through an adhesive layer, and spreading it vertically through the bottom of the silicon chip. The effects of the design of the structure and its fabrication process on the performance of the device and its thermal resistance were studied. Thermal characterization reveals that the thermal resistance from the GaN chip to the TO-3P package was 13.72 °C/W. Self-heating in AlGaN/GaN device structures was measured by infrared (IR) thermography and micro-Raman spectroscopy. Experimental results indicated that a single chip that was packaged in a 5 × 3 mm V-grooved Cu base with a total gate-periphery of 30 mm had a power dissipation of 22 W with a drain bias of 100 V. Both DC and pulsed current–voltage (I_D–V_{DS}) characteristics are measured for a range of transistor structures and sizes, at various of power densities, pulse lengths, and duty factors. These are compared with measured channel temperature profiles.

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1. Introduction

Gallium nitride (GaN) and silicon carbide (SiC) can deliver high voltages, high power densities, high temperatures and high frequencies, making them extremely interesting for potential use in power electronic applications. Electron mobility in GaN exceeds that in SiC, so GaN is preferred for use at high frequency and high power [1]. However, SiC has a greater thermal conductivity than GaN, so SiC devices can theoretically operate at higher power densities than GaN devices. A wide bandgap, high critical field and high thermal conductivity are critical characteristics of a device that is to be operated under continuous wave conditions, dissipating large amounts of thermal energy [2]. The relatively poor thermal conductivity of GaN makes the thermal management of GaN power devices difficult. Junction temperatures must be controlled effectively to guarantee the performance and reliability of components. Many RF transistor package designs use lead-frame and plastic overmolding and have a slug/paddle on the bottom to provide the primary heat removal path. A 100 μm-thick GaN HEMT device with a gate width of 14.4 mm, was mounted on a 60 mm-thick copper-moly-copper package that dissipated 4 W/mm (58 W) [3]. However, many studies of GaN-on-Si HEMTs consider their performance in terms of wafer level but not in terms of the thermal effects of the practical assembly and packaging [4]. High power densities cause significant Joule heating, so temperature and thermal management are critical to designing device packages [5]. The determination of device temperature in designing packaging is also critical to maximizing lifetime and reliability, and device performance must be monitored over time at various temperatures [6,7]. Infrared (IR) thermography yields large-scale temperature maps of device structures and packages during operation. However, Joule heating in an AlGaN/GaN HEMT occurs within 0.5 μm of the drain side of the gate contact, and cannot be measured by IR thermography [8]. One potential consequence is underestimation of the real operating temperature of the device because of the diffraction limit of infrared light [9]. An accurate method for measuring device temperatures is critical to determining the effects of localized self-heating. Micro-Raman spectroscopy with a spatial resolution of 0.5–0.7 μm has been used to obtain temperature line

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scans in the source–drain opening on a micrometer-scale. This work designs a novel package structure for AlGaN/GaN high electron mobility transistors (HEMTs) on an Si substrate in which a V-grooved Cu base and TO-3P lead frame are integrated. The use of V-shaped grooves not only provides an additional thermal path for lateral thermal spreading but also enables precise positioning. The package of the fabricated device is compared with other high-power packages by thermal analysis and micro-Raman/IR thermal imaging, which reveal that the proposed device has a lower thermal resistance of 12.16 °C/W and better thermal conductivity [10,11]. Additionally, the fabrication process may be used to fabricate other packaging lead-frames or power modules. This inexpensive packaging approach is suited to numerous low-cost power-driven applications [12].

2. Fabrication and structure of AlGaN/GaN HEMT device

AlGaN/GaN HEMTs have potential for use in high-power electronic applications at high temperatures. HEMTs were fabricated on various substrates (sapphire, SiC and Si) and electrically characterized. An Si substrate for GaN growth is less thermally conductive than SiC–4H or SiC–6H, as shown in Table 1 [13]. Therefore, thermal management is critical to the design of Si-based GaN HEMTs and their packages [14].

The AlGaN/GaN heterostructure pattern is formed by metal organic chemical vapor deposition (MOCVD) on a 1000 μm-thick silicon substrate. Fig. 1 presents the regular stacking cross-section of the fabricated AlGaN/GaN HEMT structure. The epitaxial structure consisted a 120 nm-thick AlN spacer layer, on which was deposited a 5.5 μm-thick GaN buffer layer, a 25 nm-thick AlGaN barrier layer and finally a 4 nm-thick GaN capping layer. The transistor was fabricated by forming Ohmic contacts in Ti/Al/Ni/Au (20 nm/120 nm/25 nm/5100 nm) multi-layers as well as Ni/Au (20 nm/150 nm)-based Schottky contacts, to produce a smooth surface morphology with low contact resistance. After the ohmic contact had been formed, the device was passivated using a 600 nm-thick Si_3N_4 layer as a passivation layer, grown by plasma-enhanced chemical vapor deposition (PECVD). To improve the device breakdown voltage and the power performance, the field plate electrode was formed on the Si_3N_4 passivation layer and electrically connected to the source electrode. Finally, a 6 μm-thick Au plated air-bridge process was used to connect both sides of the electrode fingers.

An AlGaN/GaN HEMT process was developed and used herein to form devices that were characterized to determine their thermal stability and electrical properties. Device testing revealed the degradation of performance in both dynamic (pulsed current–voltage) and static (DC) operations. Fig. 2 shows the AlGaN/GaN HEMT structure. The studied device layout is composed of 60 gate fingers, each with a gate length of 2 μm and a gate width of 500 μm, yielding a total width of the gate periphery of 30 mm. The active device area is 0.25 mm^2, and a 50 μm pitch separates adjacent gate fingers, and includes source and drain contact regions.

Table 1
Characteristics of substrate materials on which can be grown GaN crystal structure.

Materials property	Si	SiC–4H	SiC–6H	Sapphire	GaN
Bandgap (eV)	1.1	3.26	3.03		3.45
Breakdown field (10^6 V/cm)	0.3	2.2	3.5		3.5–5
Electron mobility (cm^2/V-s)	1450	900	500		2000
Electron saturation velocity (10^7 cm/s)	1	2	2		2.5–2.6
Thermal conductivity (Watts/cm K)	1.5	5	5	0.5	1.3–2.0

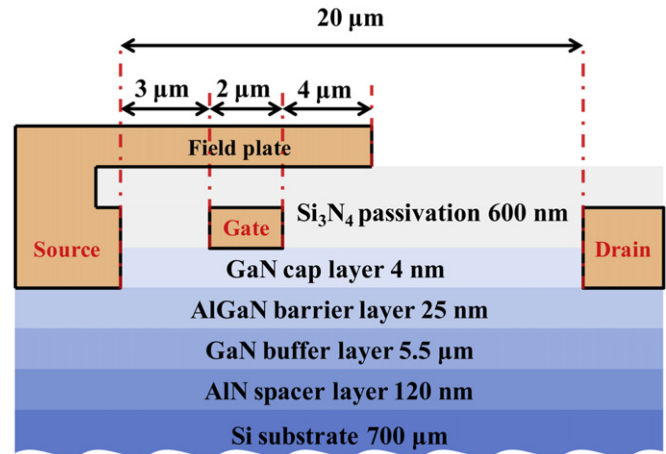

Fig. 1. Cross-section of AlGaN/GaN HEMT with source field plate structure.

3. Package for a discrete GaN HEMT

Improving the thermal performance of electronic components becomes increasingly difficult as their power density is increased and devices become smaller. Thermal management is important in high-power packaging when junctions are to be operated at over 240 °C. Self-heating effects on the transport properties of two-dimensional electron gas (2DEG) influence heat dissipation in HEMT structure, which is related to the maintenance of permitted device junction temperatures that support reliable long-term operation. Most attempts to improve thermal performance have focused on the attachment of a die to a package substrate or a lead-frame by forming a bond using a gold-silicon eutectic [15,16]. However, the solder bump array may only be effective in the micro BGA technique in which the minimum bump size and pitch are 20 μm and 150 μm, respectively [17]. Additionally, because of the

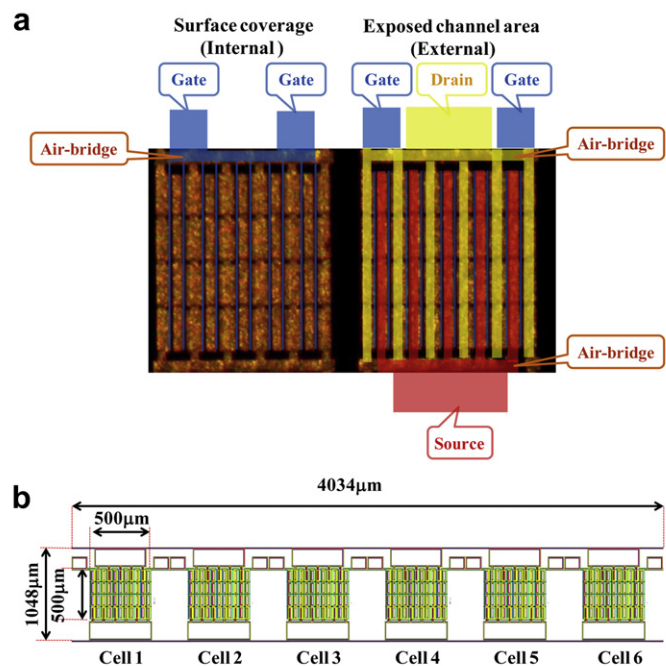

Fig. 2. Photograph and schematic diagram of HEMTs. (a) Photograph of ten-finger HEMT with air-bridge interconnection. (b) Overall die size is 4034 μm × 1048 μm (six cells) × 1 mm (thickness).

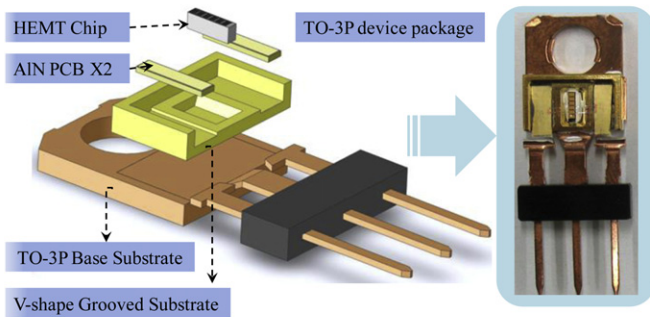

Fig. 3. Discrete GaN HEMT device in TO-3P package.

small dimensions, limitations imposed by material defects and processing are such that the cross-sectional area of the conventional PCB via array is not enough to transfer heat from high-power HEMTs to the ambient environment.

Fig. 3 shows the overall structure of the TO-3P package. Adhesive is used to attach the HEMT to the V-grooved surface; to mount the carrier substrate to the base TO-3P substrate, and to bond the connection directly to the copper substrate (HEMTs to substrate). Fig. 4 presents the packaging process in greater detail. The selection of the adhesive that is used to attach the die is critical to the operation of the device. Highly thermally conductive silver adhesive has a thermal conductivity of over 65 W/mK, and is a viable substitute for traditional thermal interface materials. Finally, thermal management is efficient when silicon-based protective coatings with a thermal conductivity of 0.11 W/mK are exposed.

This work proposes a thermal management solution to minimize thermal resistance and maximize power dissipation. Conventional heat removal paths do not provide a junction-to-case thermal solution that effectively prevents thermally induced failure; the cumulative heat of HEMTs that are operated for prolonged periods can initiate localized thermal degradation. In this work, GaN HEMTs with a gate width of 30 mm are mounted on a V-shaped grooved copper substrate, and attached to a TO-3P package, as shown in Fig. 5. The V-shaped grooved substrate not only provides an additional thermal path for lateral thermal spreading but also supports precise positioning [18]. The microstructure provides increases the surface area of the copper substrate over that achieved using ordinary metals to facilitate thermal management and to reduce the thermal resistance for a given package size.

Fig. 6 shows the extracted total thermal resistance of dies of various thicknesses. The thermal resistance of the TO-3P package is calculated to be 13.72 °C/W, which consists of a junction-to-chip thermal resistance of 11.28 °C/W, a die attachment-related thermal resistance of 1.92 °C/W, and a package-related thermal resistance of 0.52 °C/W [19]. Die thinning influences not only the internal thermal resistance but also the thermal resistance of each package. Reducing the thickness of the HEMT device with a single package from 1 mm to 500 μm reduces the thermal resistance by ~16.8% by reducing the thickness of the silicon wafer. Based on the assumption that the total power dissipation is less than 15 W, the increase in the temperature during a switching operation is less than 200 °C. High-temperature operation of the GaN HEMTs in the TO-3P package without degradation is demonstrated, as will be discussed in the following section.

4. Evaluation of performance of GaN HEMTs with gate width of 30 mm

The fabricated GaN HEMT in a TO-3P package exhibited a favorable tradeoff between the on-resistance and breakdown voltage. Its DC and pulsed current–voltage (I_D–V_{DS}) characteristics were measured using a double-channel source meter at room temperature. The dynamic (pulsed I_D–V_{DS}) characteristics were measured by pulsing the gate voltage, V_{GS}, at a repetition rate of

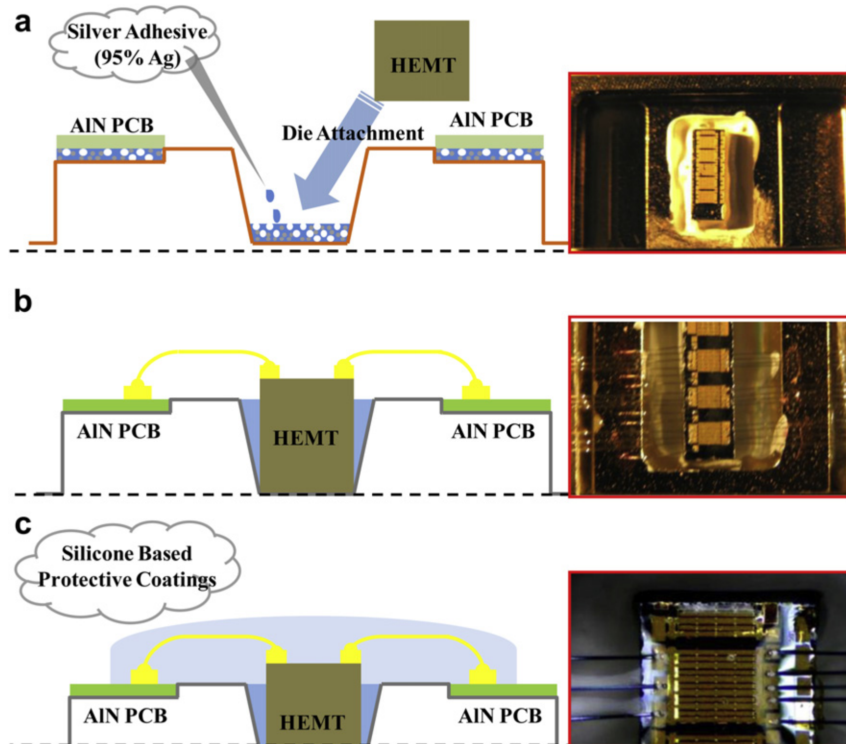

Fig. 4. Assembly and packaging processes for power GaN HEMTs. (a) Adhesive die is attached using silver thermo set paste (95% Ag-filled). (b) Bonding of 0.03 mm diameter gold wires onto pads. (c) Chip carrier with protective coating for use at device surface.

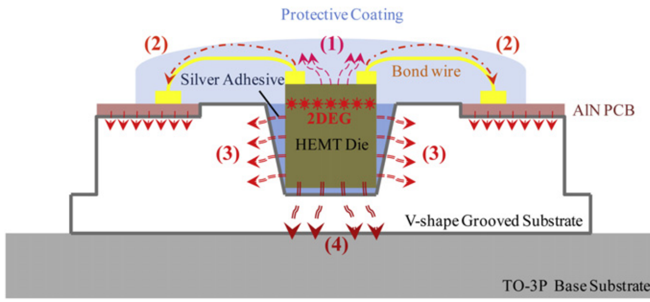

Fig. 5. Various thermal paths from junction to ambient. (1) Spreading to protective coating. (2) Transfer through bond wires. (3) Spreading in lateral device structure through adhesive layer. (4) Spreading of heat on bottom of silicon chip.

100 Hz with a duty cycle of 0.1%. This gate pulse width and duty cycle supported I_D–V_{DS} measurement with negligible trapping and thermal effects [20,21]. Fig. 7 plots the pulsed I_D–V_{DS} measurements under six gate biases. The device draws a maximum current of 2.15 A per cell or 435 mA per mm of the periphery when the gate voltage is set to 1 V. The leakage current in high-voltage switches critically affects the power loss in the system, as plotted in Fig. 8. The off-state drain (I_D) and gate (I_G) currents in the pulsed-mode are 12.5 μA (416 nA/mm) and 13 μA (433 nA/mm) at 100 V, respectively, and the leakage currents are much lower than the on-state drain current, and sufficient for a high-voltage switching application [22,23]. The observed device performance varies within acceptable limits and all devices exhibit stable and reproducible behavior.

Fig. 9 plots the DC I_D–V_{DS} characteristics of the HEMT that were measured under various maximum gate biases (V_{GS}). In this process, V_{DS} was swept from 0 V to V_{DS} (max = 9 V) as V_{GS} was stepped down from −4 V to 1 V. The DC characteristics, plotted as blue solid lines, were obtained with a maximum V_{DS} of 9 V, whereas Fig. 7 (solid red curve) plots the pulse characteristics when the maximum V_{DS} was 10 V. The packaged GaN HEMTs exhibit a DC drain current of 0.205 A/mm at V_{DS} = 4.5 V and V_{GS} = 1 V, which was considerably lower than the pulsed drain current, 0.43 A/mm, at V_{DS} = 8 V and V_{GS} = 1 V. The self-heating effect drastically reduced carrier mobility and thereby reduced the drain current, worsening device performance [23–25]. Also, the two-way operating voltage measurements, plotted in Fig. 9, reveal the temperature and self-heating effects. Each I_D–V_{DS} curve was plotted (V_{DS}

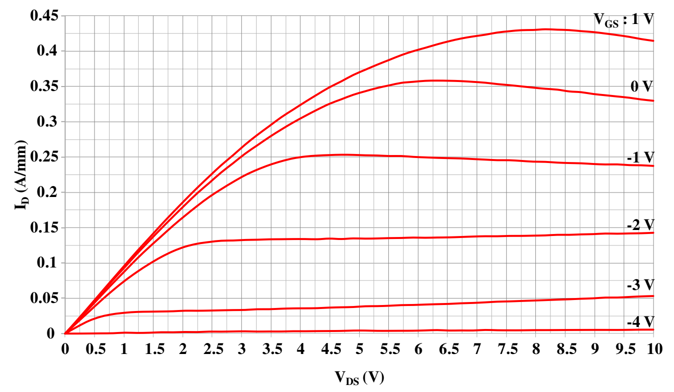

Fig. 7. Pulse I_D–V_{DS} measurements of AlGaN/GaN HEMTs. Gate voltage (V_{GS}) swept from −4 to 1 V in steps of 1 V with pulse time of 200 μs.

from 0 V to 9 V) in separate a pre-sweeping operation, with an upward sweep of V_{DS} from 0 V to 9 V (solid blue) or a downward sweep of V_{DS} from 9 V to 0 V (dashed red). A comparison of these corresponding pairs of curves indicates a 5–10% reduction in peak current density. This effect is considered to have been caused by self-heating during operation at a high drain bias. Additionally, these results reveal another mechanism of the trap-induced OR kink effect. The magnitude of kink is directly related to the drain voltage and current levels during on-state operation. The hot electrons in the 2DEG channel that were generated under a downward sweep of V_{DS} from 9 V to 0 V bias were injected into the GaN buffer layer. Hot electron trapping is posited to be the dominant mechanism of kink generation [26].

5. Experimental validation of GaN HEMTs thermal management

The measurement of temperature is essential to the thermal management in high power GaN HEMTs because localized self-heating during operation under high-voltage switching increases the channel temperature. Since Joule heating is concentrated in a small region on the drain side of the gate, IR microscopy is performed using an IR microscope at 5× magnification, as shown in Fig. 10. The packaged GaN HEMTs are placed into a temperature-controlled heat sink for IR measurement. A thin layer of thermal

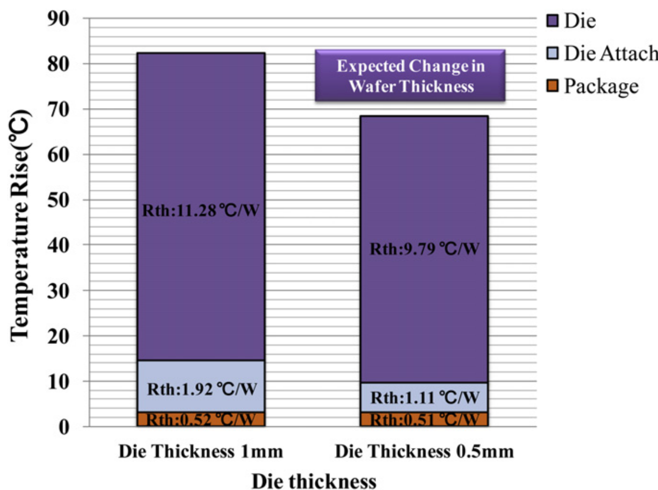

Fig. 6. Effect of thickness on thermal resistance (Rth).

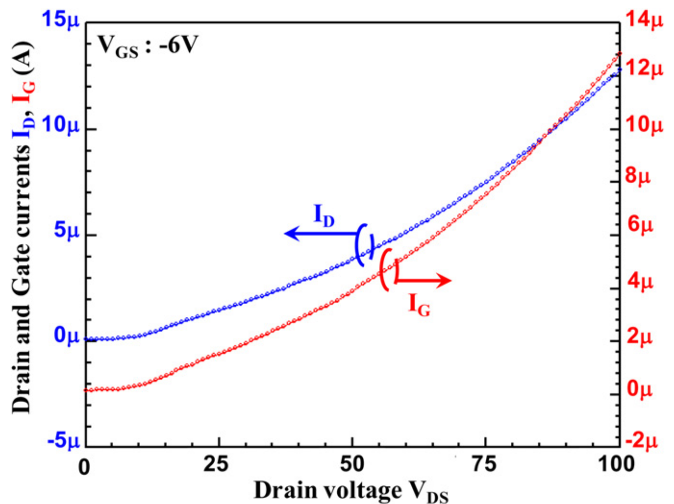

Fig. 8. Off-state I_D–V_{DS} curve of packaged GaN-HEMT at drain voltages of over 100 V.

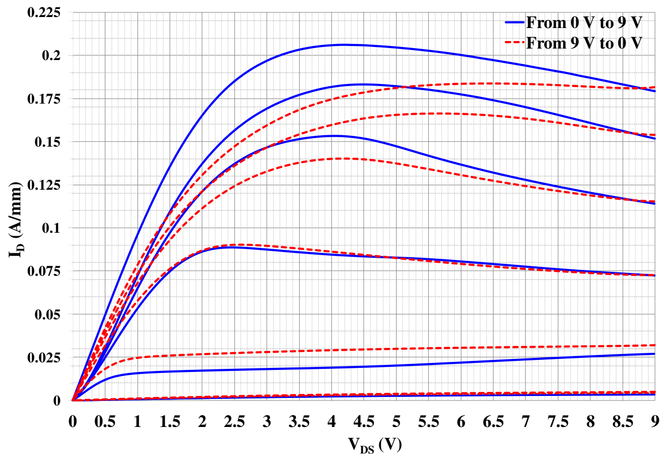

Fig. 9. Each I_D–V_{DS} curve is measured (V_{GS} from −4 V to 1 V) using two bias sweeps – an upward sweep of V_{DS} from 0 V to 9 V (solid blue) and a downward sweep of V_{DS} from 9 V to 0 V (dashed red). (For interpretation of the references to color in this figure legend, the reader is referred to the web version of this article.)

grease is applied to the bottom of the package to reduce the effects of contact resistance at the interface between the package and the heat sink. The thermal behavior of three high-power electronic packages is examined: type I is a CuW flange-based ceramic package (180 W/mK) [27]; type II is a standard dual in-line (DIP) ceramic package (17 W/mK) [28], and type III is a thermally enhanced V-groove-based T0-3P package. Fig. 10 plots the temperature distribution across multi-fingered HEMTs, with the temperature of the base platefixed at 70 °C. The dissipated heat per unit gate width for packages of types I, II, and III is 0.36 W/mm, 0.352 W/mm, and 0.372 W/mm, respectively. In contrast, the V-grooved packaging design provides sufficient thermal conduction to spread heat and remove it from the chip to the package to an extent similar to that achieved using a standard CuW package. Devices attached on T0-3P package type exhibit the temperature peak at 105.1 °C approximately equal that of the temperature peak at 101.6 °C exhibited by devices mounted on CuW package type. The proposed thermal management design considerably improves the spreading of lateral heat by the structure without sacrificing reliability or performance. The same trend is obtained for junction temperatures across the multi-fingers. However, due to the cross-talk effect, temperatures are higher in the central finger. There is a clear improvement from the proper thermal management for extracting heat of the active region, with obvious benefits for device reliability.

In the following experiments, the temperature map and profile across an HEMT structure that is operated under 100 V bias switching conditions are measured. Fig. 11 shows the infrared thermal image that is obtained with a total power dissipation of 0.303 W/mm (or 9 W). The IR imaging is performed with the temperature-controlled heat sink temperature set to 70 °C. The line scan profiles (line trace #1) reveal the increase in temperature along the finger (from source to drain) for the maximum junction temperature of 143.9 °C. The increase in temperature of the middle finger of the device (line trace #2) is negligible. Although the overall temperature gradients exist between adjacent fingers and contribute to averaging effects during IR imaging, the use of IR microscopy is employed to produce device surface to package case temperature differentials, from which junction to case thermal resistance can be calculated. The thermal drop from channel to case is 73.86 °C, yielding a junction temperature of 143.86 °C with a base plate temperature of 70 °C, equating to 12.16 °C/W thermal resistance as established by the IR data. The junction-to-chip thermal spreading resistance, 9.45 °C/W, the die-attach thermal resistance, 2.25 °C/W, and the thermal resistance associated with the thermal spreading of the package, 0.46 °C/W, are determined, when the internal thermal resistance (from junction to case) of the device is very large [29]. Fig. 12 displays the resulting increase in the junction temperature above the package temperature, and a large internal thermal resistance influences the thermal breakdown in each component. The dissipation of power to the package is improved by thinning the chips, and the thermally enhanced packages, which promote thermal management, can be feasibly used in power electronic applications at the minimum allowable chip thickness of 500 μm.

The temperature dependencies of the 2DEG mobility and the supplied power are prerequisites for an advanced HEMT

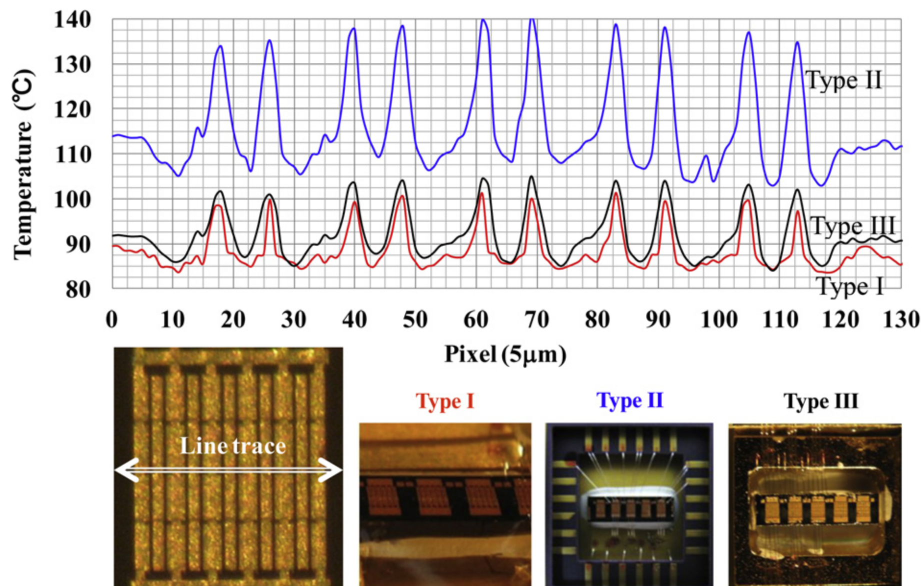

Fig. 10. Junction temperature profiles across active region of AlGaN/GaN HEMTs devices (10 fingers) obtained by infrared thermography. Type I: GaN is mounted on CuW flange-based plates. Type II: GaN is packaged in dual-inline-package lead frame. Type III: GaN is packaged in proposed thermally enhanced TO-3P lead frame.

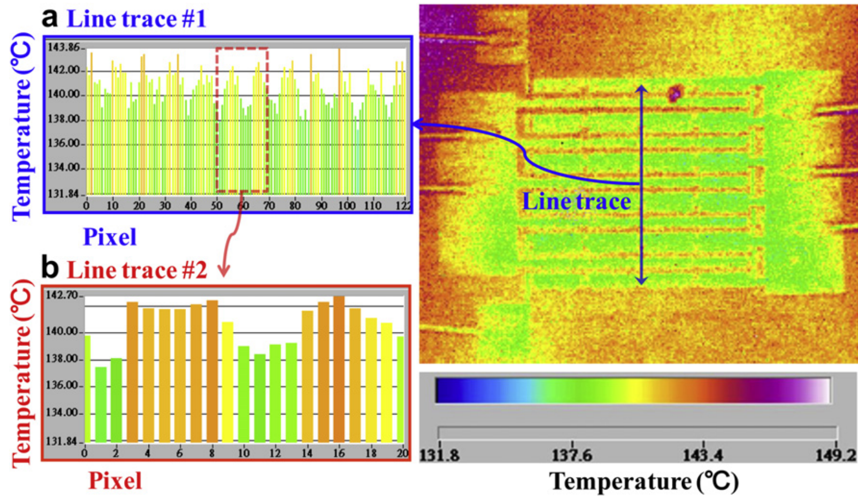

Fig. 11. Thermal maps of a single GaN cell which contains 10 GaN transistors (right), and line scan profiles of thermal map (Line trace #1). Line trace #2 is extracted to show the temperature of middle 2 GaN transistors.

engineering. However, the efficiency of switching of GaN devices for kW power conversion applications remains poor. Heat removal from the 2DEG channel is the main problem. The resultant high-temperature fatigue may cause defects generation and device degradation. To measure and map the temperature distribution with depth in the source-drain channel, *in situ* Raman experiments are conducted using an HeNe (632.8 nm) laser as the excitation source. Raman spectroscopy is used to monitor and calibrate the increase in temperature with a thermal resolution of 5 °C and a spatial resolution of 0.7 μm. Fig. 13 shows the Raman scattering spectrum of the tested AlGaN/GaN HEMT, measured and analyzed thermal expansion and related phonon frequency shifts, under on-state and pinched-off conditions. A strong band is observed at 515–525 cm^{-1} which is the contribution from the Si(111) substrate, and a band at 560–570 cm^{-1} is for the E2 mode of GaN as obtained above. The E2 (high) mode of GaN and Si phonon mode frequencies (Raman shift, or Raman peak position) are selected to be the temperature–sensitive parameter in this work. Raman scattering experiments on GaN film and related Si substrate materials show that the position of this line shifts to lower frequencies as the 2DEG temperature increases. The heat in the transistor is produced in the GaN 2DEG channel by the self-heating effect and a localized hot spot with a diameter of 0.5 μm is found close to the gate contact. Fig. 14 compares the infrared absorption (see Fig. 12 for supporting information) with the Raman spectroscopic images that are obtained from a line scan [9]. The increase in temperature across the source–drain opening is determined using the GaN (E2) phonon mode (Raman), and IR imaging yields a lower peak device temperature, 142.7 °C, (bar chart) than that, 195.6 °C (red line), determined by Raman scattering. As expected, the Fourier-transform infrared and laser-Raman spectra reveal significant temperature deviations (meaning temperature drops of 55 °C) from source–drain temperature distribution. The diffraction-limited resolution of IR, 5–10 μm, is poorer than the spatial resolution, 0.5–0.7 μm, of Raman scattering, causing considerable lateral and depth averaging. Possible consequences are underestimation of the peak temperature of the device and overestimation of its reliability [30].

Fig. 15 presents Raman temperature profiles that were measured in the source–drain opening to elucidate localized self-heating effects during high-voltage (100 V) switching operation.

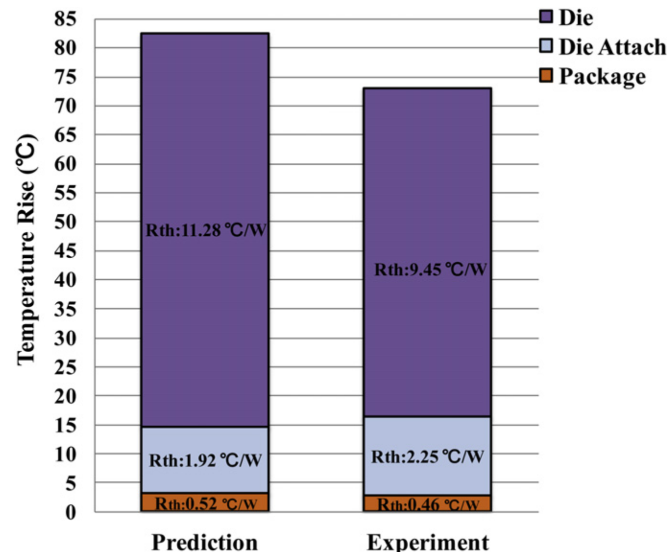

Fig. 12. Comparison between experimentally and theoretically determined thermal resistance of packaged AlGaN/GaN HEMT.

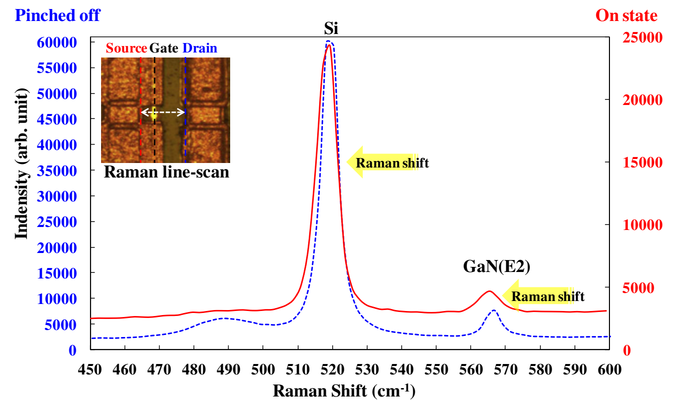

Fig. 13. Raman spectrum of AlGaN/GaN HEMT on silicon substrate with the device is operated under on-state ($V_{GS} = 1$ V, solid line) and pinched off ($V_{GS} = -6$ V, dashed line) conditions. This measurement position is located at the opening of source to drain where no field plate metal is presented on the top of gate. Metal will block from Raman spectrum measurement.

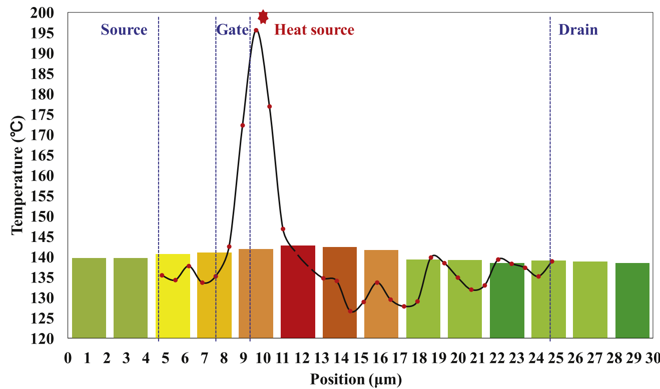

Fig. 14. IR and Raman spectroscopy to elucidate thermal behavior: a comparison with temperature profile in source–drain opening. Dashed line (blue) represents relative position along channel. (For interpretation of the references to color in this figure legend, the reader is referred to the web version of this article.)

The reliability and performance of HEMTs depend critically on the device operating channel temperature. Previous studies have focused on various effects with operating junction temperature. However, the referenced temperature is the base plate temperature. This study presents characterization and comparison of GaN devices at four different levels of power dissipations (W) with varying base plate temperatures (°C) correspond to the actual operating conditions: 1.4 W (50 °C); 3 W (50 °C); 5.1 W (70 °C); and 9 W (70 °C). The results are consistent with the measurements of devices that were operated at 100 kHz and V_{GS} of 1 V. Joule heating clearly occurs adjacent to the drain side of the gate contact on the AlGaN/GaN interface, where the maximum channel temperature also increases from 80.6 to 195.6 °C, corresponding to an increase in the dissipated power of 1.4–9 W, respectively [10,31,32]. The same base plate heating conditions were used for both Raman and IR measurements for consistency and to allow direct comparison of results. The junction temperature of less than 200 °C under worst-case high voltage (100 V) operating conditions is verified. An experimental prototype was designed to demonstrate the electrical and thermal characterization of HEMTs. Based on the proposed design and experiments, power GaN HEMTs that are encapsulated in a V-grooved TO-3P type package can be implemented.

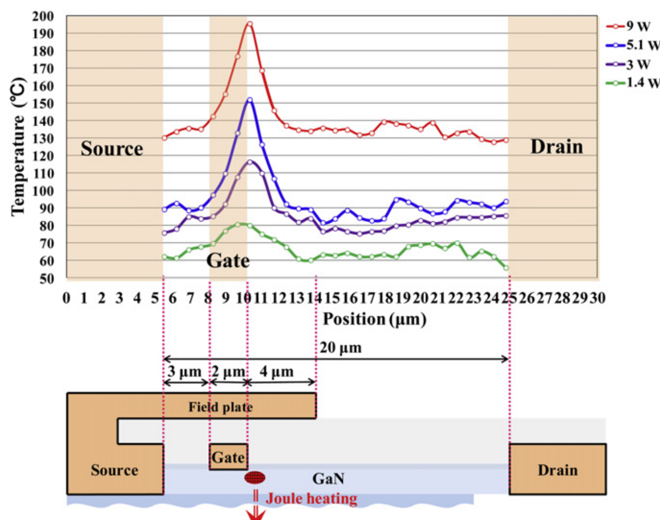

Fig. 15. Raman one-dimensional (line scan) temperature profile in source–drain area of AlGaN/GaN HEMTs that dissipate various powers.

6. Conclusions

This work presents GaN HEMTs that are fabricated on an Si substrate, packaged in a V-grooved copper base and mounted on a TO-3P lead frame. The unique features of the proposed high-power package include a V-shaped grooved platform that provides an additional lateral heat conduction path and novel packaging that simplifies the assembly and test processes. Infrared and Raman spectroscopy and analysis of the thermal behavior of packaged HEMTs demonstrate that the proposed device has improved thermal management and reliability when operated at high voltage. Temperature profiles of the source-to-drain opening are also obtained. The V-grooved packaging approach supports effective thermal management and minimizes self-heating. The difference between the experimental thermal resistance of TO-3P and the theoretically predicted value is less than 11.5%. The Raman-measured peak temperature of the device, 195.6 °C, which is lower than the maximum operating junction temperature, 200 °C, does not cause degradation or reduce reliability. These combined IR/Raman thermal analyses indicate that Joule heating causes the channel temperature to reaches its maximum close to the drain side of the gate contact. This work also examines the degradation of performance, revealed by DC and pulsed I_D–V_{DS} characterization, that is caused by self-heating. The DC drain current of the packaged GaN HEMTs is considerably (52.3%) lower than the pulsed drain current. The design flexibility and increased thermal efficiency of the enhanced V-grooved T0-3P package design were also evaluated to demonstrate the effectiveness of the proposed design in high-power applications.

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