A 10-Bit 300-MS/s Pipelined ADC With Digital Calibration and Digital Bias Generation

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***Abstract*—A 10-bit pipelined ADC was fabricated using a 65 nm CMOS technology. To reduce power consumption, switching opamps are used. These switching opamps are designed to have a short turn-on time. Digital background calibration is employed to correct the A/D conversion error caused by the low dc gain of the opamps. The biasing voltages in each opamp are automatically generated using digital circuits. This bias scheme can maintain the settling behavior of the opamp against process-voltage-temperature variations. At 300 MS/s sampling rate, the ADC consumes 26.6 mW from a 1 V supply. Its measured DNL and INL are +0.52/−0.4 LSB and +0.99/−1.65 LSB respectively. Its measured SNDR and SFDR are 55.4 dB and 67.2 dB respectively. The chip active area is 0.36 mm^2.**

***Index Terms*—Analog-to-digital conversion, analog digital conversion, switching circuits, calibration, digital background calibration, pipeline processing, digital bias generation..**

I. Introduction

PIPELINED analog-to-digital (A/D) conversion technique has been used to realized high-speed high-resolution Nyquist-rate analog-to-digital converters (ADCs). The performances of a pipelined ADC, such as resolution, sampling rate, and power consumption, are mainly determined by its internal multiplying digital-to-analog converters (MDACs). A MDAC is usually a switched-capacitor circuit comprising an opamp, analog switches, and capacitors. Thus, the specifications of the opamps, such as dc gain, speed, and power consumption, are crucial.

To reduce the power consumption of the opamps, opamp sharing scheme [1]–[5] and switching opamp technique [6]–[10] have been proposed. However, the opamp sharing scheme suffers from the memory effect [2], [3]. It also does not conform to the optimized pipeline scaling strategy [11]. For switching opamps, the long turn-on time of waking up from sleep mode to their normal bias condition hinders their operation speed [6], [8]–[10].

To relax the dc gain requirement for the opamps and the matching requirement for the capacitors, digital calibration techniques has been proposed [12]–[17]. Those calibration schemes can make the ADCs less sensitive to process, temperature, and supply voltage (PVT) variations. It is desirable that the calibration operates in the background without interrupting the normal ADC operation. It is also desirable that the accompanied modification to the circuit does not degrade the performance of the analog signal path.

In this paper, we use switching opamps to implement the MDACs [18]. These switching opamps are designed to have a short turn-on time. The use of these switching opamps also eliminates the input sampling switches of the following pipeline stage. We then apply digital background calibration to correct the A/D conversion error caused by the low dc gain of the opamps. The acquired calibration data are also used to monitor the settling behavior of the opamps. The bias currents in the opamps are then automatically adjusted such that the settling behavior of the opamps is maintained. No external bias generator is required. To demonstrate the above techniques, a 10-bit pipelined ADC was designed and fabricated using a 65 nm CMOS technology. Operating at 300 MS/s sampling rate, the ADC consumes 26.6 mW from a 1 V supply. It achieves a signal-to-noise-plus-distortion ratio (SNDR) of 55.4 dB and a spurious-free dynamic range (SFDR) of 67.2 dB.

The organization of this paper is described as follows. Section II shows the architecture of this pipelined ADC and its pipeline stage. Section III describes the design of the switching opamps. Section IV explains the principle of the digital background calibration and its implementation. Section V describes the technique to automatically control the bias current of the opamps. Section VI describes the common-mode feedback scheme for the proposed switching opamps. Section VII describes the design of the comparators for the sub-ADC. Section VIII details experimental results. Finally, Section IX draws conclusions.

II. ADC Architecture

Fig. 1 shows the architecture the reported pipelined ADC. There are five pipeline stages followed by a 4-bit flash ADC. For the j-th pipeline stage where $j = 1, \ldots, 5$, its analog processor (AP) receives the V_j analog signal from the $(j-1)$-th stage and generates the V_{j+1} analog output to be processed by the $(j+1)$-th stage. Each pipeline stage also includes a digital calibration processor (CP) and an encoder. They combine the D_j digital signal from the AP and the $D_{o,j+1}$ digital signal from the $(j+1)$-th stage to produce the $D_{o,j}$ digital output. Their function is to ensure that $D_{o,j}$ is an accurate digital representation of V_j.

Fig. 2 shows the detailed schematic of the j-th pipeline stage. Its corresponding transfer characteristic is shown in Fig. 3. Its

Manuscript received January 17, 2012; revised November 21, 2012; accepted November 21, 2012. Date of publication January 04, 2013; date of current version February 20, 2013.This paper was approved by Associate Editor Roland Thewes. This research was supported by the National Science Council (Grant NSC-101-2221-E-009-161) of Taiwan, R.O.C.

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Digital Object Identifier 10.1109/JSSC.2012.2233332

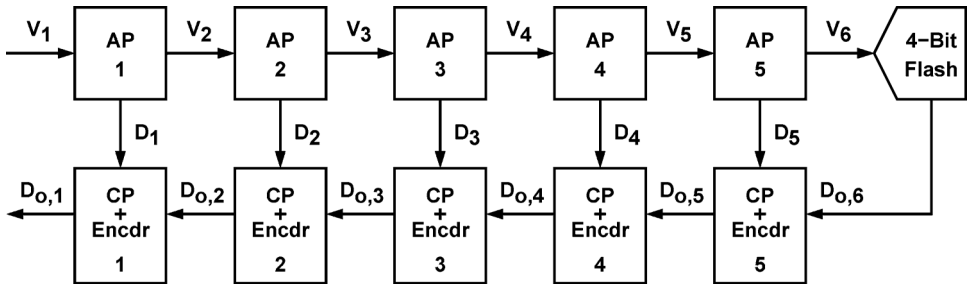

Fig. 1. Architecture of the reported pipelined ADC.

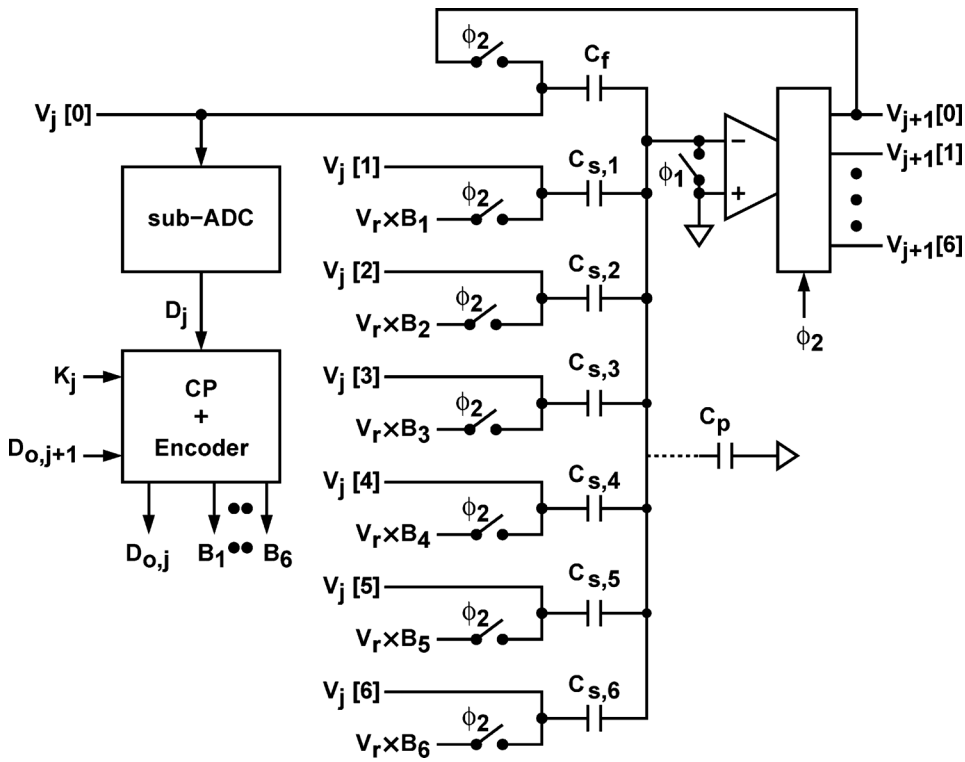

Fig. 2. Block diagram of the j-th pipeline stage.

AP includes a sub-ADC and a MDAC. The MDAC, consisting of an opamp, analog switches, and capacitors, implements the functions of a sub-DAC and a residue amplifier. The analog switches are controlled by two non-overlapping clocks, ϕ_1 and ϕ_2. During $\phi_1 = 1$, the voltage V_j is sampled on capacitors $C_f, C_{s,1}, C_{s,2}, \ldots, C_{s,6}$. During $\phi_2 = 1, C_f$ becomes a feedback capacitor, and each $C_{s,i}$, where $i = 1, 2, \ldots, 6$, is connected to a $V_r \times B_i$ reference. The value of B_i is among $\{-1, 0, +1\}$. The $C_{s,i}$ capacitors form the sub-DAC, whose output is controlled by the digital inputs B_1 to B_6.

The opamp shown in Fig. 2 has 7 outputs, $V_{j+1}[0]$ to $V_{j+1}[6]$. The opamp is activated by clock ϕ_2. When $\phi_2 = 0$, its outputs are separated and are floating. When $\phi_2 = 1$, its outputs are tied together and are equal to V_{j+1}. For the $(j-1)$-th stage, its opamp is activated by ϕ_1. When $\phi_1 = 1$, its outputs $V_j[0]$ to $V_j[6]$ are all equal to V_j. They are sampled onto capacitors $C_{s,1}$ to $C_{s,6}$ respectively. When $\phi_1 = 0$, nodes $V_j[0]$ to $V_j[6]$ are separated and floating. They are no sampling switches between the opamp and the capacitors $C_{s,1}$ to $C_{s,6}$, which introduce additional opamp loading and additional signal-path delay.

The sub-ADC comprises 13 comparators with thresholds at $0, \pm(1/8)V_r, \pm(2/8)V_r, \ldots, \pm(6/8)V_r$ respectively. Its digital output, D_j, is an estimate of the V_j input. The mapping from V_j to D_j is shown in Fig. 3. The value of D_j is among $\{\pm 0, \pm 1, \pm 2, \ldots, \pm 6\}$. The two zeros, -0 and $+0$, are used to distinguish the polarity of V_j. Detailed sub-ADC design will be given in Section VII.

The pipeline stage includes a CP and an encoder that generate the digital output $D_{o,j}$ and the sub-DAC control signals B_1 to B_6. When $K_j = 0$, the calibration operation for the j-th stage is disabled. The signal set $\boldsymbol{B} = [B_1, B_2, \ldots, B_6]$ forms a thermometer code of D_j. For example, if $D_j = +2$, then $\boldsymbol{B} = [+1, +1, 0, 0, 0, 0]$. If $D_j = -4$, then $\boldsymbol{B} = [-1, -1, -1, -1, 0, 0]$.

Assume the opamp in Fig. 2 is linear and has a finite dc gain of A_0. Its output during $\phi_2 = 1$ can be expressed as

$$V_{j+1} = \hat{G}_j \times \left[V_j - \hat{V}_j^{\mathrm{da}} - \hat{V}_j^{\mathrm{os}} \right] \tag{1}$$

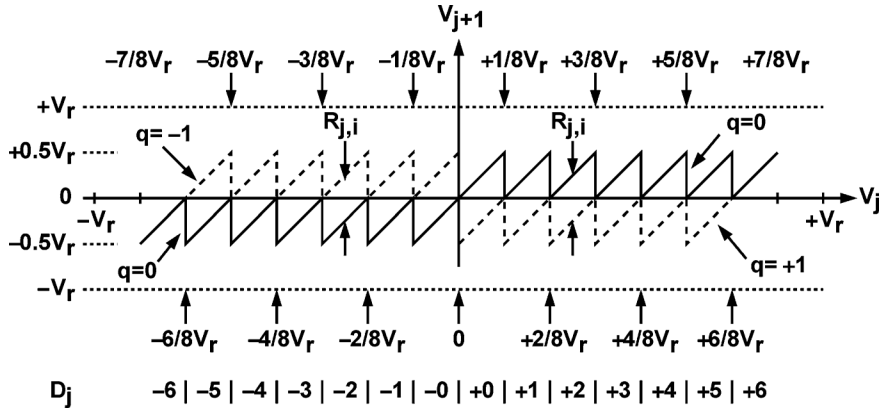

Fig. 3. Transfer curve of the j-th pipeline stage.

with

$$\hat{G}_j = \frac{C_s + C_f}{C_f} \times \frac{1}{1 + \frac{1}{A_0} \cdot \frac{C_s + C_f + C_p}{C_f}} \tag{2}$$

$$\hat{V}_j^{\mathrm{da}} = V_r \times \sum_{i=1}^{6} \frac{C_{s,i} \cdot B_i}{C_s + C_f} \tag{3}$$

$$C_s = C_{s,1} + C_{s,2} + \cdots + C_{s,6} \tag{4}$$

In the above equations, $\hat{G}_j$ is the realized MDAC gain. $\hat{V}_j^{\mathrm{da}}$ is the output of the sub-DAC. C_p is the total parasitic capacitance at the opamp's input. $\hat{V}_j^{\mathrm{os}}$ represents the offset of the MDAC.

For an ideal case, $\hat{V}_j^{\mathrm{os}} = 0$, $A_0 = \infty$, and $C_{s,i} = (1/2)C_f$ for all i. Then, the MDAC gain is $G_j = 4$. The sub-DAC's output is $V_j^{\mathrm{da}} = (V_r/8)D_j$. The ideal V_j-to-V_{j+1} transfer function is shown as the solid line in Fig. 3. In reality, the offset $\hat{V}_j^{\mathrm{os}}$ is non-zero, the opamp gain A_0 is finite, and the capacitance $C_{s,i}$ randomly deviates from the $(1/2)C_f$ nominal value. Also shown in Fig. 3 are a dashed-line V_j-to-V_{j+1} transfer function and a parameter q. They are introduced by the digital calibration of Section IV.

The complexity of both sub-ADC and sub-DAC in Fig. 2 is twice as large as those in a conventional pipeline stage with a MDAC gain of 4. These are the overhead for enabling digital background calibration without increasing the MDAC's output range [17]. However, the total $C_s + C_f$ capacitance in Fig. 2 remains the same value as that of a conventional design. Thus, the speed of the analog signal path is only degraded slightly due to the increase in input capacitance of the sub-ADC. Digital background calibration is described in Section IV.

III. Switching Opamp

Fig. 4 shows the schematic of the switching opamp used in Fig. 2. It is a two-stage cascaded amplifier. The input stage comprises a source-coupled pair M1-M2 and nMOST loads M3 and M4. It provides a voltage gain of 2.1. The output stage comprises two common-source amplifiers M5 and M6. They include current sources M7 to M10 as active loads. The output stage provides a voltage of 10.8. The dominant pole of this opamp is located at outputs of the output stage and the non-dominant pole is at the outputs of the input stage. We traded the dc gain of the input stage for frequency of the non-dominant pole so that the opamp does not need additional capacitor for frequency compensation. When used in the first-stage MDAC, this opamp achieves a unity-frequency of 3.2 GHz with a phase margin of 81°, while consuming 3.1 mW.

In Fig. 4, analog switches S1 to S4 are inserted in the opamp for power control. When the switch control ϕ is low, the opamp is turned off. A power saving of 50% is achieved by setting ϕ low when the opamp is not in use. There are 7 sets of (S1A, S2A, S1B, S2B) switches. S1A to S2A are pMOSTs. S1B and S2B are nMOSTs. When ϕ is low, each opamp output rail is split into seven isolated nodes, i.e., $V_{o,p}[i]$ and $V_{o,n}[i]$, where $i = 0, 1, \ldots, 6$. This split-output arrangement eliminates the input sampling switches in the next pipeline stage.

This opamp exhibits a very short turn-on time when ϕ changes from low to high. It does not have frequency-compensation capacitors that need to be recharged. Simulations show that the opamp turn-on time is less than 0.2 nsec, when the opamp is in an open-loop configuration and the differential input is zero.

The power-controlling switches S1A, S2A, S1B, and S2B in Fig. 4 also function as the input sampling switches of the following pipeline stage. Fig. 5 shows the cascade of the $(j-1)$-th pipeline stage and the j-th pipeline stage. From the $(j-1)$-th stage, its positive outputs, $V_{j,p}[0]$ to $V_{j,p}[6]$, and its negative output, $V_{j,n}[0]$ to $V_{j,n}[6]$, are connected to the C_f and $C_{s,1}$ to $C_{s,6}$ capacitors in the j-th stage respectively. When $\phi_1 = 1, V_{j,p} = V_{j,p}[0] = \ldots = V_{j,p}[6]$ and $V_{j,n} = V_{j,n}[0] = \ldots = V_{j,n}[6]$. Voltages $V_{j,p}$ and $V_{j,n}$ are sampled onto the C_f and C_s capacitors in the j-th stage without additional sampling switches in front of the capacitors. The differential voltage $V_j = V_{j,p} - V_{j,n}$ is digitized by the sub-ADC, yielding D_j. The CP then uses D_j to generate the sub-DAC digital inputs B_i, where $i = 1, \ldots 6$. The sub-DAC is realized using switch boxes $\mathrm{SB1}[i]$ and $\mathrm{SB2}[i]$. $\mathrm{SB1}[i]$ is connected to $V_{j,p}[i]$ and controlled by B_i. $\mathrm{SB2}[i]$ is connected to $V_{j,n}[i]$ and controlled by $\overline{B}_i$. When $\phi_1 = 0$, the opamp in the $(j-1)$-th stage is disabled and its outputs are floating. When $\phi_2 = 1$, the sub-DAC switch boxes are activated. Consider the $\mathrm{SB1}[i]$ switch box. It connects $V_{j,p}[i]$ to V_{RT} if $B_i = +1$, or to V_{RM} if $B_i = 0$, or to V_{RB} if $B_i = -1$. In this design, $V_{RT} = 0.95$ V, $V_{\mathrm{RM}} = 0.5$ V, and $V_{RB} = 0.05$ V, making $V_r = 0.9$ V.

In the first pipeline stage, boosted nMOST switches are added in front of each C_f and $C_{s,i}$ capacitors. They function as

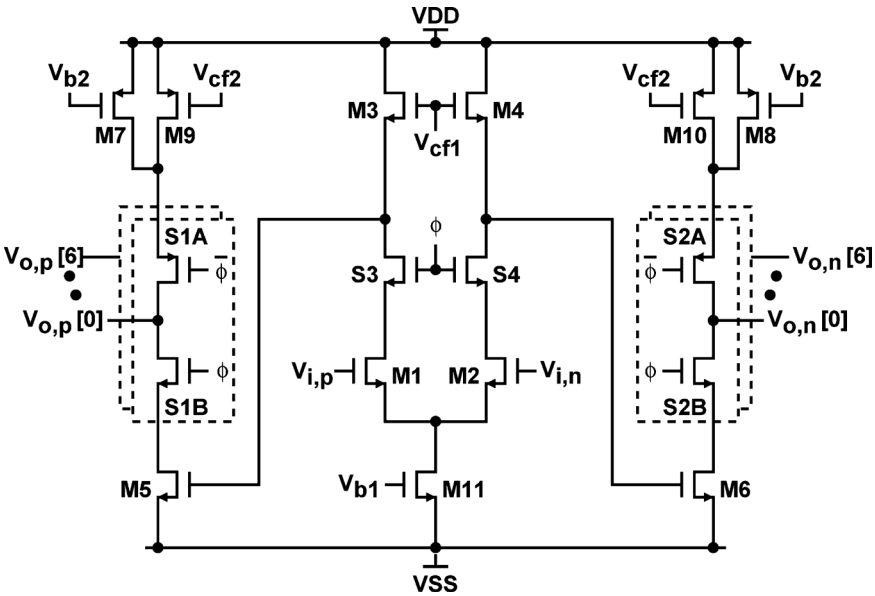

Fig. 4. Schematic of the switching opamp.

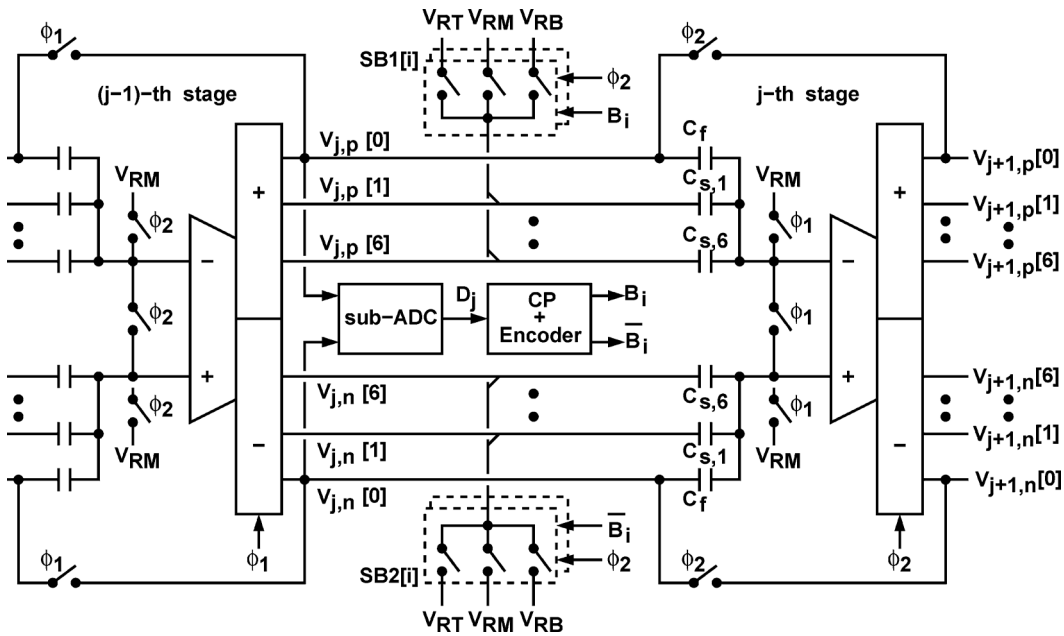

Fig. 5. Cascade of the $(j-1)$-th pipeline stage and the j-th pipeline stage.

the analog input samplers for the ADC. There is no additional sample-and-hold circuit.

IV. Digital Background Calibration

Equation (2) and (3) show that finite opamp gain A_0 and capacitor $C_{j,i}$ mismatch degrade the accuracy of the MDAC gain $\hat{G}_j$ and the sub-DAC output $\hat{V}_j^{\mathrm{da}}$. Calibration is required to correct these errors. Furthermore, the opamp of Fig. 4 can only provide a low voltage gain. Continuous calibration against voltage and temperature variations is necessary.

In the j-th pipeline stage shown in Fig. 2, the CP carries out the digital background calibration for the j-th stage. This CP controls the sub-DAC through B_1 to B_6 to dynamically alternate the AP's V_j-to-V_{j+1} transfer function. It then extracts the calibration data from the resulting $D_{o,j+1}$ data stream [16], [17]. The encoder in Fig. 2 uses the acquired calibration data to generate the digital output $D_{o,j}$, which should be an accurate digital representation of the analog input V_j. The CP can operate without interrupting the normal ADC operation.

In the following subsections, Section IV-A shows a mathematical treatment of the reported calibration scheme. Both the calibration data and the encoder function will be defined. Section IV-B shows how the CP controls the sub-DAC to enable background calibration. Section IV-C describes how the CP extracts the calibration data.

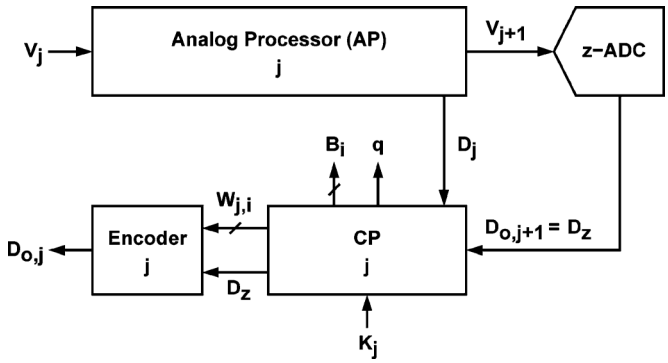

Fig. 6. Configuration for the j-th stage calibration.

A. Calibration Principle

Fig. 6 illustrates the operation of the j-th pipeline stage. The sub-ADC in the AP quantizes the analog input V_j and generates a corresponding digital code D_j. The sub-DAC in the AP is controlled by the CP through the control signals B_i where $i = 1, \ldots, 6$. The AP generates the analog signal V_{j+1} as expressed in (1). The V_{j+1} is then digitized by a back-end ADC, called z-ADC, which comprises the succeeding stages starting from the $(j+1)$-th pipeline stage to the final flash ADC. The digital output from the z-ADC is $D_{o,j+1}$. The encoder in the j-th stage combines this $D_{o,j+1}$ with data from the CP to generate the $D_{o,j}$ digital output. To simplify denotation, instead of $D_{o,j+1}, D_z$ is used as the z-ADC's digital output for the rest of this paper.

Let the A/D conversion of the z-ADC be linear and expressed as

$$V_{j+1} = \frac{1}{\hat{G}_z} \times D_z + O_z + Q_z \tag{5}$$

This V_{j+1}-to-D_z conversion exhibits a conversion gain of $1/\hat{G}_z$, an offset of O_z, and a quantization error of Q_z.

For a specific i, where $i = 1, 2, \ldots, 6$, define $R_{j,i}$ as the V_{j+1} variation when the signal B_i in Fig. 2 is changed by 1, i.e.,

$$R_{j,i} = \hat{G}_j \times V_r \times \frac{C_{s,i}}{C_s + C_f} \tag{6}$$

We define the calibration data for the j-th stage, $W_{j,i}$, as the digital value of $R_{j,i}$ when it is digitized by the z-ADC, i.e.,

$$W_{j,i} = \hat{G}_z \times R_{j,i} \tag{7}$$

The encoder combine $D_z, W_{j,i}$, and B_j to generate $D_{o,j}$. We define the encoder function as

$$D_{o,j} = \sum_{i=1}^{6} (B_i \times W_{j,i}) + D_z \tag{8}$$

It can be shown that the relationship between the stage analog input V_j and the stage digital output $D_{o,j}$ is

$$V_j = \frac{1}{\hat{G}_j \hat{G}_z} \times D_{o,j} + \left[\hat{V}_j^{\text{os}} + \frac{O_z}{\hat{G}_j} \right] + \frac{Q_z}{\hat{G}_j} \tag{9}$$

Note that (9) is arranged in a form similar to (5). This V_j-to$D_{o,j}$ A/D conversion is also linear, but exhibits a new conversion gain of $1/(\hat{G}_j \hat{G}_z)$, a new offset of $\hat{V}_j^{\text{os}} + O_z/\hat{G}_j$, and a quantization error of $Q_z/\hat{G}_j$. The quantization error is reduced by the stage gain $\hat{G}_j$. Both the unknown MDAC gain $\hat{G}_j$ and the unknown sub-DAC output $\hat{V}_j^{\text{da}}$ do not affect the linearity of (9) as long as the calibration data $W_{j,i}$ are accurate.

Thus, calibrating the j-th stage is to acquire $W_{j,i}$ for each $i = 1, 2, \ldots, 6$. Referring to Fig. 1, the entire pipelined ADC is calibrated backward and sequentially. A calibration cycle begins with calibrating the 5-th stage with the final flash ADC as the z-ADC, i.e., $D_z = D_{o,6}$. The acquired $W_{5,i}$ data are stored and used in the $D_{o,5}$ encoding. Once the calibration of the 5-th stage is completed, the calibration of the 4-th stage is initiated, while the 5-th stage and the final flash ADC are served as the z-ADC, i.e., $D_z = D_{o,5}$. The process continues toward the 1st stage. One calibration cycle is completed when the calibration procedure reaches the 1st stage.

B. Dynamic AP Control

In Figs. 6 and 2, if $K_j = k \neq 0$, then the j-th stage is under calibration. Its CP dynamically alternates the V_j-to-V_{j+1} transfer function of the AP. The CP then extract $W_{j,k}$ from the resulting $D_{o,j+1}$ data stream. The whole calibration can operate without interrupting the normal A/D operation.

In the $K_j = k$ calibration mode, the CP isolates the $C_{s,k}$ capacitor and makes the remaining $C_{s,i}$ capacitors provide the D_j-to-$\hat{V}_j^{\text{da}}$ conversion. For example, if $k = 2$, then, the signal set $\boldsymbol{B} = [B_1, B_3, B_4, B_5, B_6]$ forms a thermometer code of D_j, excluding B_2. This D_j-to-$\hat{V}_j^{\text{da}}$ conversion has an input range of $|D_j| \leq 5$. When $D_j = +6$, all B_i signals including B_2 are set to $+1$. When $D_j = -6$, all B_i signals are set to -1.

When $K_j = k$, the excluded control signal B_k adopts the value of a random sequence q, i.e., $B_k = q$. The value of q is among $\{-1, 0, +1\}$. The sequence q changes its value every clock cycle. But the change depends on D_j. When $+0 \leq D_j \leq +5$, q switches randomly between $+1$ and 0. When $-5 \leq D_j \leq -0$, q switches randomly between -1 and 0. However, when $D_j = +6, q$ is frozen as $q = +1$. When $D_j = -6, q = -1$. All correlation-based calibrations require no correlation between V_j and q. To avoid the correlation, two separate random number generators are used in our design, which are q_1 and q_2. The value of q_1 is among $\{0, +1\}$, and the value of q_2 is among $\{0, -1\}$. When $+0 \leq D_j \leq +5, q_1$ is activated and $q = q_1$. When $-5 \leq D_j \leq -0, q_2$ is activated and $q = q_2$.

When the AP is under the above control scheme, its V_j-to-V_{j+1} transfer function becomes

$$V_{j+1} = \underbrace{\hat{G}_j \times \left[V_j - \hat{V}_j^{\text{da}} - \hat{V}_j^{\text{os}} \right]}_{Y'} - R_{j,k} \times q \tag{10}$$

where $R_{j,k}$ is defined in (6) with i replaced by k. Compared to (1), a $R_{j,k} \times q$ random sequence is added to the regular V_{j+1} output. The Y' in (10) is defined as the V_j-dependent component in V_{j+1}. The resulting V_j-to-V_{j+1} transfer function is shown in Fig. 3. The sequence q dynamically changes the transfer function while confining the V_{j+1} output between $\pm 0.5 V_r$. When $q = 0$, the solid line is the transfer function, which is also the V_j-to-Y' transfer function. When $D_j \geq +0$ and $q = +1$, the dashed line is the transfer function, which is shifted downward

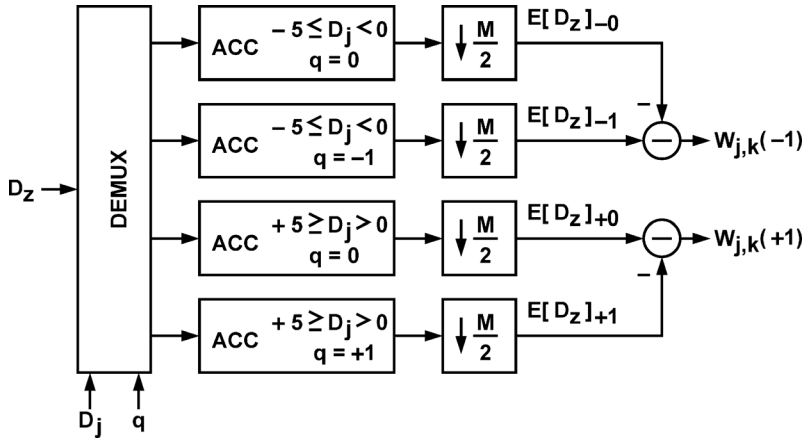

Fig. 7. A correlation-based $W_{j,k}$ extractor.

from the solid line by an amount of $R_{j,k}$. When $D_j \leq -0$ and $q = -1$, the dashed line is the transfer function, which is shifted upward from the solid line by an amount of $R_{j,k}$.

C. Correlation-Based Calibration Data Extraction

In Figs. 6 and 2, if $K_j = k \neq 0$, the CP dynamically alternates the AP's V_j-to-V_{j+1} transfer function. The voltage V_{j+1} is digitalized by the z-ADC. The corresponding digital value D_z is received by the CP. In Fig. 3, for either $-5 \leq D_j \leq -0$ or $+0 \leq D_j \leq +5$, the V_{j+1} average height for the $q = 0$ solid line is different from the V_{j+1} average height for the $q = -1$ or $q = +1$ dashed line by an exact amount of $R_{j,k}$.

The parameter $W_{j,k}$ is a digitized value of $R_{j,k}$. It is extracted from D_z using the $W_{j,k}$ extractor shown in Fig. 7. Each of its D_z input is associated with a D_j value and a q value. The extractor first sorts the D_z samples based on D_j and q. The D_z samples associated with $D_j = \pm 6$ are discarded. The sorted D_z samples are then accumulated separately by using 4 accumulators (ACCs). To complete one extraction, M samples of D_z are needed, where M is the period of the pseudo random sequences q_1 and q_2. In one q_1 period, there are $M/2$ instants with $q_1 = +1$ and $M/2$ instants with $q_1 = 0$. In one q_2 period, there are also $M/2$ instants with $q_2 = -1$ and $M/2$ instants with $q_2 = 0$. The accumulation-and-dump operation depicted in Fig. 7 acquires an average of the sorted samples. The results are $E[D_z]_{-1}, E[D_z]_{-0}, E[D_z]_{+0}$, and $E[D_z]_{+1}$, which are corresponding to the V_{j+1} average heights in different V_j range and different q values. From (10) and (5), they can be expressed as:

$$\begin{aligned}
(1/\hat{G}_z) \times E[D_z]_{+0} + O_z &= E[Y'] \\
(1/\hat{G}_z) \times E[D_z]_{+1} + O_z &= E[Y'] - R_{j,k} \\
(1/\hat{G}_z) \times E[D_z]_{-0} + O_z &= E[Y'] \\
(1/\hat{G}_z) \times E[D_z]_{-1} + O_z &= E[Y'] + R_{j,k} \qquad (11)
\end{aligned}$$

Thus, $W_{j,k}(+1) = E[D_z]_0 - E[D_z]_{+1} = \hat{G}_z R_{j,k}$, and $W_{j,k}(-1) = E[D_z]_{-1} - E[D_z]_{-0} = \hat{G}_z R_{j,k}$. Both $W_{j,k}(+1)$ and $W_{j,k}(-1)$ acquire the same $W_{j,k}$ parameter. Using both $W_{j,k}(+1)$ and $W_{j,k}(-1)$ extractors can overcome the situation in which V_j is always positive or always negative. If V_j is always negative, although the $W_{j,k}(+1)$ extractor cannot collect enough valid D_z samples to extract $W_{j,k}$, the $W_{j,k}(-1)$ extractor can produce the same $W_{j,k}$ in the expected time period.

Note that V_j is unknown and may change every clock cycle when the normal A/D conversion operates at the same time. We assume that V_j is statistically stationary and is not correlated with the random sequence q. so that different $E[Y']$ in (11) is identical. Note that the quantization error Q_z in (5) is eliminated due to averaging, and the offset O_z is eliminated by the subtraction shown in Fig. 7.

To complete the j-th stage calibration, the K_j calibration control is varied from 1 to 6 sequentially, so that all $W_{j,i}$ calibration data are acquired, where $i = 1, 2, \ldots, 6$. When a stage is under calibration, it can still perform its nominal A/D conversion, i.e., converting V_j to $D_{o,j}$. The digital output $D_{o,j}$ is generated by employing (8) with the previously acquired $W_{j,i}$ data.

The correlation-base data extraction scheme requires a minimal M to achieve an accurate $W_{j,k}$ extraction. If the z-ADC has a resolution of Z bits, then the minimum value for M is 2^{2Z-2} [17]. In this design, $M = 2^{18}$, thus, at 300 MS/s sampling rate, it takes 26 msec to calibrate 5 pipeline stages to complete one calibration cycle.

V. Digital Bias Generation

Consider the switching opamp shown in Fig. 4. This opamp requires biasing voltages V_{b1} and V_{b2}. Voltage V_{b1} is generated from a digital common-mode feedback to ensure a specified output common-mode voltage of $V_{o,n}$ and $V_{o,p}$ when the opamp is active. Its generation is described in Section VI. The voltage V_{b2} controls the bias current of the M5–M6 output stage, which takes up 75% of the overall opamp current. In our design, this V_{b2} is not derived from external reference. It is automatically generated by a local digital bias generator. This bias generator detects the settling behavior of the opamp and then adjusts V_{b2} to ensure sufficient speed for the opamp at minimum power dissipation.

The digital bias generation scheme is described in the following subsections. Section V-A introduces the concept of settling detection. Section V-B shows the implementation of the digital bias generator.

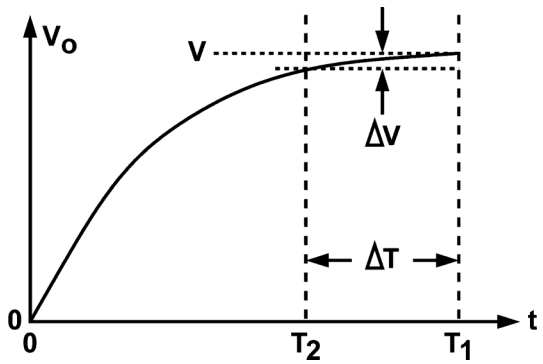

Fig. 8. V_o time-domain step response.

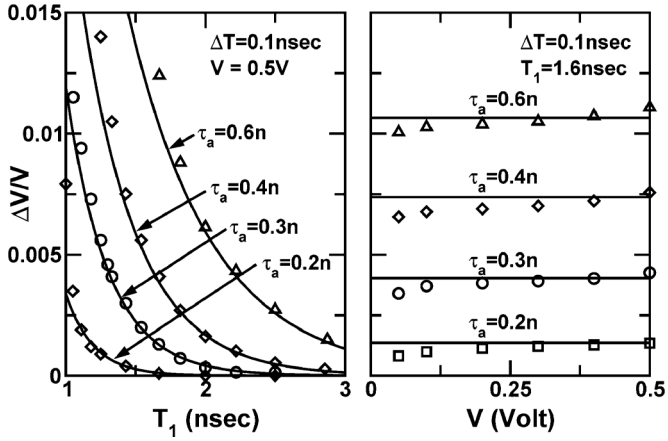

Fig. 9. $\Delta V/V$ ratio versus amplification time T_1 and output amplitude V.

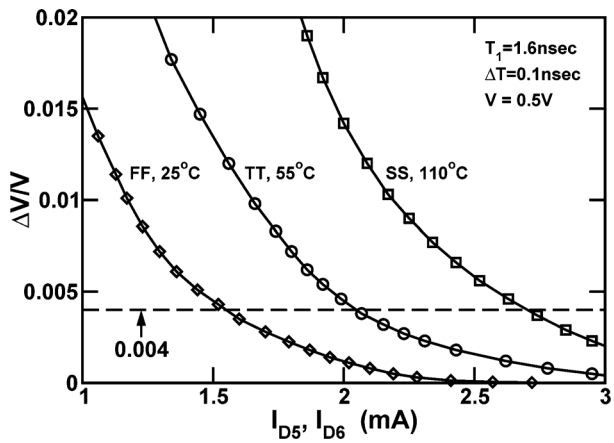

Fig. 10. $\Delta V/V$ ratio versus bias currents I_{D5} and I_{D6}.

A. Detection of Opamp Settling

The opamp shown in Fig. 4 has its open-loop dominant poles reside at its output nodes. The dominant-pole frequency (ω_p) is proportional to the transconductances of M5 and M6, which are determined by the bias currents of M5 and M6. When the opamp is used in the MDAC configuration shown in Fig. 2, the time-domain step response of its outputs can be approximated by

$$V_o(t) = V_{j+1} \times (1 - e^{-t/\tau_a}) \tag{12}$$

where V_{j+1} is the steady-state output and τ_a is the time constant of the MDAC. Since τ_a is proportional to $1/\omega_p$, We can adjust τ_a by varying the bias current of M5 and M6.

Consider the V_o step response shown in Fig. 8. At T_1 amplification time, $V_o(T_1) = V$. If the amplification time is reduced to $T_2 = T_1 - \Delta T$, $V_o(T_2)$ becomes $V - \Delta V$. From (12), we have

$$\frac{\Delta V}{V} = \frac{\Delta T}{\tau_a} \times e^{-T_1/\tau_a} \tag{13}$$

The above equation shows that the ratio $\Delta V/V$ is linearly proportional to ΔT and independent of V. For a given ΔT, $\Delta V/V$ can be used to evaluate the settling behavior of the opamp.

Fig. 9 shows the $\Delta V/V$ behavior of the MDAC in the 1st pipeline stage. The $\Delta V/V$ ratio is plotted against various T_1 and V. The opamp's output stage is biased at various current, yielding different τ_a. The solid lines are calculation using (13) with extracted τ_a. The symbols are SPICE simulation results, which agree well with (13). For this opamp design, slew does not dominant the opamp's transient behavior. Fig. 10 plots the simulated $\Delta V/V$ ratio against the bias currents of the opamp's output stage, I_{D5} and I_{D6}. The opamp is configured as the MDAC of the 1st pipeline stage. Simulation conditions include different temperature and different process corner. For the opamp to maintain a constant settling behavior with $\Delta V/V = 0.004$, I_{D5} and I_{D6} may vary from 1.54 mA to 2.74 mA.

B. Digital Bias Generator

The V_{b2} bias generator (VBG) for the j-stage's opamp of Fig. 4 operates as follows. It first set the amplification time for the opamp as T_1. The digital calibration described in Section IV is applied to the j-th pipeline stage. The acquired calibration data are denoted as $W_{j,i}(T_1)$. The VBG then changes the amplification time for the opamp to $T_2 = T_1 - \Delta T$. The corresponding calibration data are denoted as $W_{j,i}(T_2)$. From (13), we have

$$\frac{W_{j,i}(T_1) - W_{j,i}(T_2)}{W_{j,i}(T_1)} = \frac{\Delta W_{j,i}}{W_{j,i}} = \frac{\Delta V}{V} = \frac{\Delta T}{\tau_a} \times e^{-T_1/\tau_a} \tag{14}$$

The VBG compares the ratio $\Delta W_{j,i}/W_{j,i}$ to a specified constant R_w, which is a digital representation of $\Delta V/V$. It then adjusts the biasing voltage V_{b2} based on the comparison result. The bias current of the opamp's output stage and the settling time constant τ_a are adjusted when V_{b2} is varied. This control mechanism makes $\Delta W_{j,i}/W_{j,i}$ approximate R_w so that it keeps τ_a to a specified value.

The VBG controls the opamp's amplification time through clock buffer. Fig. 11 shows the non-overlapping two-phase clock generator that drives the pipeline stage of Fig. 2. The line delays T_a and T_b are controlled respectively by D_a and D_b from the VBG. If $T_a = T_b = T_{d1}$, then both ϕ_1 and ϕ_2 clocks have an activation time of T_1 and a non-overlapping time of T_{d1}. If $T_a = T_{d2}$ and $T_b = T_{d1}$, where $T_{d2} > T_{d1}$, then the ϕ_1 activation time remains as T_1 and the ϕ_2 activation time

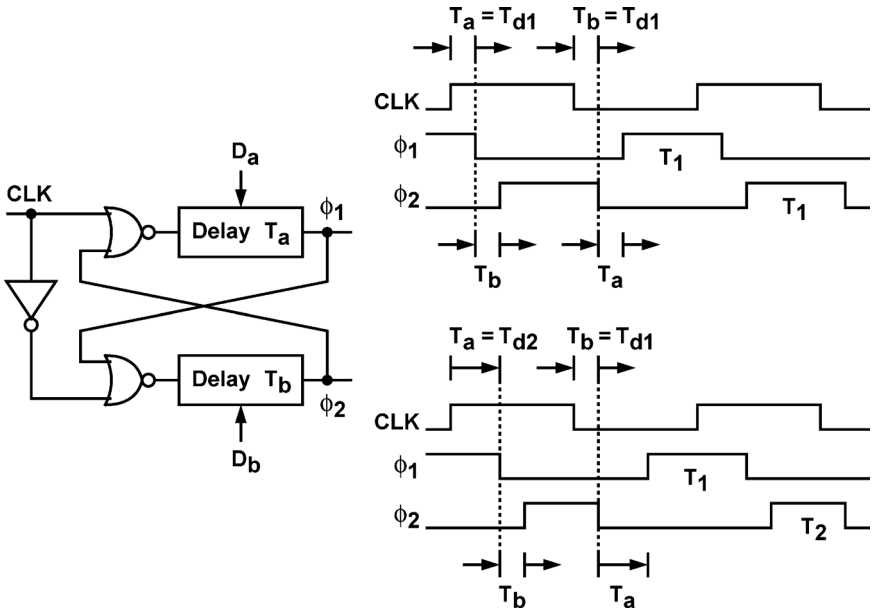

Fig. 11. The non-overlapping two-phase clock generator with variable delay lines.

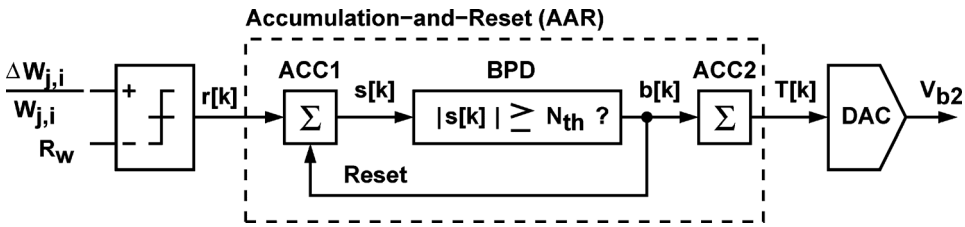

Fig. 12. Digital V_{b2} bias generator.

becomes $T_2 = T_1 - \Delta T$ where $\Delta T = T_{d2} - T_{d1}$. The ϕ_2 activation time is the opamp's amplification time.

Fig. 12 shows the block diagram of the VBG for the j-th stage. The ratio $\Delta W_{j,i}/W_{j,i}$, where $i = 1, \ldots, 6$, is acquired by the CP when the stage is under calibration. The ratio $\Delta W_{j,i}/W_{j,i}$ is compared to a constant R_w. The comparison result $r[k] \in \{-1, +1\}$ is integrated on an accumulator ACC1 followed by a binary peak detector (BPD). ACC1 and BPD together perform the accumulation-and-reset (AAR) operation [19], [20] to reduce the noise effect. The AAR operation is described as follows. Accumulator ACC1 accumulates the $r[k]$ sequence. Its output $s[k]$ is monitored by the BPD with a threshold $N_{\rm th} > 0$. Whenever $s[k]$ reaches either $+N_{\rm th}$ or $-N_{\rm th}$, the BPD issues an output $b[k] = +1$ or $b[k] = -1$ for one clock cycle respectively and then reset $s[k]$ to 0. The BPD output $b[k]$ remains at 0 when no reset occurs. Following $b[k]$ is another accumulator, ACC2, that accumulates the $b[k]$ sequence. Its output $T[k]$ is converted into voltage V_{b2} by a resistor-string DAC.

Note the above V_{b2} adjustment operates in the background. The opamp must deliver the final voltage output V_{j+1} with the required accuracy regardless its amplification time is either T_1 or $T_2 = T_1 - \Delta T$. Thus, it is necessary to choose a ΔT small enough so that $\Delta V/V$ is less than $1/2^{Z-1}$, assuming the back-end z-ADC has a resolution of Z bits. Consider a 10-bit 300-MS/s pipelined ADC and its 1st pipeline stage is under calibration. If $T_1 = 1.6$ nsec and $\tau_a = 0.4$ nsec, then we want $\Delta T < 90$ psec to achieve $\Delta V/V < 1/2^8$.

Since the scheme in Fig. 12 is a digital control of finite resolution, after the control loop converges, $\Delta W_{j,i}/W_{j,i}$ will fluctuate around R_w, i.e., $\Delta V/V$ will fluctuate around the desired value. The control resolution is determined by the LSB size of the DAC, ΔV_{b2}. Usually we want a ΔV_{b2} small enough so that the variation in $\Delta V/V$ is less than $1/2^{Z+2}$ when V_{b2} is changed by one ΔV_{b2}. In our design, $\Delta V_{b2} = 8$ mV. There are 60 control steps for the V_{b2} DAC, yiedling a 480 mV adjustable range for V_{b2}.

The threshold $N_{\rm th}$ of the BPD in Fig. 12 determines the converging time of the control loop. A control with larger $N_{\rm th}$ has better noise immunity but exhibits longer converging time. It takes at least $2MN_{\rm th}$ clock cycles to adjust V_{b2} by one ΔV_{b2}. In our design, $N_{\rm th} = 8$.

VI. Common-Mode Feedback

Fig. 13 redraws the switching opamp of Fig. 4. It contains switched-capacitor common-mode feedback (CMFB) for the opamp, including capacitors C_{m1}, C_{m2}, C_{m3}, and C_{m4}, and pMOST switches S5, S6, and S7. When $\phi_2 = 1$, the opamp is activated. The opamp's output common-mode variation is sensed by C_{m1} and C_{m2}, yielding V_{cf1}. It is also sensed by C_{m3} and C_{m4}, yielding V_{cf2}. The V_{cf1} loop is the main CMFB.

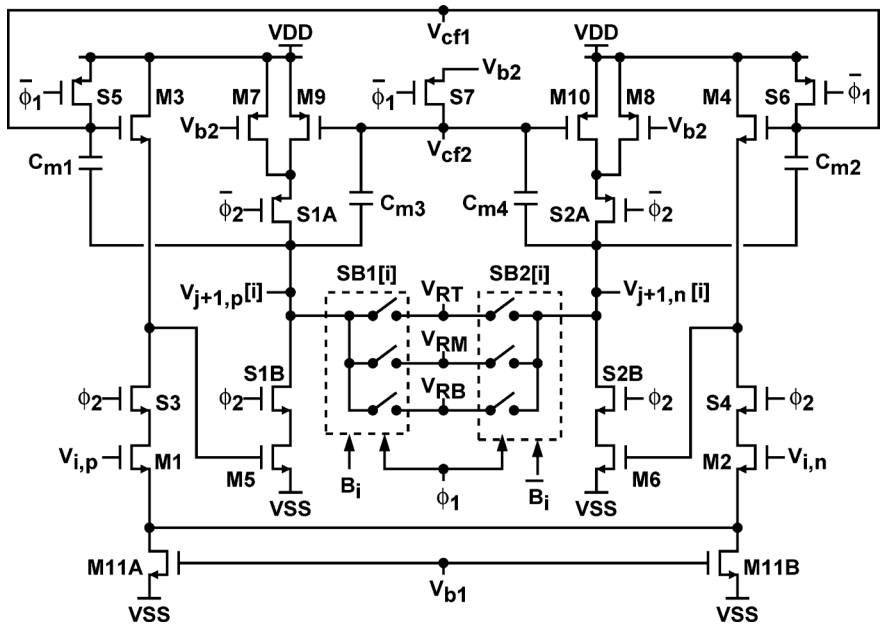

Fig. 13. Opamp common-mode feedback.

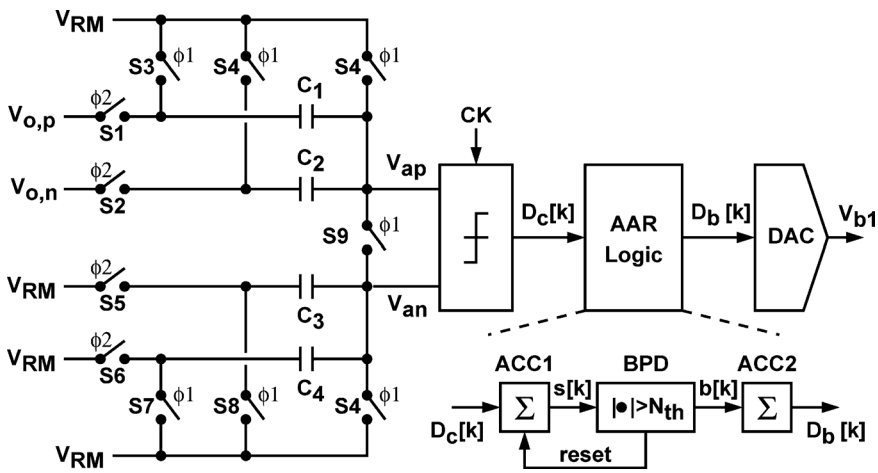

Fig. 14. Digital common-mode feedback control.

The V_{cf2} loop, which has a lower loop gain and only one pole, is added to improve the phase margin of the overall CMFB.

When $\phi_2 = 0$, the opamp is disabled. All its outputs, $V_{j+1,p}[i]$ and $V_{j+1,n}[i]$, where $i = 0, \ldots, 6$, are separated and floating. When $\phi_1 = 1, V_{cf1}$ is charged to $V_{\rm DD}$ and V_{cf2} is charged to the bias voltage V_{b2}. In addition, the sub-DAC in the $(j+1)$-th pipeline stage, shown as the switch boxes $\mathrm{SB1}[i]$ and $\mathrm{SB2}[i]$, is also activated. Nodes $V_{j+1,p}[i]$ and $V_{j+1,n}[i]$ are connected to complementary reference voltages respectively, thus their common-mode voltage is always $V_{\rm RM}$. By choosing $V_{\rm RM}$ as the desired opamp's output common-mode voltage, the output common-mode voltage of the opamp, $V_{o,\rm cm} = (V_{o,p} + V_{o,n})/2$, shows little transient fluctuation during opamp switching.

The CMFB provided by both the V_{cf1} and V_{cf2} loops is high speed but of low loop gain. It cannot cover the entire PVT variations and V_{b2} adjustment. We add a digital CMFB (DCMFB) that generates the biasing voltage V_{b1} for the opamp shown in Fig. 13. The voltage V_{b1} determines the common-mode voltage of the input stage (M1–M4), which decides the common-mode voltage of the output stage (M5–M8), $V_{o,\rm cm}$. Fig. 14 shows the block diagram of the DCMFB. It senses $V_{o,\rm cm}$ of the activated opamp and compares $V_{o,\rm cm}$ with $V_{\rm RM}$. It uses the comparison result to adjust V_{b1} to keep $V_{o,\rm cm}$ close to $V_{\rm RM}$. During ϕ_1, its front-end switched-capacitor circuit is reset. During ϕ_2, the opamp is active, its $V_{o,\rm cm}$ appears as V_{ap} in Fig. 14. The reference $V_{\rm RM}$ also appears as V_{an}. At the end of ϕ_2, a latch-type comparator compares V_{ap} with V_{an}. The comparison result $D_c[k]$ is processed by an accumulation-and-reset (AAR) logic similar to the one described in Section V-B. Its digital output $D_b[k]$ drives a resistor-string DAC that outputs V_{b1}.

VII. Capacitor-Interpolation Sub-ADC

The sub-ADC shown in Fig. 2 is a flash ADC consisting of 13 comparators. The comparators compare the input V_j with thresholds at $0, \pm(1/8)V_r, \pm(2/8)V_r, \ldots, \pm(6/8)V_r$

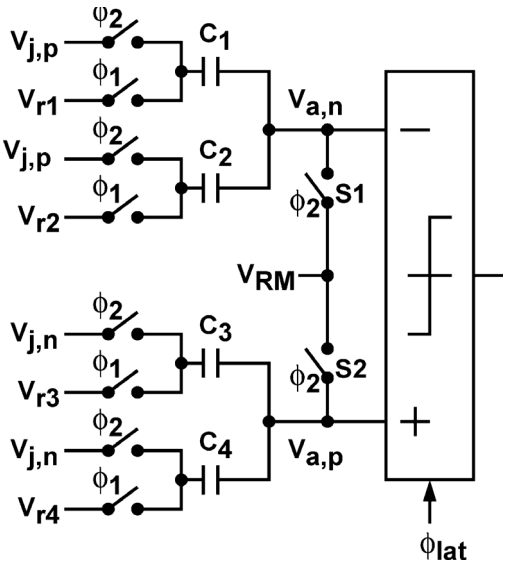

Fig. 15. Sub-ADC comparator with switched-capacitor interpolating input network.

respectively. Instead of using a resistor string to generate the thresholds, we employ the switched-capacitor technique to interpolate all thresholds from 3 reference voltages [21]. This technique is more efficient in terms of power and area. Fig. 15 shows the switched-capacitor network at the comparator input. When $\phi_2 = 1, V_j$ is sampled onto capacitors C_1, C_2, C_3, and C_4. When $\phi_1 = 1$, the capacitors are connected to references V_{r1}, V_{r2}, V_{r3}, and V_{r4} respectively. We have

$$V_a = V_{a,p} - V_{a,n} = (V_{j,p} - V_{j,n}) - V_{\rm th} = V_j - V_{\rm th} \quad (15)$$

where

$$V_{\rm th} = \frac{V_{r1} \cdot C_1 + V_{r2} \cdot C_2}{C_1 + C_2} - \frac{V_{r3} \cdot C_3 + V_{r4} \cdot C_4}{C_4 + C_4} \quad (16)$$

The threshold $V_{\rm th}$ can be varied by changing V_{r1}, V_{r2}, V_{r3}, and V_{r4}. For this design, $C_1 = C_3 = 3C, C_2 = C_4 = 1C$. Possible references are $V_{RT}, V_{\rm RM}$, and V_{RB}, with $V_{RT} - V_{RB} = V_r$ and $(V_{RT} + V_{RB})/2 = V_{\rm RM}$. Table I shows the reference assignment for each comparator with different threshold. In this design, $V_{RT} = 0.95$ V, $V_{\rm RM} = 0.5$ V, and $V_{RB} = 0.05$ V, making $V_r = 0.9$ V. Note that the input common-mode voltage, $(V_{a,p} + V_{a,n})/2$, is different for different comparator. It varies from 0.27 V to 0.49 V.

The analog input of the ADC is sampled directly by its first pipeline stage. The sample-and-hold operation of the capacitors C_s and C_f in Fig. 2 and that of the capacitors C_1, C_2, C_3 and C_4 in Fig. 15 are synchronized. Capacitances are $C_f = 120$ fF, $C_{s,i} = 60$ fF, $C_1 = C_3 = 30$ fF, and $C_2 = C_4 = 10$ fF. The total single-ended input capacitance of the ADC is 730 fF, of which the 1st-stage sub-ADC takes up 250 fF.

For other pipeline stages, the reference-interpolating network for their sub-ADCs are similar to the one shown in Fig. 15 but with modified clocking scheme. References V_{r1} to V_{r4} are sampled when S1 and S2 are turned on. Input V_j is active only when S1 and S2 are turned off. This arrangement reduce the total input capacitance of sub-ADC to 20 fF seen by the opamp of the preceding stage.

TABLE I
COMPARATOR REFERENCE ASSIGNMENT

ID	V_{th}	V_{r1}	V_{r2}	V_{r3}	V_{r4}
+6	$+(6/8)V_r$	V_{RT}	V_{RB}	V_{RB}	V_{RB}
+5	$+(5/8)V_r$	V_{RT}	V_{RB}	V_{RB}	V_{RM}
+4	$+(4/8)V_r$	V_{RT}	V_{RB}	V_{RB}	V_{RT}
+3	$+(3/8)V_r$	V_{RM}	V_{RB}	V_{RB}	V_{RB}
+2	$+(2/8)V_r$	V_{RM}	V_{RB}	V_{RB}	V_{RM}
+1	$+(1/8)V_r$	V_{RM}	V_{RB}	V_{RB}	V_{RT}
0	0	V_{RM}	V_{RM}	V_{RM}	V_{RM}
−1	$-(1/8)V_r$	V_{RB}	V_{RT}	V_{RM}	V_{RB}
−2	$-(2/8)V_r$	V_{RB}	V_{RM}	V_{RM}	V_{RB}
−3	$-(3/8)V_r$	V_{RB}	V_{RB}	V_{RM}	V_{RB}
−4	$-(4/8)V_r$	V_{RB}	V_{RT}	V_{RT}	V_{RB}
−5	$-(5/8)V_r$	V_{RB}	V_{RM}	V_{RT}	V_{RB}
−6	$-(6/8)V_r$	V_{RB}	V_{RB}	V_{RT}	V_{RB}

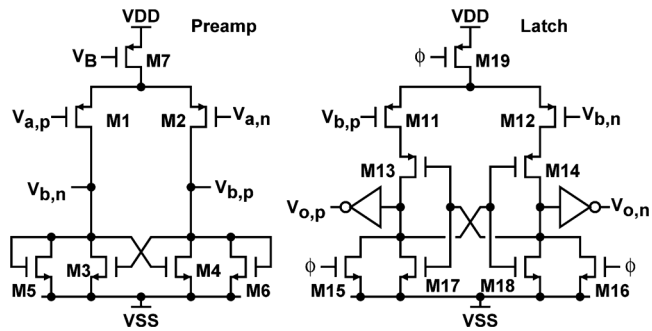

Fig. 16. Comparator schematic.

Fig. 16 shows the schematic of the comparator of the sub-ADC in the 1st pipeline stage. It comprises a low-gain preamplifier and a regenerative latch. Operating at 300 MS/s, the entire sub-ADC consumes 0.78 mW of power. For the rest of the pipeline stages, comparators are regenerative latches without these preamplifiers. Each sub-ADC consumes 0.12 mW of power.

VIII. EXPERIMENTAL RESULTS

This ADC prototype was fabricated using a 65 nm CMOS technology. Fig. 17 shows the ADC chip micrograph. The core area is 0.56×0.66 mm^2. The digital calibration processors and the digital bias generators were all integrated on the same chip. The digital calibration described in Section IV is applied to all pipeline stages. The digital bias generation described in Section V is applied only to the opamps in the 1st and 2nd pipeline stages. Each of the digitally-controlled delay lines shown in Fig. 11 is a cascade of inverters with MOST varactors attached to their outputs [20]. It is possible to achieve better delay accuracy by using the delay-locked loop or the phase-locked loop techniques. However, they were not implemented on this chip. The ADC chip is mounted directly on a circuit board for dynamic performance measurement. The

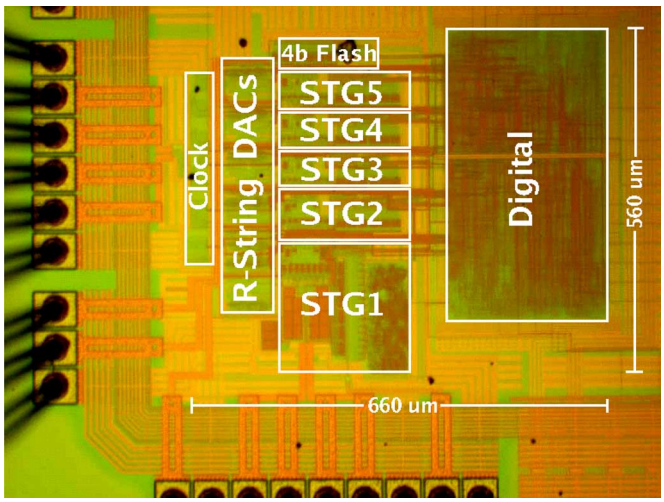

Fig. 17. ADC chip micrograph.

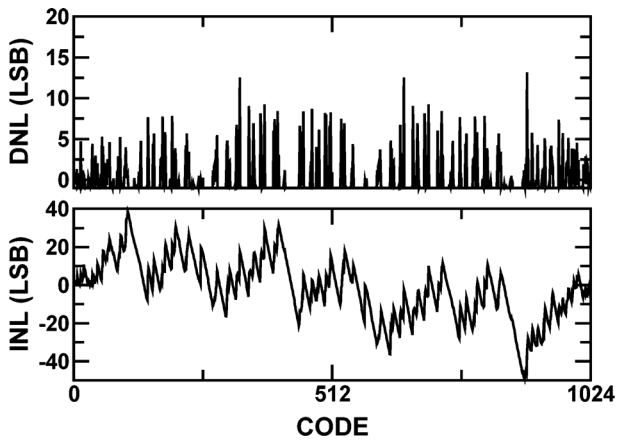

Fig. 18. Measured DNL and INL before digital calibration.

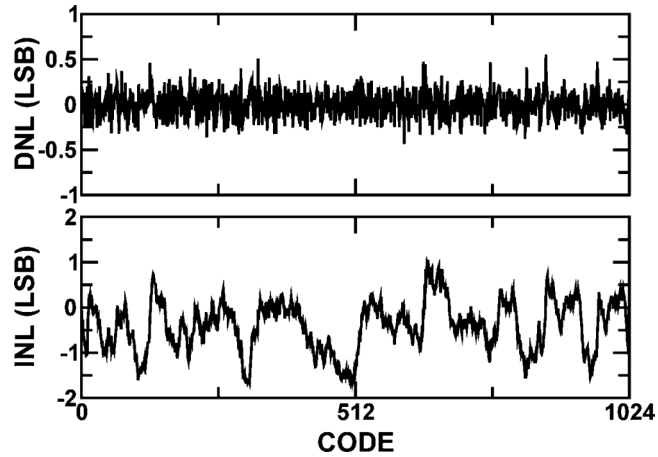

Fig. 19. Measured DNL and INL after digital calibration.

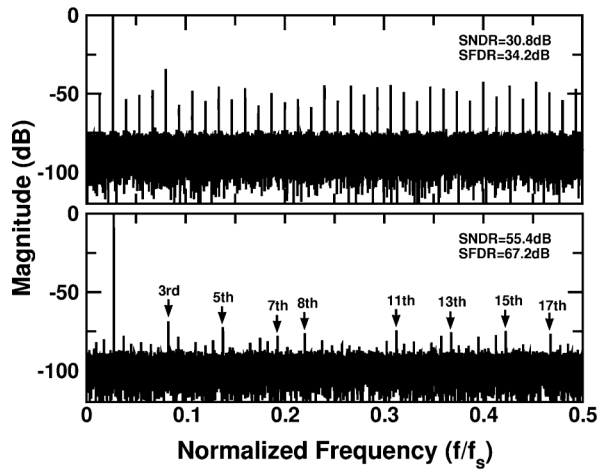

Fig. 20. Measured output spectrum at 300 MS/s before and after calibration. Input is a 1-MHz 1.6-V_{pp} sine wave. Digital output data are collected with a down-sampling ratio of 8.

ADC differential input range is 1.6 V_{pp}. At 300 MS/s sampling rate, the ADC consumes 26.6 mW from a 1.0 V supply.

Figs. 18 and 19 shows the measured differential nonlinearity (DNL) and integral nonlinearity (INL) before and after digital calibration. The sampling rate is 300 MS/s and the input is a 1 MHz sine wave. Before calibration, the ADC exhibits many missing codes, the native DNL is $+13/-1$ LSB and the INL is $+38/-48$ LSB. After calibration, the DNL is improved to $+0.55/-0.44$ LSB and the INL is improved to $+0.99/-1.65$ LSB.

Fig. 20 shows the measured output spectrum at 300 MS/s sampling rate. The input is a 1-MHz 1.6-V_{pp} sine wave. Before calibration, the signal-to-noise-plus-distortion ratio (SNDR) is 30.8 dB and the spurious-free dynamic range (SFDR) is 34.2 dB. After calibration, the SNDR is improved by 24.6 dB to 55.4 dB and SFDR is improved by 33 dB to 67.2 dB. Fig. 21 shows the measured output spectrum at 300 MS/s sampling rate with a 298-MHz 1.6-V_{pp} sine-wave input. The measured SNDR and SFDR are 52.9 dB and 64.5 dB respectively.

Fig. 22 shows the dynamic performance versus input frequency measured at 300 MS/s sampling rate. The measured

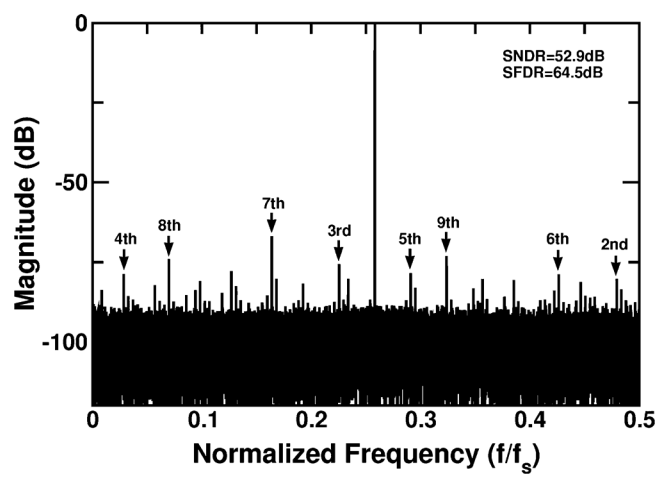

Fig. 21. Measured output spectrum at 300 MS/s sampling rate. Input is a 298-MHz 1.6-V_{pp} sine wave. Digital output data are collected with a down-sampling ratio of 32.

effective resolution bandwidth (ERBW) is about 304 MHz. Fig. 23 shows the dynamic performance versus sampling rate

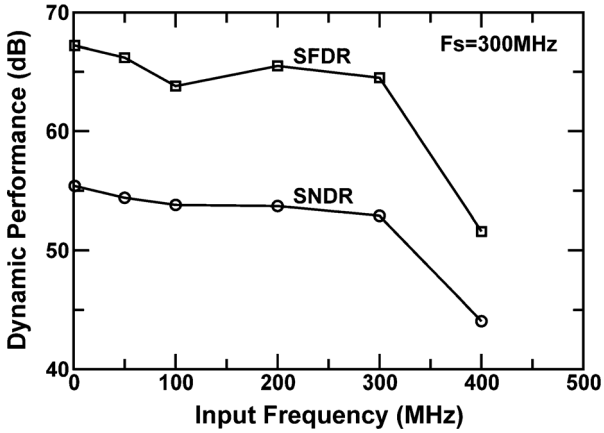

Fig. 22. SNDR and SFDR versus input frequency at 300 MS/s sampling rate.

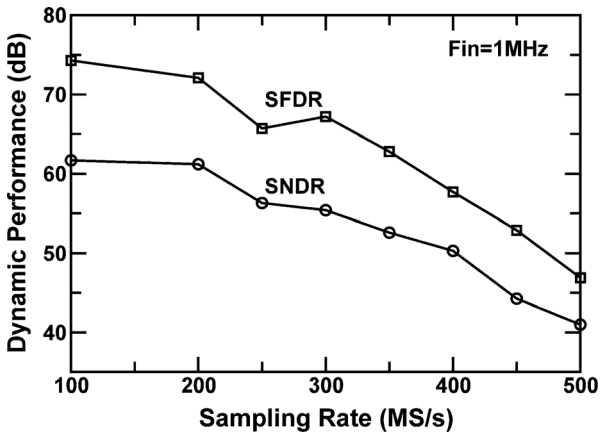

Fig. 23. SNDR and SFDR versus sampling frequency. Input frequency is 1 MHz.

with an 1-MHz sine-wave input. The measured SNDR is above 50 dB up to 400 MS/s sampling rate.

Fig. 24 shows the measured SNDR and SFDR at different temperature. The sampling rate is 300 MS/s. The input frequency is 1 MHz. To demonstrate the effectiveness of the digital bias generation described in Section V, the bias V_{b2} for the opamp is generated with two different configurations. In one configuration, V_{b2} is generated by the digital bias generator shown in Fig. 12. In the other configuration, V_{b2} is generated by using the R-string DAC shown in Fig. 12 with the DAC input set to a fixed default value. Fig. 24 shows that the digital bias generator can adapt against temperature variation.

The performance of this ADC chip is summarized in Table II. The performance of the ADC operated at 200 MS/s sampling rate is also included. At 200 MS/s sampling rate, the ADC exhibits better SNDR and SFDR while consuming less power, yielding better figure-of-merit (FOM). The FOM is defined as

$$\mathrm{FOM} = \frac{\mathrm{Power}}{2^{\mathrm{ENOB}} \cdot \min(2\mathrm{ERBW}, f_s)} \tag{17}$$

where f_s is the sampling rate, and ENOB is the effective number of bits at low input frequency, defined as $\mathrm{ENOB} = [\mathrm{SNDR(dB)} - 1.76]/6.02$. Table III compares this ADC with other 10-bit ADCs that achieve $\geq$200 MS/s sampling rate. Comparing to previous designs using switching opamps [6]–[10], this ADC achieves the fastest sampling rate under a 1.0 V supply.

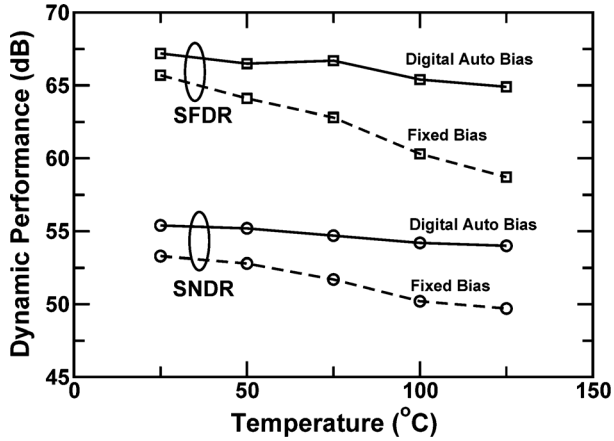

Fig. 24. Measured SNDR and SFDR versus temperature. Sampling rate is 300 MS/s. Input frequency is 1 MHz.

TABLE II
PERFORMANCE SUMMARY

Technology (nm)	65	
Supply Voltage (V)	1.0	
Resolution (Bits)	10	
Sampling Rate (MS/s)	200	300
Differential Input Range V_{pp}	1.6	1.6
DNL (LSB)	+0.43/−0.39	+0.52/−0.40
INL (LSB)	+0.64/−0.65	+0.99/−1.65
SNDR (dB) (f_{in}=1 MHz)	61.2	55.4
SNDR (dB) (f_{in}=202/298 MHz)	60.4	52.9
SFDR (dB) (f_{in}=1 MHz)	72.1	67.2
SFDR (dB) (f_{in}=202/298 MHz)	70.6	64.5
ERBW (MHz)	240	304
Total Power (mW)	19.85	26.6
Analog	11.2	13
Digital	4.7	7.35
Clock	3.5	5.8
R-String	0.45	0.45
FOM (fJ·V/conv.-step)	105.7	184.5
Active Area (mm^2)	0.36	

IX. CONCLUSION

A 10 bit 300 MS/s pipelined ADC using was fabricated using a 65 nm CMOS technology. Simple switching opamps are used to achieve a short turn-on time and save power. Digital calibration is used to cover the deficiency of the opamps as well as capacitor mismatch. Digital calibration can also be used to monitor the settling behavior of the opamps, leading to the design of a digital auto bias generator. Thus, it is possible to set up the bias for the entire opamp without using the external bias generator. This digital bias scheme is adapt to PVT variation while saving power.

ACKNOWLEDGMENT

The authors thank Taiwan Semiconductor Manufacturing Company (TSMC), Hsin-Chu, Taiwan, for chip fabrication under the TSMC University Shuttle Program.

TABLE III
ADC PERFORMANCE COMPARISON

Reference	[22]	[23]	[24]	[25]	[26]	[27]	[28]	[29]	[30]	This Work	
Technology (nm)	90	180	130	130	90	130	90	90	40	65	
Resolution (bits)	10	10	10	10	10	10	10	10	11	10	
Sampling Rate (MS/s)	200	200	205	200	205	210	500	204	300	200	300
Supply (V)	1.2	1.8	1.2/3.3	1.2	1.0	1.2	1.2	1.0	1.8	1.0	1.0
SNDR (dB)	54.4	54.8	56.0	54	55.2	55.0	52.8	55.2	56.6	61.2	55.4
SFDR (dB)	66.5	63.2	73.5	67	64.8	74	N/A	63.5	N/A	72.1	67.2
ERBW (MHz)	200	N/A	200	97	110	100	233	100	100	240	304
Power (mW)	54.6	128	93	83	61	52	55	9.15	40	19.85	26.6
FOM (fJ·V/conv.-step)	641	1430	880	1010	633	560	310	95.4	362	105.7	184.5
Area (mm^2)	1.26	0.79	0.52	1.8	1.0	0.38	0.5	0.22	0.42	0.36	

REFERENCES

[1] P. C. Yu and H.-S. Lee, "A 2.5-V, 12-b, 5-MSample/s pipelined CMOS ADC," *IEEE J. Solid-State Circuits*, vol. 31, no. 12, pp. 1854–1861, Dec. 1996.

[2] K. Nagaraj, H. S. Fetterman, J. Anidjar, S. H. Lewis, and R. G. Renninger, "A 250-mV, 8-b, 52-Msample/s parallel-pipelined A/D converter with reduced number of amplifiers," *IEEE J. Solid-State Circuits*, vol. 32, no. 3, pp. 312–320, Mar. 1997.

[3] B.-M. Min, P. Kim, I. Frederick, W. Bowman, D. M. Boisvert, and A. J. Aude, "A 69-mW 10-bit 80-MSample/s pipelined CMOS ADC," *IEEE J. Solid-State Circuits*, vol. 38, no. 12, pp. 2031–2039, Dec. 2003.

[4] B.-G. Lee, B.-M. Min, G. Manganaro, and J. W. Valvano, "A 14-bit 100-MS/s pipelined ADC with a merged SHA and first MDAC," *IEEE J. Solid-State Circuits*, vol. 43, no. 12, pp. 2613–2619, Dec. 2008.

[5] B.-G. Lee and R. M. Tsang, "A 10-bit 50 MS/s pipelined ADC with capacitor-sharing and variable-gm opamp," *IEEE J. Solid-State Circuits*, vol. 44, no. 3, pp. 883–890, Mar. 2009.

[6] M. Waltari and K. A. I. Halonen, "1-V 9-bit pipelined switched-opamp ADC," *IEEE J. Solid-State Circuits*, vol. 36, no. 1, pp. 129–134, Jan. 2001.

[7] J. Crols and M. Steyaert, "Switched-opamp: An approach to realize full CMOS switched-capacitor circuits at very low power supply voltages," *IEEE J. Solid-State Circuits*, vol. 29, no. 8, pp. 936–942, Aug. 1994.

[8] H.-C. Kim, D.-K. Jeong, and W. Kim, "A partially switched-opamp technique for high-speed low-power pipelined analog-to-digital converters," *IEEE Trans. Circuits Syst. I*, vol. 53, no. 4, pp. 795–801, Apr. 2006.

[9] Y.-J. Kim, H.-C. Choi, G.-C. Ahn, and S.-H. Lee, "A 12 bit 50 MS/s CMOS Nyquist A/D converter with a fully differential class-AB switched op-amp," *IEEE J. Solid-State Circuits*, vol. 45, no. 3, pp. 620–628, Mar. 2010.

[10] P. Y. Wu, V. S.-L. Cheung, and H. C. Luong, "A 1-V 100-MS/s 8-bit CMOS switched-opamp pipelined ADC using loading-free architecture," *IEEE J. Solid-State Circuits*, vol. 42, no. 4, pp. 730–738, Apr. 2007.

[11] D. W. Cline and P. R. Gray, "A power optimized 13-b 5 Msamples/s pipelined analog-to-digital converter in 1.2 μm CMOS," *IEEE J. Solid-State Circuits*, vol. 31, no. 3, pp. 294–303, Mar. 1996.

[12] S.-U. Kwak, B.-S. Song, and K. Bacrania, "A 15-b, 5-Msample/s low-spurious CMOS ADC," *IEEE J. Solid-State Circuits*, vol. 32, no. 12, pp. 1866–1875, Dec. 1997.

[13] B. Murmann and B. E. Boser, "A 12-bit 75-MS/s pipelined ADC using open-loop residue amplification," *IEEE J. Solid-State Circuits*, vol. 38, no. 12, pp. 2040–2050, Dec. 2003.

[14] E. Siragusa and I. Galton, "A digitally enhanced 1.8-V 15-bit 40-MSample/s CMOS pipelined ADC," *IEEE J. Solid-State Circuits*, vol. 39, no. 12, pp. 2126–2138, Dec. 2004.

[15] C. R. Grace, P. J. Hurst, and S. H. Lewis, "A 12-bit 80-MSample/s pipelined ADC with bootstrapped digital calibration," *IEEE J. Solid-State Circuits*, vol. 40, no. 5, pp. 1038–1046, May 2005.

[16] H.-C. Liu, Z.-M. Lee, and J.-T. Wu, "A 15-b 40-MS/s CMOS pipelined analog-to-digital converter with digital background calibration," *IEEE J. Solid-State Circuits*, vol. 40, no. 5, pp. 1047–1056, May 2005.

[17] J.-L. Fan, C.-Y. Wang, and J.-T. Wu, "A robust and fast digital background calibration technique for pipelined ADCs," *IEEE Trans. Circuits Syst. I*, vol. 54, no. 6, pp. 1213–1223, June 2007.

[18] B.-N. Fang and J.-T. Wu, "A 10-bit 200-MS/s digitally-calibrated pipelined ADC using switching opamps," in *Proc. IEEE Int. Symp. Circuits and Systems*, May 2012, pp. 1042–1045.

[19] C.-C. Huang and J.-T. Wu, "A background comparator calibration technique for flash analog-to-digital converters," *IEEE Trans. Circuits Syst. I*, vol. 52, no. 9, pp. 1732–1740, Sept. 2005.

[20] C.-C. Huang, C.-Y. Wang, and J.-T. Wu, "A CMOS 6-bit 16-GS/s time-interleaved ADC using digital background calibration techniques," *IEEE J. Solid-State Circuits*, vol. 46, no. 4, pp. 848–858, Apr. 2011.

[21] J. Mulder, C. M. Ward, C.-H. Lin, D. Kruse, J. R. Westra, M. Lugthart, E. Arslan, R. J. van de Plassche, K. Bult, and F. M. L. van der Goes, "A 21-mW 8-b 125-MSample/s ADC in 0.09-mm^2 0.13-μm CMOS," *IEEE J. Solid-State Circuits*, vol. 39, no. 12, pp. 2116–2125, Dec. 2004.

[22] D. Kurose, T. Ito, T. Ueno, T. Yamaji, and T. Itakura, "55-mW 200-MSPS 10-bit pipeline ADCs for wireless receivers," *IEEE J. Solid-State Circuits*, vol. 41, no. 7, pp. 1589–1595, Jul. 2006.

[23] T. Nezuka, K. Misawa, J. Azami, Y. Majima, and J. Ichi Okamura, "A 10-bit 200 MS/s pipeline A/D converter for high-speed video signal digitizer," in *Proc. IEEE Asian Solid-State Circuits Conf.*, Nov. 2006, pp. 31–34.

[24] B. Hernes, J. Bjornsen, T. N. Andersen, A. Vinje, H. Korsvoll, F. Telsto, A. Briskemyr, C. Holdo, and O. Moldsvor, "A 92.5 mW 205 MS/s 10b pipeline if ADC implemented in 1.2 V/3.3 V 0.13 μm CMOS," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, 2007, pp. 462–463.

[25] Y.-J. Kim, Y.-J. Cho, D.-H. Sa, and S.-H. Lee, "A 10b 200 MS/s 1.8-mm^2 83 mW 0.13-μm CMOS ADC based on highly linear integrated capacitors," *IEICE Trans. Electron.*, vol. e90-c, no. 10, pp. 2037–2043, Oct. 2007.

[26] S.-C. Lee, Y.-D. Jeon, J.-K. Kwon, and J. Kim, "A 10-bit 205-MS/s 1.0-mm^2 90-nm CMOS pipeline ADC for flat panel display applications," *IEEE J. Solid-State Circuits*, vol. 42, no. 12, pp. 2688–2695, Dec. 2007.

[27] Z. Cao and S. Yan, "A 52 mW 10b 210 MS/s two-step ADC for digital-IF receivers in 0.13 μm CMOS," in *Proc. IEEE Custom Integrated Circuits Conf.*, Sep. 2008, pp. 309–312.

[28] A. Verma and B. Razavi, "A 10b 500 MHz 55 mW CMOS ADC," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, 2009, pp. 84–85.

[29] Y.-D. Jeon, Y.-K. Cho, J.-W. Nam, K.-D. Kim, W.-Y. Lee, K.-T. Hong, and J.-K. Kwon, "A 9.15 mW 0.22 mm^2 10b 204 MS/s pipelined SAR ADC in 65 nm CMOS," in *Proc. IEEE Custom Integrated Circuits Conf.*, Sep. 2010.

[30] T. Miki, T. Morie, T. Ozeki, and S. Dosho, "An 11b 300 MS/s 0.24 pJ/Conversion-Step double-sampling pipelined ADC with on-chip full digital calibration for all nonidealities including memory effects," in *IEEE Symp. VLSI Circuits Dig. Tech. Papers*, Jun. 2011, pp. 122–123.

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