Spur-Reduction Frequency Synthesizer Exploiting Randomly Selected PFD

Te-Wen Liao, Jun-Ren Su, and Chung-Chih Hung

***Abstract*— This brief presents a low-spur phase-locked loop (PLL) system for wireless applications. The low-spur frequency synthesizer randomizes the periodic ripples on the control voltage of the voltage-controlled oscillator to reduce the reference spur at the output of the PLL. A novel random clock generator is presented to perform the random selection of the phase frequency detector control for the charge pump in locked state. The proposed frequency synthesizer was fabricated in a TSMC 0.18-μm CMOS process. The proposed PLL achieved phase noise of −93 dBc/Hz with a 600-kHz offset frequency and reference spurs below −72 dBc.**

***Index Terms*— Low spur synthesizer, phase-locked loop (PLL), voltage-controlled oscillator (VCO).**

I. Introduction

Phase noise and spurious-free dynamic range (SFDR) are highly important to the design of a frequency synthesizer. One of the major sources of noise associated with SFDR is switching noise from the charge pump at the reference frequency. The switching noise modulates the control voltage and hence the output frequency of the voltage-controlled oscillator (VCO). Two tones, called reference spurs, appear in the upper and lower sidebands around the carrier and reduce SFDR performance [1]–[4]. The reference spurs are measured according to the difference in power between the carrier and the spurs at a set frequency offset (Δw) given in dBc, as shown in Fig. 1.

The periodic ripples on the control line of the VCO generate reference spurs at the frequency synthesizer output [5], [6]

$$\frac{A_{\text{spur}}}{A_{\text{carrier}}} = \frac{1}{2} \times \frac{K_{\text{VCO}} A_m}{2\pi f_{\text{ref}}}. \tag{1}$$

In [7, Eq. (1)], it should be noted that reducing both K_{VCO} and A_m (A_m is the ripple amplitude), or increasing f_{ref} can decrease the reference spur. However, K_{VCO} is restricted to the tuning range of the specification, and f_{ref} is not a design variable in a conventional Integer-N-based phase-locked loop (PLL). As a result, designers must focus only on reducing the ripples on the control voltage to reduce the reference spur.

A charge-distribution mechanism on the control voltage of the VCO was used to suppress the reference spur [8], as was the technique using distributed phase frequency detectors (PFDs) and CPs [9]. In addition to the use of a spur frequency-boost block [10], techniques involving the doubling of the spur frequency and randomization of the charge redistribution time were also employed to reduce spurs [11]. This brief proposes a novel reference spur-reduction system, involving the randomization and reduction of ripples on the control voltage of the VCO to achieve a low-spur level and relatively smooth spectrum. To this end, we propose a novel random clock generator to perform the random operation. Using the proposed technique, the frequency synthesizer has achieved a phase noise of −93 dBc/Hz at 600-kHz offset frequency and reference spurs below −72 dBc. The architecture of the proposed circuit is presented in Section II. The design of the main building blocks is outlined in Section III. The experimental results for the synthesizer are presented in Section IV, and conclusions are drawn in Section V.

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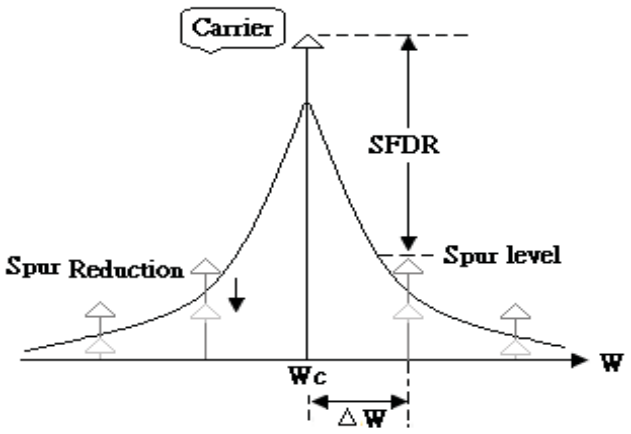

Fig. 1. Frequency domain representation of spurs.

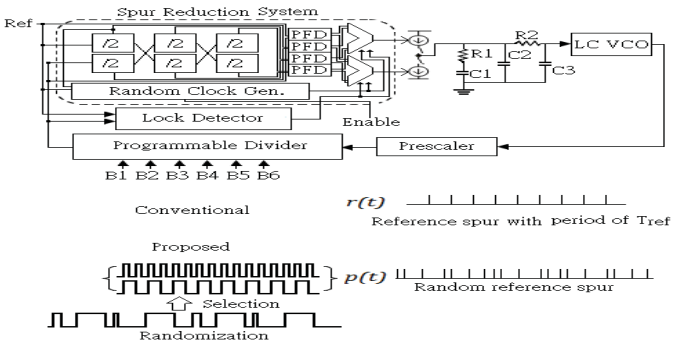

Fig. 2. Architecture of the low-spur frequency synthesizer.

II. Low Spur PLL Architecture

Fig. 2 shows the proposed spur-reduction Integer-N frequency synthesizer. The accuracy of the synthesizer is maintained by locking to a reference frequency to set the output frequency. This locking action is accomplished using feedback by dividing the LC VCO output frequency and comparing its phase with the phase of the reference source to produce an error signal. The phase comparison operation is performed using PFDS, which also acts as a frequency discriminator when the PLL is out of lock. The low pass filter (LPF) attenuates high-frequency components of the charge pump output to ensure that a smooth signal is sent to the LC VCO input. The LPF is typically fed by a charge pump, which converts the error signal to a current waveform. A key characteristic of the Integer-N synthesizer is the ability to use a random clock generator to randomize the output of two MUXs, and hence the speed of the charge or discharge operation of the charge pump enabling the control voltage line to randomly skip or reduce ripples. Thus, reducing the ripples generated by charge pump switches should produce relatively smooth voltage at the loop filter output, resulting in a reduction in spur tones in the frequency domain. This concept led to the idea of randomly sampling the charge

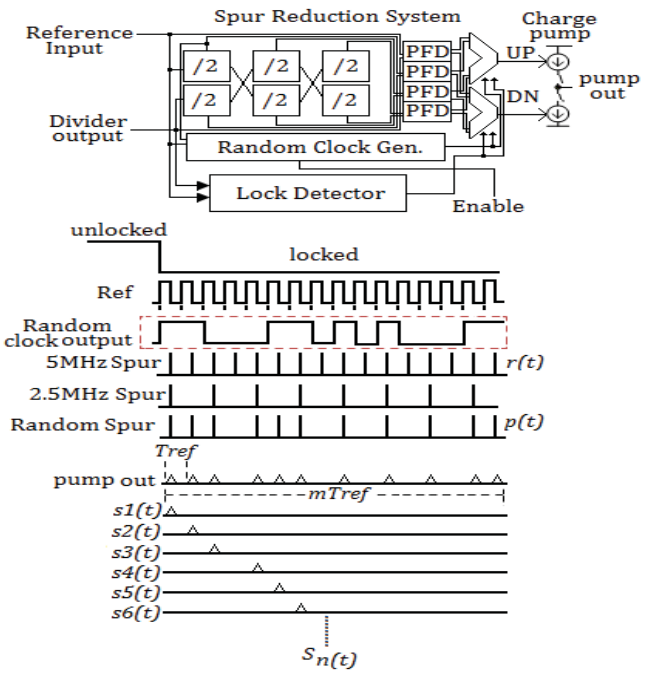

Fig. 3. Spur-reduction system.

pump output of frequency synthesizers. The proposed approach is easily applicable to a wide range of similar advanced processes.

III. Main Building Blocks

A. Spur-Reduction System

For conventional synthesizers in lock mode, the PFD generates fast spikes that modulate the VCO control line and generate spurious signals at the reference frequency offset, the harmonics of which reduce SFDR performance in communication systems. The spur at the reference frequency is difficult to filter out. Higher harmonics are generally filtered out using a loop filter. As shown in Fig. 3, this brief employed a lock detector and a novel random clock generator to randomize and average the charge pump output ripple. This system provides four random frequencies of charge pump operation implemented using four PFDs, six divided-by-two dividers, and two MUXs. Three of the six divided-by-two dividers divide the reference input to produce Ref/2, Ref/4, and Ref/8. Similar signals are also generated for the output of the feedback divider by the other three divided-by-two dividers. The four PFDs compare the reference input and the feedback divider output, their divided-by-two signals, divided-by-four signals, and divided-by-eight signals, respectively. The random clock generator provides a random signal enabling the deployment of the four frequencies used for charge pump operation within the synthesizer, which we refer to as a randomized charge pump. Two MUXs afford 00, 01, 10, and 11, enabling the randomizing of U_P and D_N signals to the charge pump. In the unlocked status, we selected Ref/4 or Ref/8 for tracing. In the locked state, we selected the Ref or Ref/2 frequency for the charge pump, as shown in Fig. 3. Thus, the random clock can reduce and separate spurs throughout the frequency domain to produce a high performance PLL for communications systems.

With a reference clock (Ref) period of T_{ref}, the traditional control voltage of the VCO can be simplified as [8], [12]

$$r(t) = a_0 + \sum_{k=1}^{\infty} a_k \cos\left(\frac{k \times 2\pi}{T_{\text{ref}}}\right) t. \tag{2}$$

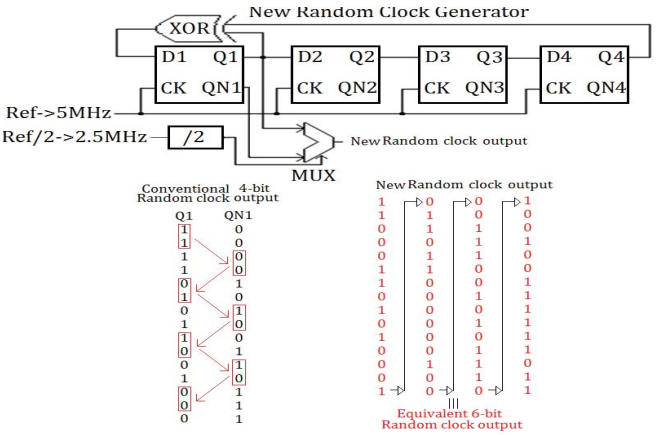

Fig. 4. Proposed random clock generator.

For the spur at the reference frequency, the corresponding term is

$$a_1 = \frac{1}{T_{\text{ref}}} \int_0^{T_{\text{ref}}} r(t) \cos\left(\frac{2\pi}{T_{\text{ref}}} t\right) dt. \tag{3}$$

Assume that $p(t)$ is the random-disturbance waveform with a period of mT_{ref}, where m is determined by the random bit length s, $m = 2^s$. $p(t)$ can be expressed as

$$p(t) = b_0 + \sum_{k=1}^{\infty} b_k \cos\left(\frac{k \times 2\pi}{mT_{\text{ref}}}\right) t. \tag{4}$$

For the random spur at the reference frequency, the corresponding term is

$$b_1 = \frac{1}{mT_{\text{ref}}} \int_0^{mT_{\text{ref}}} p(t) \cos\left(\frac{2\pi}{T_{\text{ref}}} t\right) dt. \tag{5}$$

$P(t)$ can be expanded into n periodic pulses $S_1(t)$, $S_2(t)$,... and $S_n(t)$ with the period of mT_{ref}. Each periodic pulse is the same, aside from differences in phase shift. Thus, we can rewrite (5) as

$$b_n = \sum_{k=1}^{n} c_{n,k} = \sum_{k=1}^{n} \frac{1}{mT_{\text{ref}}} \int_0^{mT_{\text{ref}}} s_k(t) \cos\left(\frac{2\pi}{T_{\text{ref}}} t\right) dt. \tag{6}$$

According to (6), the spur at the reference frequency is reduced by a factor of two to the power of the random clock bit length. Therefore, the spur power spectrum density can be averaged to reduce the spur and obtain a smooth spectrum in the frequency domain.

B. Random Clock Generator

In Fig. 4, we present a novel random clock generator. The spur at the reference frequency is reduced by a factor of two to the power of the random clock bit length, which is directly related to hardware cost, power consumption, and chip area. A conventional random clock is likely to obtain more "1s" than "0s," as illustrated in Fig. 4, which degrades the effectiveness of reducing the spur level. The proposed random clock generator enables equal chances to obtain "0s" and "1s," which averages the periodic spur tones in the frequency domain. The new random clock generator comprises a conventional 4-bit random clock generator, one MUX, and one divided-by-two circuit. The output of the conventional 4-bit random clock generator is a Pseudo Random Binary Sequence (PRBS). Fig. 4 illustrates that Q1 is more likely to be "1" than "0," however, QN1 is more likely to be "0" than "1." Therefore, the MUX selection is meant to equalize the likelihood of obtaining "1" and "0." With the

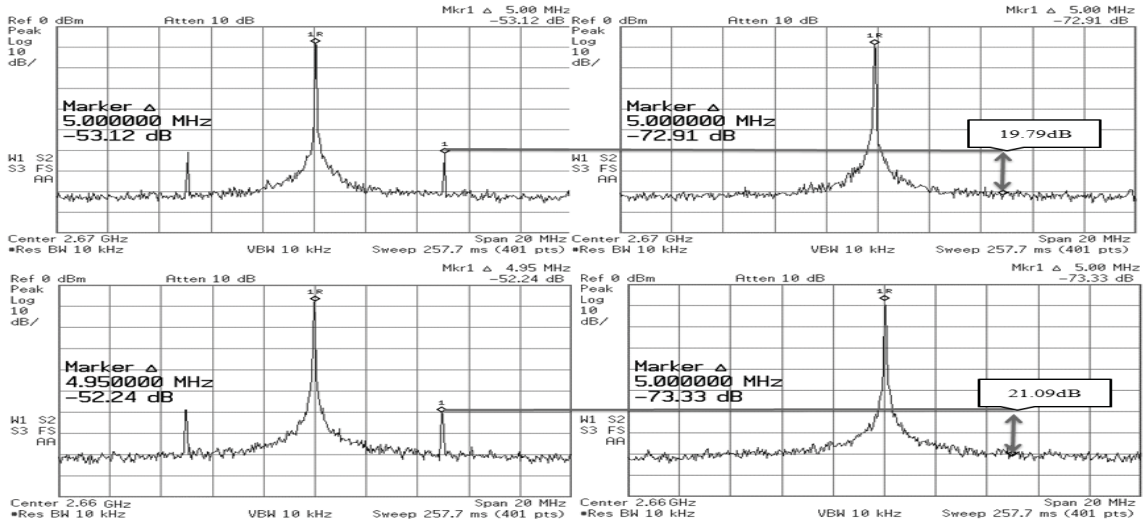

Fig. 5. Measured spur-reduction.

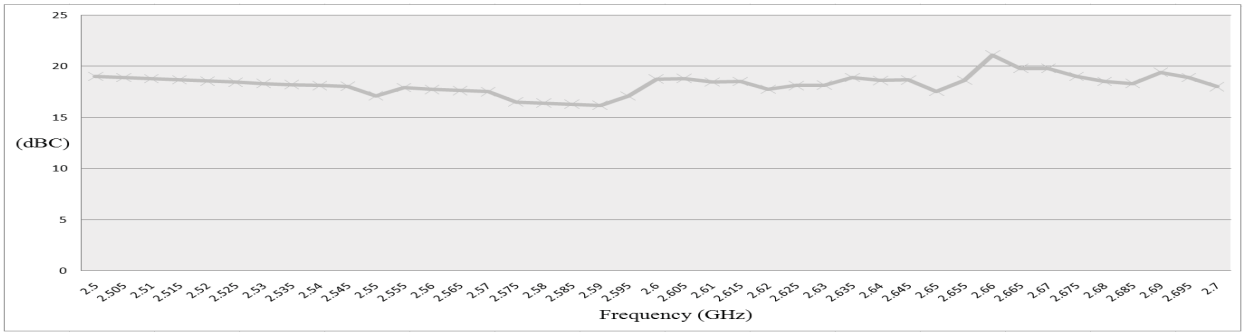

Fig. 6. Measured spur suppression from 2.5 to 2.7 GHz.

input of a 5 MHz reference clock (Ref), the outputs (Q1, QN1) of the conventional 4-bit random clock generator are connected to the inputs of the MUX, controlled by Ref/4. Therefore, the output of the new random clock generator will take two consecutive outputs of Q1 (11), two consecutive outputs of QN1 (00), and the next two Q1 outputs (01), and so on. In this manner, generating outputs by alternating between two Q1s and two Q1Ns, the Q1 and Q1N sequences are circulated four times starting from the generation of the initial (11). In this manner, the additional MUX enables an increase (by two) in the effective bits of the random clock generator to produce a 6-bit PRBS. The proposed circuit occupies less area and consumes less power than conventional 6-bit random clock generators. In the locked state, the periods of 4- and 6-bit random clock generators are

$$\frac{5\ \text{MHz}}{2^4-1} = 333\ \text{KHz} \quad \text{and} \quad \frac{5\ \text{MHz}}{2^6-1} = 79\ \text{KHz}. \tag{7}$$

A third LPF is sufficient to attenuate the spur level using the proposed 6-bit random clock generator for PLL in a wireless system.

C. Multi-Modulus Divider (MMD)

The divider architecture is essential to low power dissipation and high design flexibility. All of the cells in MMDs are identical, which is highly beneficial in layout work. The programmable divider provides an output signal with a period of

$$T_{\text{out}} = (2^6 + B6\cdot 2^5 + B5\cdot 2^4 + B4\cdot 2^3 + B3\cdot 2^2 + B2\cdot 2^1 + B1)\times T_{\text{in}}.$$

This equation shows that division ratios from 64 (if all CON = 0) to 127 (if all CON = 1) are achieved [13].

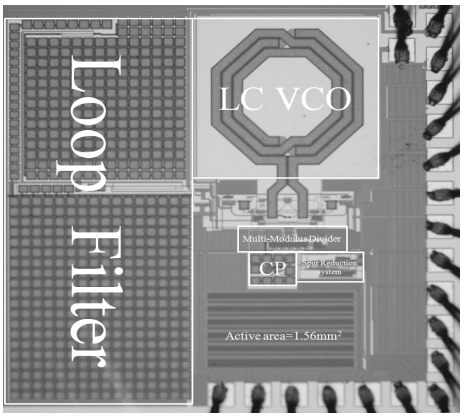

Fig. 7. Die micrograph.

IV. Experimental Results

The circuit was fabricated using the TSMC 0.18-μm 1P6M CMOS process. The low-spur frequency synthesizer has an output frequency range of 2.5 to 2.7 GHz. The reference frequency is 5 MHz. The tunable range of the LC VCO is from 2.2 to 2.8 GHz, and the gain is 336 MHz/V. Without a spur suppression mechanism, experimental results show a measured reference spur of −53 dBc at a locked frequency of 2.67 GHz and −52 dBc at a locked frequency of 2.66 GHz with a 5-MHz frequency offset. With the spur suppression circuit enabled, the measured reference spurs are −72 and −73 dBc,

TABLE I
PERFORMANCE SUMMARY

Technology	TSMC 0.18-μm 1P6M CMOS
Power supply	1.8 V
Reference fre.	5 MHz
LC VCO	2.2–2.8 GHz
Divider ratio	500
Kvco	336 MHz/V
Spur level	−72 dBc
Phase noise at 600 kHz	−93 dBc/Hz
Phase noise at 1 MHz	−105 dBc/Hz
Phase noise at 3 MHz	−111 dBc/Hz
Power consumption	20 mW

TABLE II
COMPARISON WITH PRIOR WORKS

	[4]	[6]	[14]	[15]	This brief
Process	**0.18-μm CMOS**	**0.18-μm CMOS**	**0.18-μm CMOS**	**0.25-μm CMOS**	**0.18-μm CMOS**
Supply	**1.8**	**1.8**	**1.8 v**	**2.5 v**	**1.8**
Power (mW)	**22**	**18**	**7.6**	**117.5**	**20**
Freq. (GHz)	**2.2**	**4.8/2.4**	**2.21**	**4.12–4.72**	**2.5–2.7**
Ref. freq. (MHz)	**20**	**1**	**55.25**	**4**	**5**
Loop band-width	**270 kHz**	**N/A**	**N/A**	**90 kHz**	**50 kHz**
Loop filter	**N/A**	**2nd**	**N/A**	**N/A**	**3rd**
Ref. spur (dBc)	**−52**	**−55**	**−46**	**−45**	**−72**

respectively, as shown in Fig. 5. Phase noise of −93 dBc/Hz with a 600-kHz offset and −111 dBc/Hz with a 3-MHz offset were obtained. The circuitry added to reduce the reference spur results in a small increase in phase noise. With the spur-reduction system off, the phase noise is −108 dBc/Hz at 1-MHz offset; with the spur-reduction system on, the phase noise becomes −105 dBc/Hz at 1-MHz offset, representing an increase of 3 dBc/Hz. Without the proposed technique, the total integrated phase noise from 100 Hz to 1 MHz is 20.31 mrad, with the proposed technique, the total integrated phase noise is 32.29 mrad. According to Fig. 5, the proposed spur-reduction system is capable of reducing the reference spur by approximately 20 dB. The proposed spur-reduction system reduces the reference spur with only a small increase in phase noise. Fig. 6 illustrates the degree to which the reference spur was decreased across the entire tuning range. The proposed suppression technique was implemented with 5-MHz channel spacing for wireless applications. Within a frequency range of 2.5 to 2.7 GHz, the spur suppression level is between 17 and 21 dBc. The Die micrograph is shown in Fig. 7. The area of the synthesizer is 1.56 mm^2, include the LPF.

A summary of the performance of the proposed circuit is provided in Table I and a comparison with prior works is provided in Table II. The proposed method has a lower reference spur level than other 0.18-μm CMOS frequency synthesizers for wireless applications.

V. CONCLUSION

This brief proposed a low-spur frequency synthesizer for randomizing the ripples on the VCO control voltage to reduce the reference spur at the output of the locked PLL. A novel random clock generator was also presented to perform the averaging operation. The circuit was fabricated using the TSMC 0.18-μm CMOS process, demonstrating phase noise of −93 dBc/Hz with a 600-kHz offset frequency and reference spurs below −72 dBc.

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