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SILICIDE-CAUSED ANOMALOUS REVERSE CURRENT–VOLTAGE CHARACTERISTICS OF $CoSi_2$ SHALLOW p^+n JUNCTIONS

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Abstract—Silicided shallow p^+n junctions formed by BF_2^+ implantation into thin Co films on Si substrates to a low dosage (5×10^{14} cm^{-2}) and subsequent rapid thermal annealing (RTA) or conventional furnace annealing (CFA) are used to show the impact of silicides on junction characteristics. CFA results in a lower leakage than RTA at a low bias as 5 V at high temperatures attributable to longer annealing time. All the diodes made by RTA exhibit a hard-breakdown behavior. For CFA 700°C annealing, however, an anomalously poor reverse I–V behavior indicative of athermal emission is found at high bias. In addition, the 800°C-formed diodes and the CFA-treated 1×10^{16} cm^{-2} implanted samples show good reverse characteristics even at high bias. As a result, annealing conditions should be properly chosen to reduce the impact of silicides on shallow junctions.

1. INTRODUCTION

Due to the scale-down of the devices in ultra-large-scale-integration (ULSI) circuits, a concomitant reduction in source/drain (S/D) junction depth is required to minimize short channel effects[1]. Metallized S/D contacts improve performances for the submicrometer MOSFET because of the reduction in the parasitic S/D resistance and in the contact resistance. Forming silicides in S/D regions is the most attractive approach due to its self-aligned features[2–4]. However, devices with shallow junctions ($\leqslant 0.2\ \mu$m) are difficult to metallize due to junction leakage associated with the S/D silicidation process, although junctions with depth $\sim 0.25\ \mu$m have been successfully metallized with silicides[5,6]. An available approach to form silicided shallow junctions is to implant dopant into silicided and then outdiffuse the dopant within silicides to form junction regions[7–11].

In this study, silicide-caused anomalous reverse I–V characteristics of $CoSi_2$ shallow p^+n junctions are discussed. The silicided shallow junctions were formed by implanting BF_2^+ ions into thin Co films on Si substrates to a low dose and subsequent drive-in/silicidation using conventional furnace annealing (CFA) or rapid thermal annealing (RTA). A low-dose implant, and thus a low-doped junction, was used to helpfully exhibit the impact of silicides on the junction behavior.

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2. EXPERIMENTAL DETAILS

(100) oriented, 0.55–1.1 Ω-cm, phosphorus-doped Si wafers were used. A 4500 Å-thick SiO_2 layer was thermally grown for patterning the active regions of diodes as well as for the utilization of selective-etching. After the patterning, a thin Co film of 300 Å-thickness were deposited at room temperature in an electron-beam evaporation system with a base pressure better than 4×10^{-6} torr. An a-Si capping layer of 50 Å-thickness was followly deposited to prevent Co from oxidation during annealing. The as-deposited samples were then BF_2^+ implanted at 70 keV to a dose of 5×10^{14} cm^{-2}. A two-step annealing process was used to carry out the salicide process. The Co film selectively reacted with the exposed Si at 450°C for 30 min in a N_2 ambient to form CoSi and then the unreacted Co on SiO_2 was chemically removed by utilizing the etchants consisting of a 5:3:1:1 volume mixture of acetic, nitric, phosphoric and sulphuric acids, used at 40°C[2]. The resintering was performed either by CFA for 30 min or by RTA for 60 s at temperatures ranging from 500 to 800°C.

For the 70 keV implant, the boron only partly penetrates into the Si substrate. Subsequent annealing eventually makes the transition of Co into $CoSi_2$ and thus consumes ~ 1000 Å Si. Hence, the junction formation is primarily due to the dopant released from Co or CoSi films during silicidation and/or the residual penetrating dopant below silicides. As a result, the process closely resembles siliciding an existing junction.

3. RESULTS AND DISCUSSION

The value of J_r was defined to be the leakage current density measured at -5 V and at room temperature. At least 10 diodes for each sample were taken to evaluate the value. Figure 1 shows the dependencies of J_r on annealing temperature for the specimens treated by RTA and CFA processes, respectively. Figure 2 shows the forward ideality factor, n, corresponding to Fig. 1. For the CFA process, the J_r value decreased rapidly when the annealing temperature was raised, attributable to the improved defect recovery and the increased dopant activation. The junctions formed by RTA were also improved with increasing RTA temperature, except that slight degradation was found at 800°C. The degradation was conjectured to be that the implanted dopant could be largely confined by the formed silicides during high-temperature RTA processing[12] due primarily to metal-dopant compound formation[9].

Generally at the same annealing temperature, the longer CFA should be expected to annihilate more damage than RTA. But, RTA was reported to be better than CFA in defect recovery because of its high heating rate[13]. As a result, as shown in Fig. 1, RTA caused smaller leakage than CFA at temperatures <600°C. However, high annealing temperature greatly enhanced the annealing time effects on junction formation. Hence, CFA would drive-in more dopants and yield better but deeper junctions than RTA at high temperatures. As a result, CFA optimized an excellent junction with a J_r of 0.1 nA/cm^2, an n of 1.00, and a depth of about 0.12 μm at 800°C. The junction depth is evaluated starting from the silicide/Si interface, using a spreading-resistance probe apparatus. Meanwhile, the optimum junction yielded by RTA showed diode characteristics of about 1.5 nA/cm^2, 1.00 and 0.07 μm, correspondingly, for 700°C annealing.

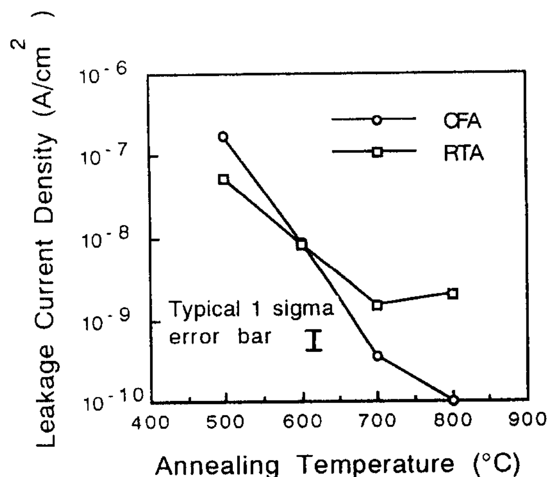

Fig. 1. Dependencies of leakage current on annealing temperature for the samples annealed by CFA and RTA processes, respectively.

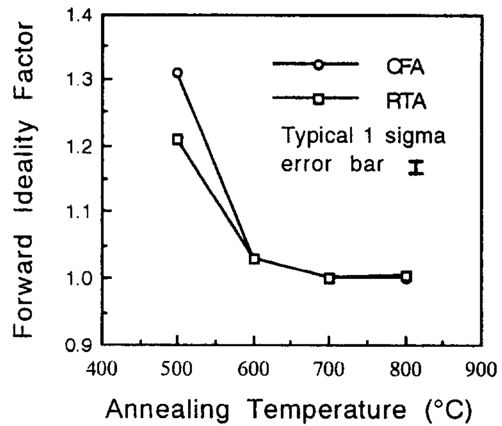

Fig. 2. Forward ideality factor corresponding to Fig. 1.

For the present samples, CFA could yield better junctions than RTA at temperatures >600°C. However, the reverse I–V characteristics at high bias voltages were quite distinct for RTA and CFA. Figure 3 shows the variations of reverse current density with reverse bias for the samples CFA-processed at 500, 700 and 800°C, respectively. A hard-breakdown behavior with a breakdown voltage of about 32 V was present for 500°C annealing. The RTA-treated samples also displayed a similar behavior for the 500°C anneal. However, a very soft-breakdown I–V curve was observed for the samples CFA-treated at 700°C. When the bias voltage was <7 V, the leakage was very small (<1 nA/cm^2). As the bias was raised to be above 7 V, the reverse currents increased very rapidly with increasing bias. At a high reverse bias as 10 V, the Arrhenius plot of (J_r/T^3) vs $1/T$ (with T being $25 \sim 200$°C) showed a diffusion-dominant leakage at the region of high measuring temperatures and an almost temperature-independent profile showing a large leakage current at the region of low measuring

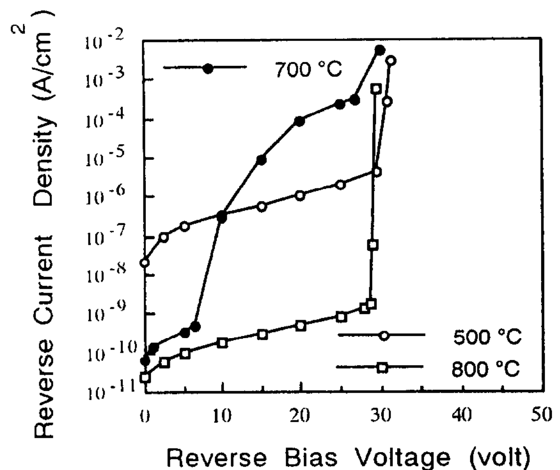

Fig. 3. Variations of reverse current density with bias voltage for the samples CFA-treated at 500, 700 and 800°C, respectively.

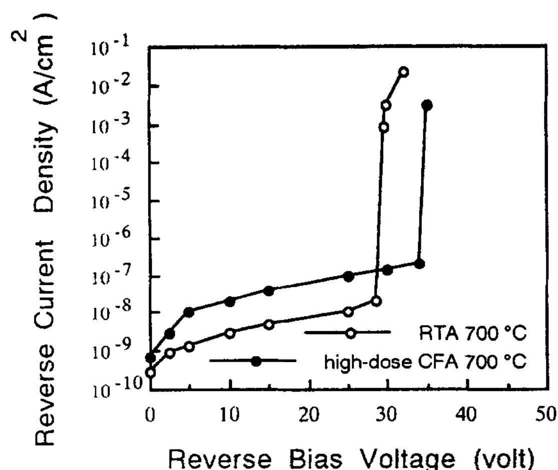

Fig. 4. Variations of reverse current density with bias voltage for the low-dose samples RTA-treated at 700°C and the high-dose samples CFA-treated at 700°C, respectively.

temperatures. However, at a low reverse bias as 5 V, the Arrhenius plot showed a junction leakage dominated by generation current at the region of low measuring temperatures.

Previously, an athermal emission was reported to be associated with the asperity of silicides on the diffused regions and thus an enhanced electric field[14]. The present athermal emission at high reverse bias may also be attributable to a similar leakage mechanism. Moreover, the junctions formed by CFA at 800°C exhibited again a hard-breakdown behavior with a breakdown voltage of about 29 V. However, the breakdown voltage for 800°C annealing was slightly lower than that for the 500°C anneal attributed to a larger interfacial roughness of silicide/Si. The above results indicated that the high-bias reverse characteristics were strongly affected by the CFA temperature. By properly choosing the CFA temperature, then the prepared silicided shallow junctions could preserve good junction characteristics.

On the other hand, all the RTA-treated samples manifested a hard-breakdown behavior. Figure 4 shows the variations of reverse current density with bias voltage for the low-dose samples RTA-treated at 700°C and the high-dose samples ($1 \times 10^{16}\,cm^{-2}$ implant) CFA-treated at 700°C, respectively. High-dose implant, thus high-doped junction regions, greatly improved the reverse characteristics by screening the strong electric field from the silicide/Si interface. As a result, considering the formation of silicided junctions in ULSI circuits, the yield of devices needed a great attention due to a probable lowering of breakdown voltage of S/D junctions.

4. CONCLUSIONS

Silicided shallow p^+n junctions are formed by implanting BF_2^+ ions into thin Co films on Si substrates to a low dose ($5 \times 10^{14}\,cm^{-2}$) and subsequent annealing, by which to show the impact of silicides on junction characteristics. Both CFA and RTA yield low-leakage diodes at a low bias as 5 V. RTA results in good junctions showing a hard-breakdown behavior for all diodes. For CFA 700°C annealing, however, anomalously poor reverse I–V characteristics are found at high reverse bias. The severe soft-breakdown behavior was indicative of an athermal emission that may be attributable to an enhanced electric field near the silicide/Si interface. However, the CFA 800°C-formed diodes again exhibit a hard-breakdown behavior. In addition, the junctions formed by $1 \times 10^{16}\,cm^{-2}$ implant show good reverse characteristics for all CFA temperatures. As a result, the annealing conditions should be properly utilized to reduce the impact of silicides on junction characteristics.

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