A Power Cloud System (PCS) for High Efficiency and Enhanced Transient Response in SoC

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***Abstract*—Tradeoff between power efficiency and transient performance usually comes out during the design consideration of a power module. A configurable power supplying implementation named as the power cloud system (PCS) is proposed to handle different load conditions for simultaneously improving the power efficiency and the transient response in order to meet the system-on-chip (SoC) requirements. At heavy loads, the switching regulator takes over the energy delivery scheme in the PCS with the fast transient technique. An auxiliary power unit, which activates hybrid operation in both medium and light loads, can realize the low-dropout (LDO) regulator to provide a supplementary energy immediately in transient duration and be the high-side power switches of the switching regulator to minimize the power loss. Besides, owing to its low quiescent current of an LDO regulator, it can directly operate under the ultralight-load condition. Therefore, the satisfactory power conversion efficiency and the load transient response can be derived over a wide load range, which will certainly meet the power requirement for different operated functions in the SoC. The chip was fabricated by a 0.25-μm CMOS process, and the experimental results show the improvements of 56% transient dip voltage and 25% transient recovery time in hybrid operation, as well as a peak efficiency of 94%.**

***Index Terms*—Auxiliary power unit (APU), hybrid operation, power cloud system (PCS), power conversion efficiency, power module, system-on-chip (SoC), transient response.**

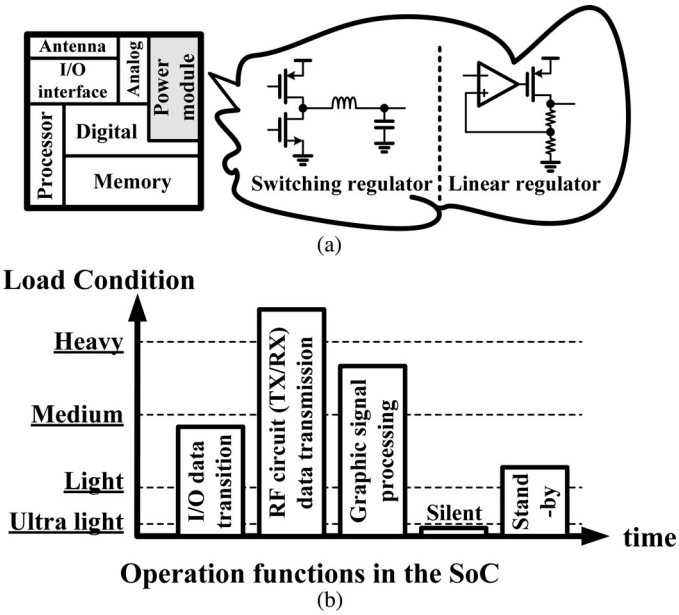

Fig. 1. (a) Embedded power module in SoC. (b) Illustration of the energy demands provided by a power module for different system operation functions in SoC.

I. Introduction

HIGH-PERFORMANCE power management has been an essential part in today's system-on-chip (SoC) integration. The complex system operation needs the adequate power supply function to further enhance its performance. Thus, the correct operation function and the lengthened battery life can be achieved, especially in the portable electron device applications. In the common power distribution scheme of the SoC system, a power controller can indicate the demand of core voltage or other energy requirements according to the different system operation scheme [1]–[3]. Dynamic voltage scaling (DVS) [4]–[6] is also a popular energy modulation scheme provided by a power module, which manages the power distribution according to the indication of the SoC system. Fig. 1 shows the illustration of the energy demand in SoC with the distinct operation functions and the required energy consumptions. The embedded power module in SoC, which is generally implemented through the switching regulators [7]–[12] or the low-dropout (LDO) regulators [13]–[15], can provide a regulated supply voltage. However, the load current condition of the power module in the SoC would be varied rapidly. The high power conversion efficiency and the satisfactory load transient performance along with the wide load range are considered as the critical design issues. The inductor-based switching regulator has the capability to drive the large load current with good power conversion efficiency, but derives the efficiency deterioration at light loads and the slow load transient responses. The LDO regulator can provide the rapid transient response; nevertheless, it is hard to extend its load current range and will carry out the poor power conversion efficiency. In addition, the voltage recovery reaction is obtained after the occurrence of load current variation in conventional power module implementation. Hence, the resultant slow

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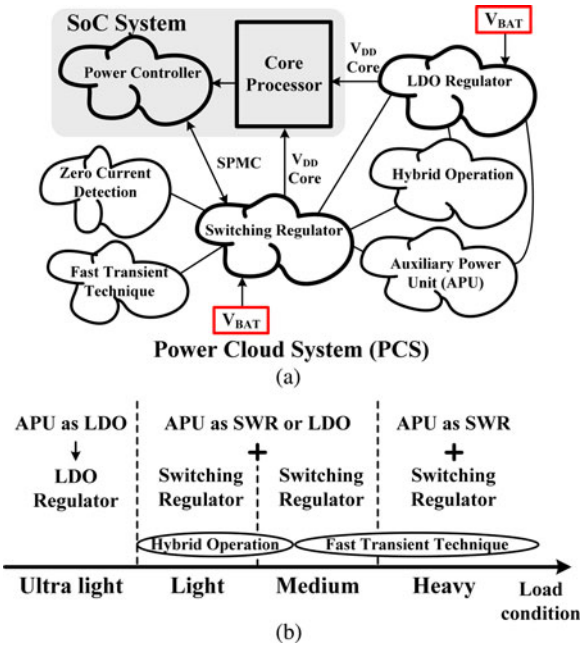

Fig. 2. Idea illustration of the PCS. (a) Relationships between the different supply mechanisms for achieving a proper power module for the SoC system. (b) PCS operation under different load conditions.

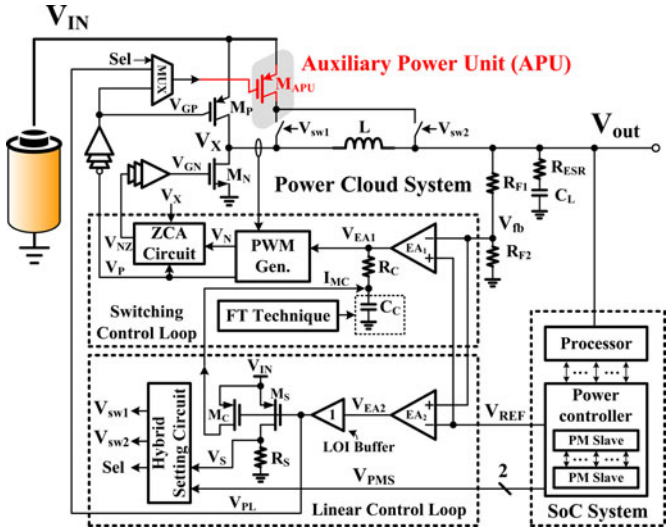

Fig. 3. Architecture of the proposed PCS.

transient response and the large voltage dip will be derived, which might cause the incorrect function in the SoC and needs to be minimized.

As the trend of advanced power consideration, the system processor can determine the energy demand and send the energy requests to the power module by a master power controller. Thus, the proposed power module for SoC applications is implemented as the power cloud system (PCS) as shown in Fig. 2, which can vary the structure of the power module according to the different power demand as well as the load current conditions in the SoC system. Fig. 2(a) indicates the relationship between the different supply mechanisms in the PCS, which are directed by the master power controller in the SoC. The core processor in the SoC is mainly supplied by the switching regulator or the LDO regulator with a regulated $V_{\rm DD}$ core voltage to guarantee its correct function. However, to obtain high power conversion efficiency and good load transient response in the power module, the supply mechanism should be effectively organized according to variable load conditions. There are some existing functional power clouds, which can be reorganized as the tradeoff between power conversion efficiency and transient response over a wide load range. Specially, the implementation of auxiliary power unit (APU) can help strengthen the driving capability of the switching regulator, as well as enhance load transient response through the realization of the LDO regulator [16].

The illustration of PCS operation with the different load conditions is shown in Fig. 2(b). When the SoC requires larger energy, the PSC will provide higher driving current through the pure switching regulator operation to guarantee the power conversion efficiency. In addition, the APU is activated to behave as a switching regulator at this instant condition. The fast transient technique, which regards the unobvious power consumption compared to the high current supply at the output, is also utilized to speed up the load transient response and derive the small transient dip voltage. On the other hand, the hybrid operation is activated at both medium and light loads. That is, the APU acts as the switching regulator in steady state, whereas it can be realized as the LDO regulator during the load transient period since the LDO regulator equips the larger loop bandwidth compared to that of the general switching regulator design. That is, the utilization of fast transient technique may be inappropriate due to it apparent current consumption. As a result, the issues of power conversion efficiency and load transient response can be taken into consideration simultaneously. As the load decreases, the LDO regulator, which is achieved by the APU only, takes over the complete supply function in the PCS at ultralight loads to retain the regulated output voltage. The small power consumption in the LDO can maintain the efficiency since the power loss consumed by a switching regulator grows into a relatively high portion at ultralight loads. That is to say, the PCS can determine which of the small power clouds need to be included at one specific load condition through the demand from the SoC, so as to guarantees the power conversion efficiency and the operation of load transient response over a wide load range.

This paper is organized as follows. The proposed PCS operation is illustrated in Section II. System stability analysis is described in Section III. Circuit implementations and experimental results are shown in Sections IV and V, respectively. Finally, a conclusion is made in Section VI.

II. Operation of the PCS

Fig. 3 shows the architecture of the proposed PCS. To properly regulate the output voltage $V_{\rm out}$ for supplying the SoC, the control loops recognized as the switching control loop and the linear control loop can realize the distinct energy supply topologies according to different system requirements. The switching regulator contains the high-side power switch M_P and the

low-side power switch M_N to deliver energy from the battery input $V_{\rm IN}$ to $V_{\rm out}$ with the utilization of off-chip inductor. Besides, the APU can serve as the high-side power switch $M_{\rm APU}$, which is operated in parallel with M_P to enhance the driving capability of a switching regulator at heavy loads, or regard as the pass device in the linear regulator to strengthen the load transient response and to assure the energy driving function at ultralight loads. That is, the PCS achieves the proper power module realization in the SoC, which is derived under the demand. As a result, the energy on-the-fly function is deservedly carried out that depicts the advantages of power module integration in the SoC.

A. High Power Demand in SoC (Heavy-Load Condition)

When the SoC activates the operation such as the high-speed data transmission or the complex signal processing as shown in Fig. 1, the power module will receive the request of high power demand. Thus, the PCS will form the switching regulator owing to its high driving capability. As shown in Fig. 4(a), a current-mode buck operation is achieved through the switching control loop at heavy loads. By referring the detailed control circuits illustrated in Fig. 3, the error amplifier $\rm EA_1$, which is implemented with the high gain structure by using the cascode output stage, can maintain the high loop gain for good output voltage regulation and can generate the error signal $V_{\rm EA1}$ for deciding duty cycle. The current sensing mechanism helps achieve the current-mode control while the system stability can be guarantee by the proportional integral (PI) compensation, which is achieved by compensation resistance R_C and compensation capacitance C_C. The fast transient technique is also implemented to dynamically adjust the system compensation scheme [17] in order to accelerate the load transient response in the current-mode buck converter operation. The PWM generator and driver produce the control signals of $V_{\rm GP}$ and $V_{\rm GN}$ to drive the M_P and the M_N, respectively. The zero current adjusting (ZCA) circuit can eliminate the negative inductor current by compensating the effect of nonideal offset and the propagation delay. In addition, the MOSFET $M_{\rm APU}$ of APU, which is set in parallel with M_P in Fig. 4(a), works as a part of high-side power switch under the heavy-load condition It can enhance the driving capability through the enlarged power switch size to minimize the conduction loss in power stage.

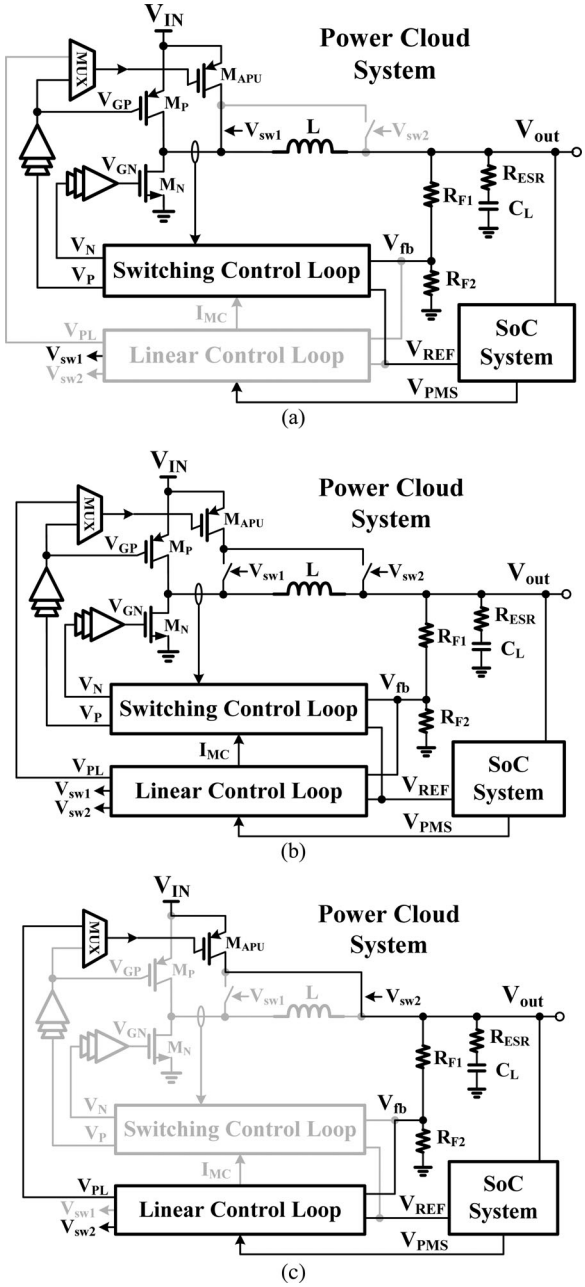

Fig. 4. Proposed PCS operation under the different load conditions for the SoC. (a) Heavy-load condition. (b) Medium- or light-load conditions. (c) Ultralight-load condition.

B. Regular Energy Requirement in SoC (Medium- and Light-Load Conditions)

To enhance the transient operation and derive the good power conversion efficiency at both medium and light loads, the PCS enables the hybrid operation for the power module as shown in Fig. 4(b). In steady state, the APU can act as the high-side power switch of a buck converter to minimize power loss. The gate drive voltage of $M_{\rm APU}$ is connected to the driving signal $V_{\rm GP}$ that activates the pure switching regulator operation with the step-down function. However, the transient response of a switching regulator is still restricted by the switching control loop and the off-chip inductor. To properly enhance the transient response for minimizing the drop voltage and shortening the recovery time, the linear control loop with APU can realize the goal thought the utilization of the LDO regulator. It can carry out the superior transient operation during the load transient period owing to its larger system bandwidth compared to switching regulators, which typically limit the system bandwidth within only 10–20% of switching frequency. That is, the APU will be the power switch along with M_P of a buck converter in steady state, and acts as the pass device of LDO when the load transient occurs with the hybrid operation.

The hybrid operation exhibits through the indication of hybrid setting circuit after receiving the demand of increased load from the power controller in SoC. The control signal $V_{\rm PMS}$ can

inform $M_{\rm APU}$ to behave as a linear regulator and wait for the load variation before the coming of step-up load transient. Consequently, the transient dip voltage can be alleviated and the transient response time can be shortened. As depicted in Fig. 3, the error amplifier $\rm EA_2$ and the low-output-impedance (LOI) buffer are used to modulate the gate control signal $V_{\rm PL}$ for the pass device $M_{\rm APU}$ in order to derive the adequate system loop gain and to ensure the system stability. Moreover, the current $I_{\rm MC}$ can help move the load current driving from the LDO regulator to the switching regulator at the end of the load transient period. That is, the replica current $I_{\rm MC}$, which is proportional to the current flowing through $M_{\rm APU}$, will charge the compensation capacitance C_C in the switching control loop and raise the voltage level of $V_{\rm EA1}$ for increasing the driving capability of a buck converter. Thus, the load driving provided by the LDO regulator will be decreased so as to enhance the power conversion efficiency. When the output voltage is regulated to its rated value, the APU will be switched back and thereby being the power switch for the pure buck operation. V_S, which is proportional to the current flowing through $M_{\rm APU}$ in the LDO, can be used to end the LDO regulator operation as well as the transient response with the hybrid setting circuit. As a result, this hybrid operation can guarantee an improved transient response with a low dip voltage as well as the decreased transient recovery time, and more specifically, can properly handle the upcoming load variation in the SoC. In steady state, the APU can also help enhance the driving capability and the power conversion efficiency.

C. Silent Mode Operation in SoC (Ultralight-Load Condition)

The silent mode operation is the commonly used methodologies in the SoC to minimize the power dissipation. The power consumption will be decreased below 1 mA [1] in the silent mode, which is improper to utilize the switching regulator as the power module due to its deserved power loss. Thus, the LDO regulator becomes a good candidate at ultralight loads. As shown in Fig. 4(c), $M_{\rm APU}$ behaves as a pass device of LDO to regulate the output voltage along with the linear control loop that monitors the output load condition and generates the gate control signal $V_{\rm PL}$ for $M_{\rm APU}$. Therefore, not only the output voltage regulation can be ensured, but also the power conversion efficiency at ultralight loads can be guarantees by the PCS controlled power module.

III. Stability Analysis of the Hybrid Operation in the PCS

The proposed PCS forms the different supply mechanism according to the different load conditions. The switching regulator in the PCS is implemented with the current-mode buck converter, which generates a load-dependent system pole at output. The PI compensator can be utilized to stabilize its operation by inserting a pair of compensation pole and zero [17]–[19]. However, the hybrid operation is activated under both medium- and light-load conditions with an upcoming load transient response. That is, the switching regulator and the LDO regulator simultaneously supply power to the SoC system. Thus, the stability of the hybrid operation needs to be carefully considered to guarantee the smooth load transient response.

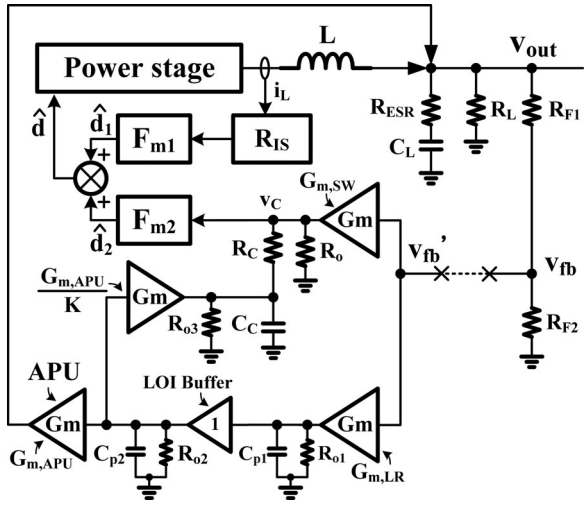

Fig. 5. Equivalent small-signal model of the hybrid operation in the proposed PCS.

Fig. 5 shows the small-signal illustration of the hybrid operation in the PCS. By breaking up the feedback loop, the system loop gain can be derived to demonstrate the system stability. The error amplifier in the switching control loop provides the transconductance $G_{m,\rm SW}$ and the output resistance R_o to ensure the high dc voltage gain. The current sensing implementation, which conveys the inductor current information into the controller, can be modeled as the sensing resistance R_{IS}. F_{m1} and F_{m2} are the transferring coefficients of the analog-to-digital conversion for determining the operated duty cycle in the buck converter. In addition, the transfer function of the PI compensation with the error amplifier is illustrated in

$$\left.\frac{v_c}{v'_{fb}}\right|_{\rm Switching} = G_{m,\rm SW}R_o\frac{1+sC_CR_C}{1+sC_C(R_C+R_o)} = A_{v,\rm SW}\frac{1+(s/\omega_z)}{1+(s/\omega_p)}. \quad (1)$$

C_C and R_C generate the compensation pole ω_p and the compensation zero ω_z, which is regarded as the system dominant pole and is used to extend the system bandwidth by canceling the effect of system load-dependent pole at output, respectively, in the pure buck converter operation. The loop gain of the switching buck converter can be shown as

$$L_{\rm SW}(s) = \left.\frac{v_{fb}}{v'_{fb}}\right|_{\rm Switching} = \frac{R_{F2}}{R_{F1}+R_{F2}} \times \frac{G_{m,\rm SW}R_o(1+sC_CR_C)}{1+sC_C(R_C+R_o)}\frac{R_L(1+sC_LR_{\rm ESR})}{R_{IS}(1+sC_LR_L)}. \quad (2)$$

In addition, the LDO regulator in the proposed PCS is implemented with an inserted buffer stage that aims to guarantee stable operation. The error amplifier in the linear control loop can monitor the output voltage variation by generating the

transconductance $G_{m,\mathrm{LR}}$. The LOI buffer stage carries out the output resistance R_{o2} and the parasitic gate capacitance C_{p1} to separate the nondominant poles. The APU forms as the pass transistor in the LDO regulator to provide the transconductance $G_{m,\mathrm{APU}}$, which varies according to the driving condition of the LDO regulator. The loop gain of the LDO regulator is shown in

$$L_{\mathrm{LR}}(s) = \left.\frac{v_{fb}}{v'_{fb}}\right|_{\mathrm{Linear}} = \frac{R_{F2}}{R_{F1}+R_{F2}} \times \frac{G_{m,\mathrm{LR}}R_{o1}G_{m,\mathrm{APU}}R_L(1+sC_LR_{\mathrm{ESR}})}{(1+sC_{p1}R_{o1})(1+sC_{p2}R_{o2})(1+sC_LR_L)}. \quad (3)$$

Through the combination of the switching control loop and the linear control loop, the hybrid operation in the PCS can be activated. With the sensing mechanism to generate the current I_{MC} shown in Fig. 3 for transferring the current from the LDO regulator to the switching buck converter, the signal path with the transconductance $G_{m,\mathrm{APU}}/K$ needs to be included in the stability analysis of the hybrid operation. The transfer function of the feedback node to the control signal of the switching buck converter is depicted in

$$\left.\frac{v_c}{v'_{fb}}\right|_{\mathrm{Hybrid}} = G_{m,\mathrm{SW}}R_o\frac{(1+sC_CR_C)}{1+sC_C(R_C+R_o)} + \frac{G_{m,\mathrm{LR}}R_{o1}(G_{m,\mathrm{APU}}/K)R_{o3}}{(1+sC_{p1}R_{o1})(1+sC_{p2}R_{o2})(1+sC_CR_{o3})}. \quad (4)$$

The factor K is the current sensing ratio between the current of the LDO regulator and I_{MC}. Therefore, the transfer function of the dual loop integration is shown in (5), at the bottom of this page, and thus the loop gain of the PCS in hybrid operation is illustrated in (6), shown at the bottom of this page.

The dc voltage gain in the hybrid operation is contributed by both the switching loop and the linear loop. The illustration of the poles and zeros in the hybrid operation is shown in

$$L_{\mathrm{HB}}(s) = \frac{v_{fb}}{v'_{fb}} = \frac{R_{F2}}{R_{F1}+R_{F2}} \times \frac{R_L}{R_{IS}}\left[G_{m,\mathrm{SW}}R_o + G_{m,\mathrm{LR}}R_{o1} \times \left(\frac{G_{m,\mathrm{APU}}}{K}R_{o3} + G_{m,\mathrm{APU}}R_{IS}\right)\right] \times \frac{\left(1+\frac{s}{\omega_{z1}}\right)\left(1+\frac{s}{\omega_{z2}}\right)\left(1+\frac{s}{\omega_{\mathrm{ESR}}}\right)}{\left(1+\frac{s}{\omega_p}\right)\left(1+\frac{s}{\omega_{ps}}\right)\left(1+\frac{s}{\omega_{pa}}\right)\left(1+\frac{s}{\omega_{\mathrm{ph1}}}\right)\left(1+\frac{s}{\omega_{\mathrm{ph2}}}\right)}. \quad (7)$$

The pole ω_p generated by the PI compensator is located at the low-frequency region as the system dominate pole. The compensation zeros, ω_{z1} and ω_{z2}, can be used to cancel the effect of output load-dependent system pole ω_{ps} and the nondominate pole ω_{pa} at the sensing path of the current I_{MC}. Fig. 6 shows the frequency response of the hybrid operation in the PCS. The system bandwidth can be enlarged in the hybrid operation, so as to minimize the voltage drop at the output node. With the change of K, the locations of the compensation zeros are varied. That is, compared with the pure buck operation, the different utilization of K results in the distinct system phase margin, which affects the system stability. The utilization of a smaller factor of K indicates the larger of the sensing current I_{MC}, and thereby the worse of the system phase margin. In addition, the nondominant poles, ω_{ph1} and ω_{ph2}, which are carried out from the LOI buffer in the LDO regulator, are put at high frequency, so the system phase margin will not be deteriorated. As a result, the stable hybrid operation can be guaranteed that achieves the

$$\left.\frac{v_{\mathrm{out}}}{v'_{fb}}\right|_{\mathrm{Hybrid}} = \left[\left(\frac{G_{m,\mathrm{SW}}R_o(1+sC_CR_C)}{1+sC_C(R_C+R_o)} + \frac{G_{m,\mathrm{LR}}R_{o1}\frac{G_{m,\mathrm{APU}}}{K}R_{o3}}{(1+sC_{p1}R_{o1})(1+sC_{p2}R_{o2})(1+sC_CR_{o3})}\right)\frac{R_L(1+sC_LR_{\mathrm{ESR}})}{R_{IS}(1+sC_LR_L)} + \frac{G_{m,\mathrm{LR}}R_{o1}G_{m,\mathrm{APU}}R_L(1+sC_LR_{\mathrm{ESR}})}{(1+sC_{p1}R_{o1})(1+sC_{p2}R_{o2})(1+sC_LR_L)}\right]$$
$$\approx \frac{(1+sC_LR_{\mathrm{ESR}})\left[\frac{R_L}{R_{IS}}\left(G_{m,\mathrm{SW}}R_o(1+sC_CR_C)(1+sC_CR_{o3}) + G_{m,\mathrm{LR}}R_{o1}\frac{G_{m,\mathrm{APU}}}{K}R_{o3}(1+sC_CR_o)\right) + G_{m,\mathrm{LR}}R_{o1}G_{m,\mathrm{APU}}R_L(1+sC_CR_o)(1+sC_CR_{o3})\right]}{(1+sC_LR_L)(1+sC_CR_o)(1+sC_CR_{o3})(1+sC_{p1}R_{o1})(1+sC_{p2}R_{o2})} \quad (5)$$

$$L_{\mathrm{HB}}(s) = \frac{v_{fb}}{v'_{fb}} \approx \frac{R_{F2}}{R_{F1}+R_{F2}} \times \frac{R_L}{R_{IS}}\left[G_{m,\mathrm{SW}}R_o + G_{m,\mathrm{LR}}R_{o1}\left(\frac{G_{m,\mathrm{APU}}}{K}R_{o3} + G_{m,\mathrm{APU}}R_{IS}\right)\right]$$
$$\times \frac{(1+sC_LR_{\mathrm{ESR}})\left[1+s\frac{G_{m,\mathrm{SW}}R_oC_C(R_C+R_{o3}) + G_{m,\mathrm{LR}}R_{o1}\frac{G_{m,\mathrm{APU}}}{K}R_{o3}C_CR_o + G_{m,\mathrm{LR}}R_{o1}G_{m,\mathrm{APU}}R_{IS}C_C(R_C+R_{o3})}{G_{m,\mathrm{SW}}R_o + G_{m,\mathrm{LR}}R_{o1}\frac{G_{m,\mathrm{APU}}}{K}R_{o3} + G_{m,\mathrm{LR}}R_{o1}G_{m,\mathrm{APU}}R_{IS}} + s^2\frac{G_{m,\mathrm{SW}}R_oC_CR_CC_CR_{o3} + G_{m,\mathrm{LR}}R_{o1}G_{m,\mathrm{APU}}R_{IS}C_CR_oC_CR_{o3}}{G_{m,\mathrm{SW}}R_o + G_{m,\mathrm{LR}}R_{o1}\frac{G_{m,\mathrm{APU}}}{K}R_{o3} + G_{m,\mathrm{LR}}R_{o1}G_{m,\mathrm{APU}}R_{IS}}\right]}{(1+sC_LR_L)(1+sC_CR_o)(1+sC_CR_{o3})(1+sC_{p1}R_{o1})(1+sC_{p2}R_{o2})} \quad (6)$$

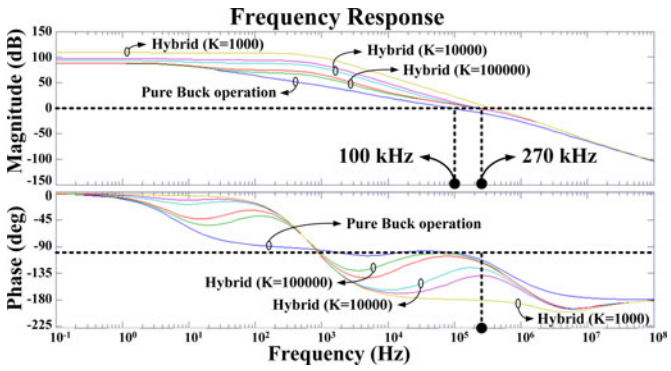

Fig. 6. Simulated frequency response of the proposed PCS in the hybrid operation ($I_{\mathrm{Load}} = 200\,\mathrm{mA}$).

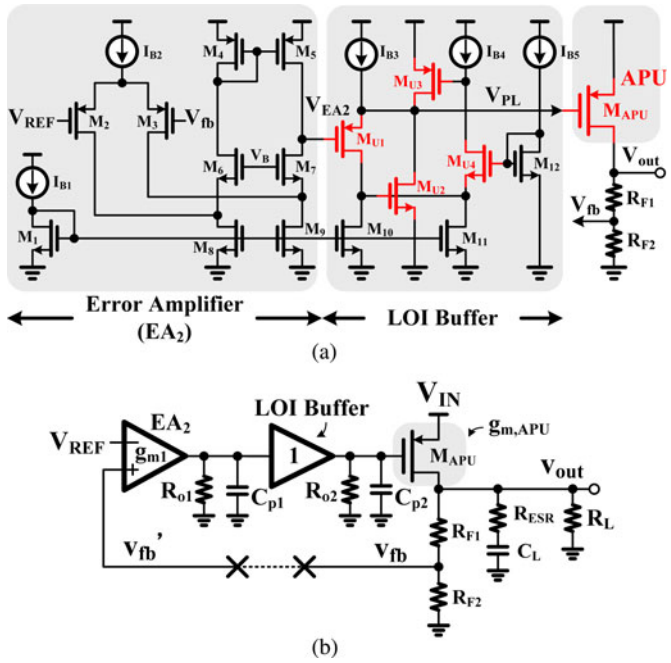

Fig. 7. (a) Schematic of the LDO regulator in the PCS. (b) Loop gain of the LDO regulator.

enhanced transient response for providing a satisfactory supply in the SoC.

IV. Circuit Implementation

A. LDO Regulator With the LOI Buffer

The LDO regulator in the PCS can be activated under both hybrid operation and ultralight-load conditions. Fig. 7(a) shows the schematic of the LDO regulator, which contains the linear control loop and the pass device M_{APU} as depicted in Fig. 3. EA_2 provides the transconductance g_{m1} and the output resistance of R_{o1} in Fig. 7(b). However, due to the use of a large off-chip filter capacitor C_L, the loop dominate pole must be put at the output node. A low-frequency nondominate pole, which would appear at the gate of the pass device V_{PL} without the LOI buffer, will degrade the loop stability. Thus, the proposed LOI buffer is designed to generate a small output resistance R_{o2} for separating the nondominate pole as the separate high-frequency poles to obtain the satisfactory loop phase margin.

The LOI buffer also helps enhance the slew rate of the error amplifier and the system bandwidth due to its small input gate capacitance compared to the pass transistor. In the conventional design, using a bipolar transistor reduces the output impedance of a buffer stage to guarantee the system stability [14]. Nevertheless, the additional cost is required owing to the NPN bipolar utilization. The proposed LOI buffer constitutes a super source follower structure [20] through the utilization of double shunt feedback loops, which are formed through M_{U1}–M_{U2} and M_{U1}–M_{U3}–M_{U4}, that can effectively reduce the output resistance R_{o2} derived at the gate of pass device V_{PL} as shown in

$$R_{o2} \approx \frac{1}{g_{mU1}g_{mU2}r_{oU1} + g_{mU1}g_{mU3}g_{mU4}r_{oU1}r_{oU4}}. \quad (8)$$

Here, g_{mU1}–g_{mU4} and r_{oU1}–r_{oU4} are the transconductance and the intrinsic resistance of M_{U1}–M_{U4}, respectively. The implementation is similar to the flipped voltage follower structure [20], so R_{o2} can be noticeably decreased without requiring high current consumption or a large aspect ratio of M_{U1}. The loop gain of the LDO regulator is derived in (9) from the depiction of Fig. 7(b). g_{m1} and $g_{m,\mathrm{APU}}$ are the transconductances of EA_2 and M_{APU}, respectively. $R_{o,\mathrm{pass}}$ is the equivalent resistance of a pass device while R_L represents the load resistance at the output. C_{p1} and C_{p2} are the parasitic capacitances derived at nodes V_{EA2} and V_{PL}, respectively. The loop stability can be assured since the nondominate poles can be put at high frequencies through the proposed LOI buffer

$$L_{\mathrm{LDO}}(s) = \frac{v_{fb}}{v'_{fb}} \approx \frac{R_{F2}}{R_{F1}+R_{F2}} \times \frac{g_{m1}R_{o1}g_{m,\mathrm{APU}}R_{oL}(1+sC_LR_{\mathrm{ESR}})}{(1+sC_{p1}R_{o1})(1+sC_{p2}R_{o2})(1+sC_LR_{oL})}$$

$$\text{where} \quad R_{oL} = R_L||R_{o,\mathrm{pass}}||(R_{F1}+R_{F2}). \quad (9)$$

B. Hybrid Setting Circuit

Fig. 8 shows the hybrid setting circuit, which generates the control signals V_{sw1}, V_{sw2}, and Sel to realize the supply mechanism in the PCS through the indication of two-bit signal V_{PMS} from the SoC. As shown in Fig. 8(a), the hybrid operation occurs when the PCS receives the positive trigger of $V_{\mathrm{PMS}}[0]$ along with the setting on $V_{\mathrm{PMS}}[1]$. The APU will behave as the pass device for the LDO regulator, and thereby waiting for the upcoming load transient response. However, to enhance the power efficiency in the PCS, the LDO regulator should be shut down in steady state excepting for the ultralight-load condition. That is, when the sensing signal V_S, which conveys the current information of the pass device in the LDO, becomes smaller than a predefined reference voltage V_{RL}, the APU will be switched back as the power switch for the buck converter. Furthermore, the offset-canceled (OFC) comparator, which contains the two-stage amplifier with two-phase operation and is used to guarantee this handover operation at the end of load transient response, is shown in Fig. 8(b). Phase 1 only activates

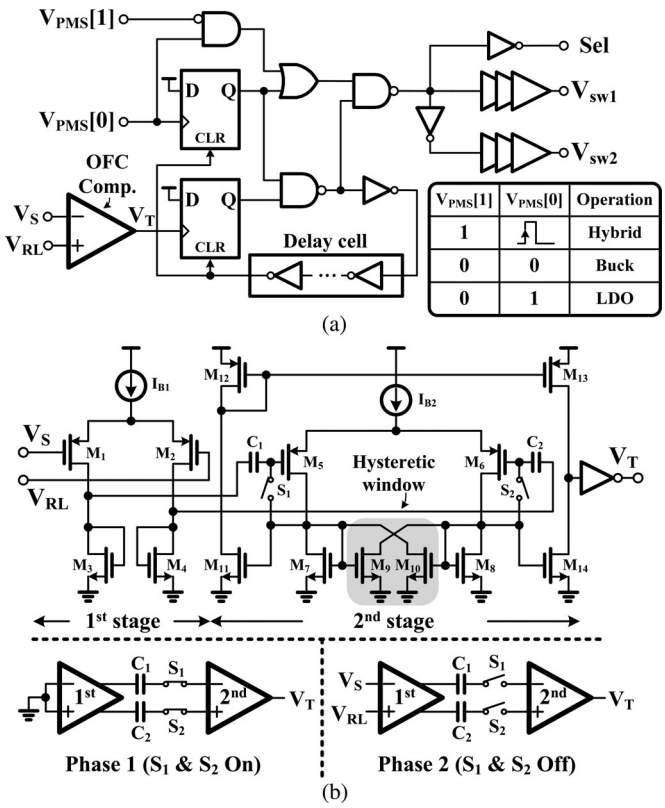

Fig. 8. (a) Schematic of the hybrid setting circuit. (b) Schematic of the OFC comparator and its brief operation.

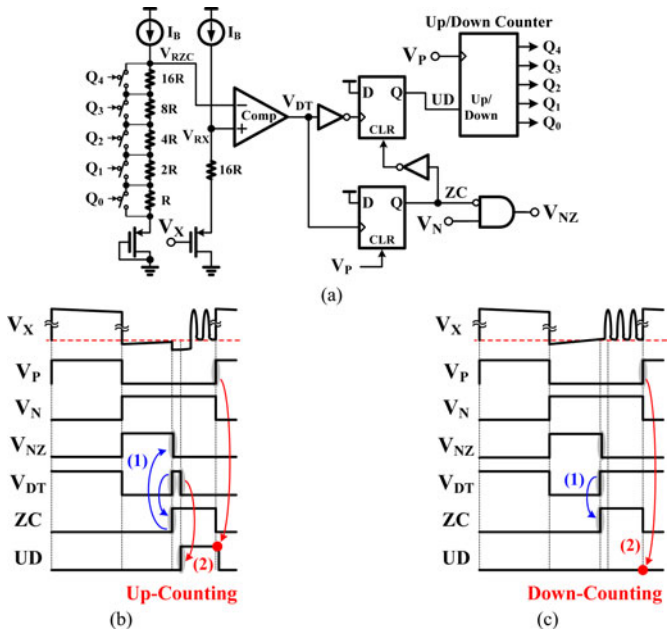

Fig. 9. (a) Schematic of the proposed ZCA circuit. (b) Time diagram of the up-counting operation. (c) Time diagram of the down-counting operation.

with the pure switching regulator operation, while phase 2 is enabled when hybrid operation occurs. The first stage is regarded as the preamplifier to amplify the realistic voltage difference of the effective input signals.

Two flying capacitors, C_1 and C_2, can be used to record the offset voltage, which is resulted from the realistic mismatch after the chip manufacturing. Fortunately, the offset voltage can be canceled though these stored charges in phase 2. The second stage is then be implemented with a well-known comparator structure to determine the optimal handover point at the end of hybrid operation. Therefore, the hybrid operation can be ended; nevertheless, it guarantees the high efficiency operation in steady state since the switching regulator can handle all of the energy delivery for outputs and is waiting for the next hybrid activation. Moreover, the pure buck operation and the LDO operation in the PCS are activated at heavy loads and ultralight loads, respectively. These operations are indicated by the signal $V_{\rm PMS}[0]$ when $V_{\rm PMS}[1]$ is fixed to low. Summaries of the proposed hybrid setting circuit are listed in the attached table of Fig. 8(a).

C. ZCA Circuit

To properly guarantee the power conversion efficiency under the steady-state light-load condition, the discontinuous-conduction-mode (DCM) operation can be realized along with the pulse frequency modulation (PFM) to obtain the reduced power loss in the buck converter. That is, for preventing the occurrence of inversed inductor current, the low-side power switch needs to be turned OFF once the inductor current decreases to zero. In the prior implementation of zero current detection [21]–[23], a simple comparator is used to determine the operation by directly modulating the voltage variations of switching node V_X. However, the offset voltage of a comparator and the propagation delay of a driver in power stage will postpone the turned-off operation on the low-side power switch, which results in the negative inductor current and the degradation of power conversion efficiency at light loads. Thus, to derive the optimal operation of zero current detection in the PCS, the proposed ZCA circuit is shown in Fig. 9(a). By monitoring the voltage variation on switching node V_X, the output of the comparator will trigger the up/down counter so that the reference voltage level $V_{\rm RZC}$ generated by a resistor string can be adjusted to track the optimal zero current switching point.

If the zero current detection is activated too early, the low-side power switch will be disabled with a positive inductor current. That is, the parasitic diode of the low-side power switch will be turned ON automatically to conduct the inductor current as shown in Fig. 9(b). V_P and V_N are the control signals for power switches in the switching control loop generated by the PWM generator in Fig. 3. V_X can be pulled to a negative voltage value with a conductive drop voltage of a parasitic diode, which is typically about 0.7 V. When the output of comparator $V_{\rm DT}$ sets a positive trigger, which represents the detection of zero inductor current during the low-side power switch turn-on period, *ZC* will be enabled to turn OFF the low-side power switch by $V_{\rm NZ}$. Besides, the appearance of negative voltage on V_X leads the comparator to output a negative trigger to set the up/down counter through *UD*. As a result, the up-counting can be activated at the beginning of a next switching period, so as to raise the reference voltage $V_{\rm RZC}$ for delaying the timing of

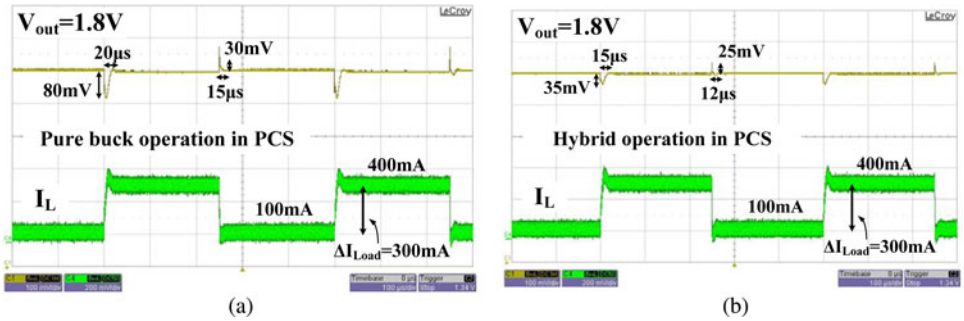

Fig. 10. Measured load transient response in the PCS with the load step from 100 to 400 mA. (a) Pure buck operation. (b) Hybrid operation.

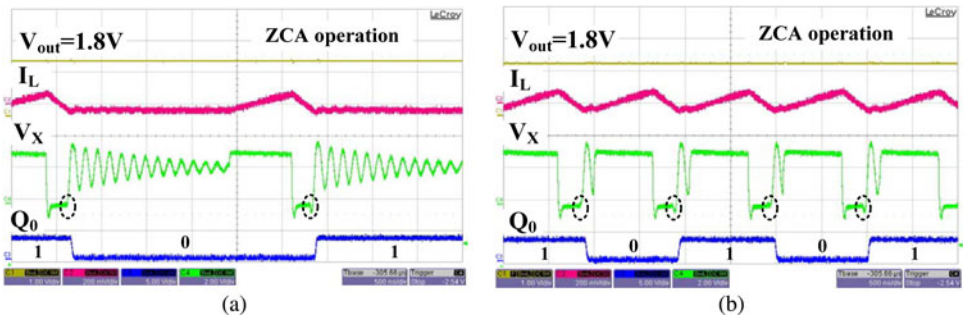

Fig. 11. Measured ZCA operation in the PCS operated buck converter. (a) With a 10-mA load current. (b) With a 40-mA load current.

zero current detection. On the other hand, when the occurrence of zero inductor current detection is late, the reversed inductor current would appear even to deteriorate the power conversion efficiency as shown in Fig. 9(c). V_X will be raised after the low-side power MOSFET is turned OFF. That is, $V_{\rm DT}$ can have no longer to send a trigger voltage for the up/down counter, so the down-counting operation will be realized. As a result, the operation of zero current detection in the switching regulator can be automatically adjusted, so as to eliminate the negative inductor current and compensate the effect of comparator offset as well as the propagation delay of a driver.

V. Experimental Results

The proposed PCS for achieving the power module integration in SoC was fabricated in a 0.25-μm CMOS process. The off-chip inductor and the output filter capacitor are 4.7 μH and 4.7 μF, respectively. The switching frequency of a buck converter is 1 MHz. The nominal output voltage is 1.8 V with the battery input voltage range of 2.7–4.3 V. The maximum load current is about 600 mA. Fig. 10 shows the measured load transient response in the proposed PCS. When the load current changes from 100 to 400 mA, the PCS with the pure switching regulator operation derives the output voltage drop of 80 mV and the recovery time of 20 μs shown in Fig. 10(a). That is, the APU in the power stage continuously behaves as a part of the high-side power switch for a buck converter. However, the performance of transient response is restricted by the system compensation implementations, which are the essential design consideration for guaranteeing the system stability. The load transient response with the hybrid operation in the PCS is shown in Fig. 10(b). The output voltage drop can be reduced to 35 mV with the transient recovery time of 15 μs. The APU can act as the pass device in the LDO regulator when it receives the demand of the upcoming load increasing from the SoC. The larger system bandwidth can be derived in hybrid operation to immediately handle extra energy request so that the load transient response can be improved. That is, the transient voltage drop can be reduced by 56% and the transient recovery time is improved by 25%. The load regulation is about 0.015 mV/mA because of the satisfactory dc voltage gain in the hybrid operation. Furthermore, the hybrid operation is changed back to the pure buck operation at the end of load transient response that can enhance the power conversion efficiency in steady state.

Fig. 11 shows the measured ZCA operation. The DCM operation is activated in a buck converter to maintain the light-load efficiency. The proposed ZCA operation can track the response of the switching node V_X after the low-side power switch is turned OFF, and automatically adjust the detection level to derive the optimal zero current detection operation. Fig. 11(a) shows the PCS operated buck converter with 10-mA load current. The variation on the last bit of the up/down counter Q_0 in a ZCA circuit demonstrates the auto adjusting operation through the response of V_X. Thus, the effect of the propagation delay in a driver can be compensated so that the negative inductor current will no longer be derived. The 40-mA load current condition of the DCM operation in a buck converter is depicted in Fig. 11(b). The automatic zero inductor adjusting mechanism is still activated to eliminate the occurrence of negative inductor current. Consequently, the proposed ZCA circuit in the PCS can

TABLE I
DESIGN SPECIFICATION OF THE PROPOSED PCS IN SOC

Technology	0.25 μm CMOS process
Input voltage	2.7 - 4.2 V
Off-chip inductor	4.7 μH
Off-chip capacitor	4.7 μF
Switching frequency	1 MHz (for buck converter)
Output voltage	1.8 V (Nominal)
Maximum load current	600 mA
Transient dip voltage (Hybrid operation)	35 mV (56% improvement) Load changes from 100 mA to 400 mA
Transient recovery time (Hybrid operation)	15 μs (25% improvement) Load changes from 100 mA to 400 mA
Power conversion efficiency	Peak value of 94 %
Chip area	1500 μm x 1100 μm (Including pads)

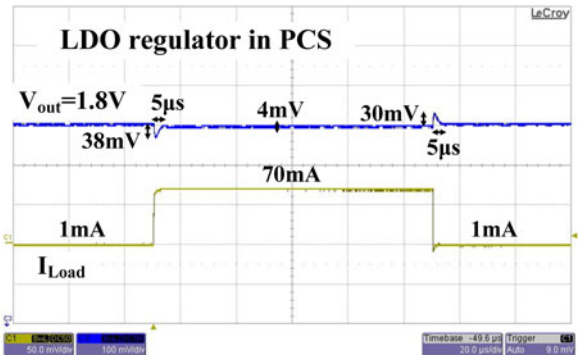

Fig. 12. Measured LDO regulator in the PCS with the load variation between 1 and 70 mA.

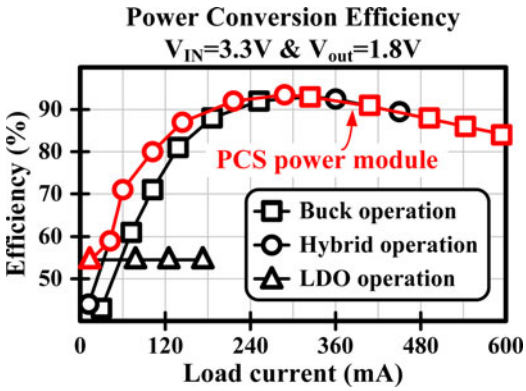

Fig. 13. Power conversion efficiency of the proposed PCS power module.

further strengthen the light-load operation in the power module, and thereby improving the light-load efficiency.

Fig. 12 shows the measured LDO regulator operation in the PCS. The output derives a 38-mV voltage drop with the step-up load variation from 1 to 70 mA. The transient recovery time is about 5 μs. The output voltage overshoot is derived as 30 mV with the 5 μs transient settling time when the load changes from 70 to 1 mA. It can demonstrate the stable operation in the LDO regulator since the LOI buffer can move the nondominate poles to high frequencies without causing the phase deterioration. The load transient response is about 0.055 mV/mA. Fig. 13 shows the measured power conversion efficiency of the proposed PCS. With the different supply mechanism according to the distinct

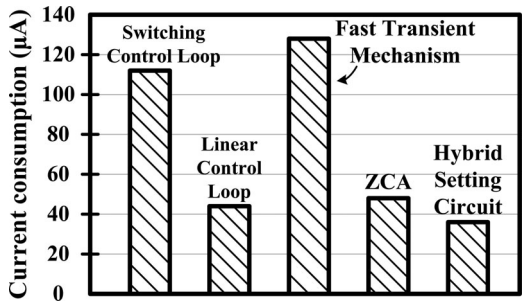

Fig. 14. Current consumption of the distinct power cloud units in the PCS.

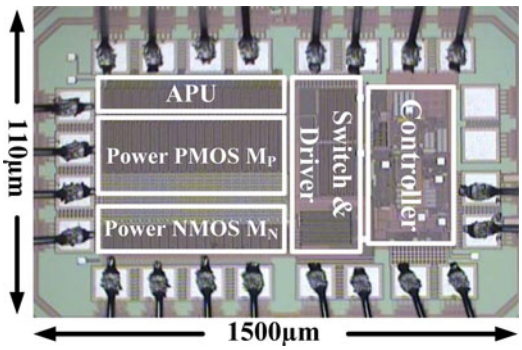

Fig. 15. Chip micrograph.

load conditions, the power conversion efficiency can be kept within a relatively high value. Moreover, the hybrid operation can enhance the load transient response but will degrade the efficiency in steady state owing to the switchable APU. The current consumptions of the distinct power cloud units in the PCS are depicted in Fig. 14. It can help further demonstrate the operation in the PCS with the different output load conditions. Fig. 15 shows the chip micrograph with a 1.65 mm^2 active silicon area including embedded power switches and the APU. The detailed design specifications are listed in Table I.

VI. CONCLUSION

The PCS is proposed to be the appropriate power module for the SoC. The different power cloud units will form the distinct supply mechanism in the PCS through the power demand from the SoC. When the PCS receives large energy requirements,

the pure switching regulator operation is activated to provide sufficient energy driving capability with high power conversion efficiency. The hybrid operation is realized under medium-load or light-load conditions to utilize the APU to carry out both LDO regulator function to enhance the load transient response and the pure buck operation for guaranteeing efficiency. Besides, the LDO regulator will take over the full energy delivery scheme in the PCS when the SoC enters in the silent mode, which can effectively reduce current consumption but maintain the output voltage regulation. The hybrid setting circuit and the ZCA circuit can also help strengthen the performance of the PCS. The chip was fabricated in a 0.25-μm CMOS process. Experimental results demonstrate that the 56% load transient dip voltage is derived with an improvement of 25% transient recovery time that both the transient response and power conversion efficiency can be ensured at the same time, and the 94% peak efficiency.

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