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EMPIRICAL MODELING FOR GATE-CONTROLLED COLLECTOR CURRENT OF LATERAL BIPOLAR TRANSISTORS IN AN n-MOSFET STRUCTURE

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Abstract—The I–V characteristics of a gated lateral bipolar transistor in an n-MOSFET structure have been measured. The measured collector current has exhibited two distinct components: (i) the gate-controlled collector current due to the modulation of the surface space-charge region; and (ii) the pure lateral bipolar transistor collector current which is independent of the gate bias applied. These two components have been separated experimentally and have been reproduced by analytic model expressions. The work is useful not only for understanding the hybrid-mode operation but also for designing appropriately the gated lateral bipolar transistors.

I. INTRODUCTION

Recently, the gated lateral bipolar transistors based on the MOSFET structures have been proposed[1–4] and have exhibited experimentally new features such as high current gain[1–4], high cut-off frequency[4], and improved low-temperature characteristics[2]. Importantly, the fabrication process for such bipolar transistors is compatible with the MOS-based technology, which can greatly reduce the cost and complexity of the process for the mixed bipolar-MOS integrated circuits[1–4]. To explain high current gain in the gated lateral bipolar transistors, the gate-induced barrier lowering for enhancing carrier injection from the emitter has been introduced and has been employed to qualitatively interpret the hybrid-mode operation of the gated lateral bipolar transistors[2,3].

In this paper we report the work of quantitatively modeling the collector current of the gated lateral bipolar transistor. First, the process for fabricating the n-channel LDD MOSFET device based on which the gated lateral n-p-n bipolar transistor is characterized will be described. The measured high current gain comparable with those in [1–4] will also be demonstrated. One of the contributions of the work will be placed on the experimental separation of the collector current into two components:

(i) the gate-controlled collector current due to the modulation of the surface space-charge region; and
(ii) the pure lateral bipolar transistor collector current which is independent of the gate bias applied.

The corresponding model expressions will be presented along with the comparisons with the experimental data.

II. EXPERIMENT

A. Test device

The gated lateral n-p-n bipolar transistor under study was based on the LDD n-channel MOSFET fabricated by a conventional twin-well CMOS process. The starting material was ⟨100⟩ oriented p-type substrate with the resistivity of 8–12 Ω-cm. The p-well was formed by an implantation of $4.5 \times 10^{12}\,cm^{-2}$ boron atoms at 80 keV and then a 1150°C thermal drive-in. The dosage and energy of boron threshold implant were $1.9 \times 10^{12}\,cm^{-2}$ and 25 keV, respectively. The n^+ polysilicon gate was deposited on a 18 nm gate oxide. The low-doped source/drain implantation was implemented by $2.0 \times 10^{13}\,cm^{-2}$ phosphorus atoms at 60 keV. An oxide spacer of 2500 Å thickness was grown and the highly-doped source/drain implantation of $3.0 \times 10^{15}\,cm^{-2}$ arsenic atoms at 80 keV was used. The peak doping concentration of the implanted region beneath the gate was about $6.0 \times 10^{16}\,cm^{-3}$. The gate length and width were 1.5 and 10 μm, respectively. The schematic cross section of the device is drawn in Fig. 1.

B. Device characteristics

To measure the I–V characteristics of the gated lateral bipolar transistor, the test device was biased in common-base configuration as shown in Fig. 1. The measured Gummel plot (at $V_{CB} = 1.0$ V) as a function

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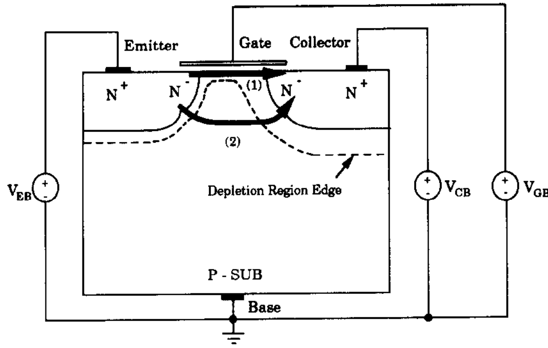

Fig. 1. Schematic cross section view of the test device. The total collector current is composed of two components: (1) the gate-controlled collector current in the surface space-charge region; and (2) the collector current of the pure lateral bipolar transistor.

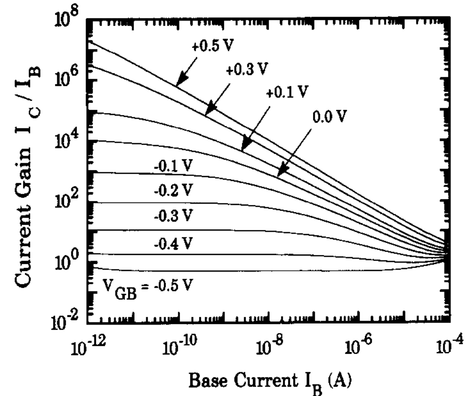

Fig. 3. The current gain vs the base current corresponding to Fig. 2 for nine different gate biases. $V_{CB} = 1.0$ V.

of gate bias is shown in Fig. 2. From Fig. 2 it can be observed that the base current is independent of gate bias while the collector current is a strong function of gate bias. Such observation results can be reasonably attributed to the gate-induced barrier lowering that enhances electron injection from the n^+ emitter but not at all affects the holes injected into and recombined within the emitter[3]. Also it can be seen from Fig. 2 that for the low current level (i.e. $< 10^{-6}$ A) a slope of ≈ 60 mV/decade appears not only in the base current vs the emitter bias characteristics but also in the collector current vs the emitter bias characteristics. From the Gummel plot in Fig. 2, the corresponding current gain (I_C/I_B) vs the base current is drawn in Fig. 3. As depicted in Fig. 3 the peak value of current gain increases exponentially with the gate bias. Note that for the case of $V_{GB} = 0$ V, i.e. both the gate and the base are tied together and grounded, the device exhibits a high current gain of over 1000 for a wide base current range, which is comparable with those reported in [1–4]. It can also be observed from Fig. 3 that the range of constant current gain decreases as the gate bias is raised. For $V_{GB} \geqslant 0.3$ V, the constant current gain range disappears and the measured current gain falls off with the increase of base current.

C. Separation of collector current components

The collector current can be separated into two distinct components as schematically depicted in Fig. 1. The component of interest, flowing through the surface space-charge region controlled by the gate bias, can be turned off as the surface beneath the gate is accumulated (i.e. the surface depletion region disappears). Thus the collector current of the pure lateral bipolar transistor can be separated under the strong accumulation condition. Due to the shielding effect of the accumulation charges, the collector current of the pure lateral bipolar transistor is considerably independent of the gate bias. Therefore, the gate-controlled component can be separated by subtracting the collector current of a pure lateral bipolar transistor from the collector current of a gated lateral bipolar transistor.

Figure 4 shows the measured collector current as a function of emitter bias for 10 different gate biases. From the figure, we can observe that the collector current becomes independent of gate bias as the V_{GB} increases negatively over -1.0 V, indicating the

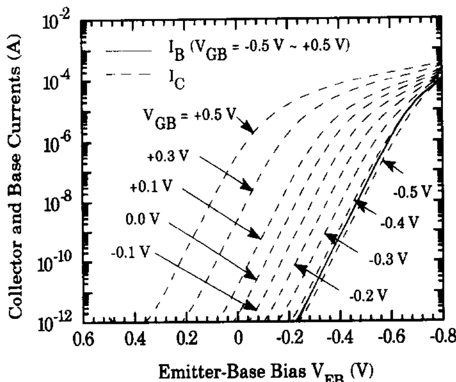

Fig. 2. The Gummel plot of the test device for nine different gate biases. $V_{CB} = 1.0$ V.

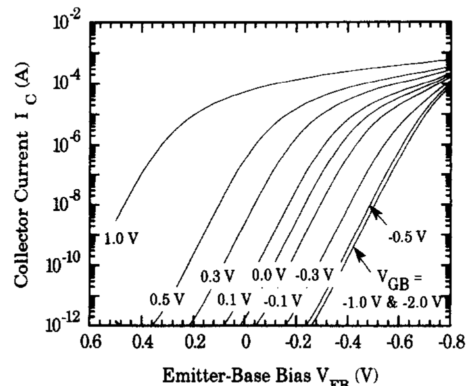

Fig. 4. The measured collector current vs the emitter-base bias for 10 different gate biases. $V_{CB} = 1.0$ V.

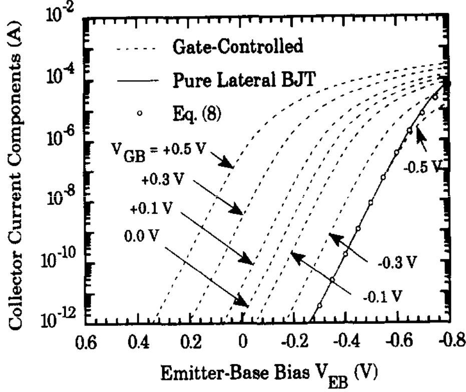

Fig. 5. The two components of the collector current separated from Fig. 4. The calculated results using eqn (8) are also shown for comparison.

strong accumulation of the surface beneath the gate. Therefore, the measured collector current vs emitter bias curves for $V_{GB} = -1.0$ to -2.0 V in Fig. 4 represent the collector current of a pure lateral bipolar transistor. The two components of the collector current have been subsequently separated and are given in Fig. 5.

III. MODEL EXPRESSIONS

A. Gate-controlled collector current

As mentioned above, the gate-controlled collector current exists only when the surface is depleted or inverted. The condition for the surface depletion is $V_{GB} > V_{FB}$, where V_{FB} is the flat-band voltage (≈ -0.75 V, as determined by C–V method in this work). In the surface depletion region, the gate-controlled collector current is dominated by the diffusion component, which is related to the amount of minority carriers (electrons, in this work) climbing over the surface p-n junction barrier. The potential barrier height $q\Psi_{B,e}$ at the surface can be given as[3]

$$q\Psi_{B,e} = q\phi_{bi} + qV_{EB} - q\varphi_c \tag{1}$$

where ϕ_{bi} is the built-in potential of the emitter-base junction and φ_c is the surface potential associated with the gate-to-bulk bias. From eqn (1), we can observe that the potential barrier is lowered by $q\varphi_c$[3]. The potential lowering φ_c can be expressed as[7]

$$\varphi_c = \tfrac{1}{2}\gamma^2 + (V_{GB} - V_{FB}) - \frac{\gamma}{2}\sqrt{\gamma^2 + 4(V_{GB} - V_{FB})} \tag{2}$$

where $\gamma (\equiv t_{ox}/\epsilon_{ox}\sqrt{2q\epsilon_{si}N_B})$ is the body effect coefficient, t_{ox} is the gate oxide thickness, ϵ_{ox} is the oxide permittivity, ϵ_{si} is the silicon permittivity, and N_B is the well (base) doping concentration.

Because the amount of minority carriers is exponentially proportional to $-q\Psi_{B,e}$, the diffusion current is also exponentially proportional to $-q\Psi_{B,e}$. Therefore the diffusion current expression well constructed in the MOSFET subthreshold region $I_{diff,o}$ can be applied[8–10]

$$I_{diff,o} = \frac{I_{CO}}{\sqrt{\frac{q\varphi_c}{kT}}}\exp\left(\frac{q(\varphi_c - V_{EB})}{kT}\right) \times \left(1 - \exp\left(\frac{-qV_{CE}}{kT}\right)\right) \tag{3}$$

where I_{CO} is the current factor to be determined. The diffusion current, $I_{c,diff}$, however, approaches to a limit value I_{limit} as V_{GB} increases above the threshold voltage, which can be modeled empirically by[11]

$$I_{c,diff} = \frac{I_{diff,o}I_{limit}}{I_{diff,o} + I_{limit}}. \tag{4}$$

When the gate bias increases above the threshold voltage, opposite-polarity charges are induced and the surface beneath the gate becomes inverted. The inversion charges contribute to the drift component, which has to be taken into account for accurate modeling of the gate-controlled collector current in a wide current level. The condition for the surface inversion is $V_{GB} \geqslant V_{THO}$, where the threshold voltage V_{THO} can be expressed as[7,10]

$$V_{THO} = V_{FB} + \left(\frac{2kT}{q}\ln\frac{N_B}{n_i} + V_{EB}\right) + \gamma\sqrt{\left(\frac{2kT}{q}\ln\frac{N_B}{n_i} + V_{EB}\right)} \tag{5}$$

where n_i is the intrinsic carrier concentration. If $V_{CB} \geqslant V_{GB} - V_{THO}$, the drift current in the above-threshold regime, $I_{c,drift}$, can be expressed as[12]

$$I_{c,drift} = \frac{I'_{CO}}{1 + \theta(V_{GB} - V_{THO})}(V_{GB} - V_{THO})^2 \quad \text{for } V_{GB} \geqslant V_{THO} \tag{6}$$

where I'_{CO} and θ are two parameters to be determined. The gate-controlled collector current, $I_{C,G}$, therefore, can be written as

$$I_{C,G} = I_{c,diff} + I_{c,drift}. \tag{7}$$

B. Pure lateral BJT collector current

The collector current of the pure lateral bipolar transistor can be modeled by[6]

$$I_{C,B} = \frac{I_o\left[\exp\left(-\frac{qV_{EB}}{kT}\right) - 1\right]}{\frac{1}{2} + \frac{1}{2}\sqrt{1 + 4\frac{I_o}{I_k}\left[\exp\left(-\frac{qV_{EB}}{kT}\right) - 1\right]}} \tag{8}$$

where I_o is the saturation collector current and I_k is the knee current. Both I_o and I_k can be determined from the experimental data. When the emitter-base bias is low (low injection), eqn (8) can be reduced to

$$I_{C,B} \approx I_o\left[\exp\left(-\frac{qV_{EB}}{kT}\right) - 1\right] \tag{9}$$

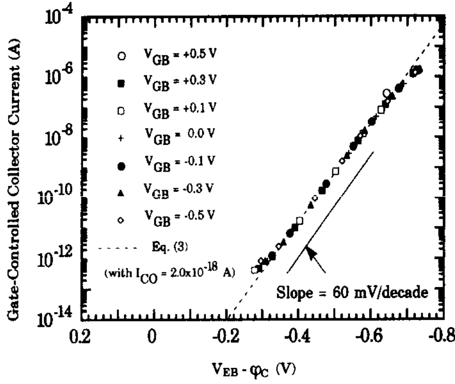

Fig. 6. The measured gate-controlled collector current as a function of the net surface emitter-base junction bias $V_{EB} - \varphi_c$ for 7 different gate biases. The φ_c is calculated by using eqn (2). The collector saturation current I_{CO} in eqn (3) is extracted to be 2.0×10^{-18} A by fitting the experimental data in the low-level injection condition.

which is the ideal expression for the low-level collector current of a bipolar transistor. On the other hand, if the emitter-base bias is high enough (high injection), $I_{C,B}$ can be approximated by

$$I_{C,B} \approx \sqrt{I_o I_k} \exp\left(-\frac{qV_{EB}}{2kT}\right), \tag{10}$$

which indeed shows the $\exp(-qV_{EB}/2kT)$ dependences of the collector current under the high-level injection condition.

IV. RESULTS AND DISCUSSION

From eqn (2), the surface potential φ_c for a given V_{GB} is determined by the parameters γ and V_{FB}. Both the body effect coefficient γ and the flat-band voltage V_{FB} are related to the process parameters such as the base (well) doping concentration, the surface implant energy and dosage, the work function difference, and the gate oxide thickness. According to eqn (1), the potential barrier of minority carriers can be lowered by the surface potential through the gate bias control

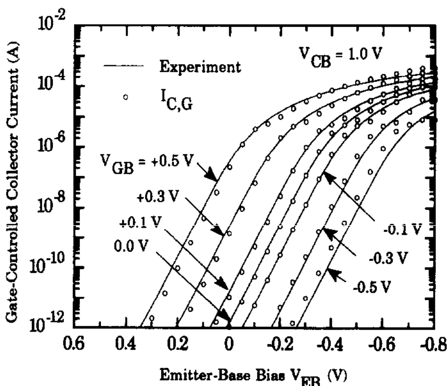

Fig. 7. The comparison of the measured gate-controlled collector current vs emitter bias for 7 different gate biases and the calculated results using eqn (8) with $I_{CO} = 2.0 \times 10^{-18}$ A, $I'_{CO} = 4.36 \times 10^{-4}$ A/V^2, $\theta = 0.32$ V^{-1} and $I_{limit} = 6.25 \times 10^{-6}$ A.

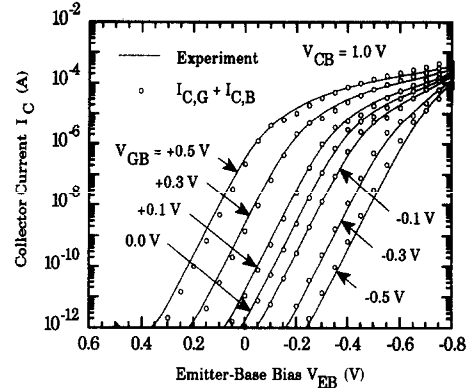

Fig. 8. The comparison of the measured total collector current vs emitter bias for 7 different gate biases and the calculated results by summing eqns (7) and (8).

as analytically described by eqn (2). Since the surface potential φ_c can be analytically obtained from eqn (2) with the process parameters as input variables, the only parameter to be determined when employing eqn (3) is the current factor I_{CO}. The value of I_{CO} has been extracted from the experimental data as demonstrated in Fig. 6. From the Fig. 6 it can be observed that with $I_{CO} = 2.0 \times 10^{-18}$ A the validity of eqn (3) has been identified under the low-level injection condition. It is also noted from Fig. 6 that the net emitter-base junction bias, i.e. $V_{EB} - \varphi_c$, increases by about 60 mV for a factor of 10 increase in the collector current, as transparently revealed by the exponential term in eqn (3). For the above-threshold condition, the drift component as expressed in eqn (6) dominates. The parameters in eqn (6) for best fitting the experimental data are: $I'_{CO} = 4.36 \times 10^{-4}$ A/V^2 and $\theta = 0.32$ V^{-1}. Figure 7 demonstrates the calculated results concerning the gate-controlled component for $V_{GB} = -0.5$ to 0.5 V. From Fig. 7 it can be observed that the superposition of two components $I_{c,diff}$ and $I_{c,drift}$ can yield close agreement with the experimental data.

By appropriately adjusting the parameter values, the measured collector current of the pure lateral bipolar transistor has been reasonably reproduced be eqn (8). With $I_o = 3.43 \times 10^{-17}$ A and $I_k = 1.0 \times 10^{-5}$ A, the calculated results using eqn (8) are plotted in Fig. 5. From Fig. 5, it can be observed that good agreement has been obtained. Again, by a simple combination of eqns (4), (6) and (8), the complete set of expressions for the collector current of the gated lateral bipolar transistor is established. The corresponding calculated results are shown in Fig. 8 where the experimental I–V characteristics in Fig. 4 are re-plotted for comparison. From the figure, we can find reasonable agreement in the low- and high-level current regimes.

V. CONCLUSION

The gated lateral n-p-n bipolar transistor in an n-MOSFET structure has been characterized. Both

the gate-controlled collector current and the pure lateral bipolar collector current, which constitute the whole collector current of the gated lateral bipolar transistor, have been separated experimentally. The corresponding model expressions have been proposed and have been shown to be capable of reproducing the experimental data in a wide current range.

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