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Bipolar switching characteristics of low-power Geo resistive memory

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ABSTRACT

We reported an ultra low-power resistive random access memory (RRAM) combining a low-cost Ni electrode and covalent-bond GeO_x dielectric. This cost-effective Ni/GeO_x/TaN RRAM device has very small set power of 2 μW, ultra-low reset power of 130 pW, greater than 1 order of magnitude resistance window, and stable retention at 85 °C. The current flow at low-resistance state is governed by Poole–Frenkel conduction with electrons hopping via defect traps, which is quite different from the filament conduction in metal-oxide RRAM.

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1. Introduction

As continuously scaling down the size of flash non-volatile memory (NVM) to sub-30 nm [1,2], the number of stored carriers becomes fewer that degrade the data retention and cycling endurance significantly [1]. The resistive random access memory (RRAM) [3–11] has a simple metal–insulator-metal (MIM) structure and bistable resistance states, which is a promising candidate beyond flash memory. Besides, the RRAM has a small cell size, large memory window for multiple level cell (MLC) operation and three-dimensional integration capability. To reach the needed bistable resistance states, non-stoichiometric transition metal-oxides have been used. Good memory device performances have been reported using NiO [3,4], HfO_2 [5] and ZrO_2 [6], ZnO [7], CeO_2 [8], WO_x [9], Cu-doped MoO_x (Cu–MoO_x) [10], and perovskite-type $SrTiO_3$ [11] transition metal-oxides. In most cases, the high work-function Pt electrode was used in these devices to reach a stable switching behavior and lower down the leakage current, but it is difficult to pattern by Pt reactive-ion etching (RIE). Besides, these devices suffer the penalty of high forming power and high set/reset currents of >100 μA, even using expansive noble Pt metal. Recently, the low-power RRAMs with the low current of <10 μA have been reached in GeO_x/$SrTiO_3$ and GeO_x/HfON RRAM devices [12,13], but the effect of buffered GeO_x is still not clear.

In this study, we fabricated an ultra-low power RRAM device using covalent-bond GeO_2 dielectric and low-cost Ni electrode. Very low 2 μW set power, ultra-low 130 pW reset power, more than 1 order of magnitude resistance window and stable data retention at 85 °C were simultaneously reached in the cost-effective Ni/GeO_x/TaN RRAM device.

2. Experimental procedure

The covalent-bond GeO_2 RRAM devices were fabricated on standard Si wafers. To permit VLSI backend integration, the process began with depositing a 200 nm thick SiO_2 layer on Si substrate. Then the 100-nm-thick TaN was deposited by a sputter system with a fixed Ar/N_2 ratio of 5% as the bottom electrode. After that, the 7-nmn-thick amorphous Ge and 8-nm-thick GeO_2 were deposited by e-gun evaporation on bottom TaN. Finally, a 25-nm-thick Ni metal was evaporated and patterned via a metal mask as the top electrode. Similar high work-function Ni electrode was also used for DRAM MIM capacitors. The fabricated devices were characterized by *C–V* and *I–V* using HP4284A precision LCR meter and HP4156C semiconductor parameter analyzer, respectively. All the *I–V* characteristics given in this study were measured at a sweep rate of 10 ms/V.

3. Results and discussion

Fig. 1a shows the *I–V* switching characteristics of Ni/GeO_x/TaN RRAM with different GeO_x thickness of 8 and 12 nm. The RRAM with 8-nm-thick GeO_x shows very small set current of 0.5 μA at 4 V and ultra-low reset current of −0.17 nA at −0.75 V. The asymmetric bipolar switching is attributed to the different work-function between top Ni (5.1 eV) and bottom TaN (4.6 eV) elec-

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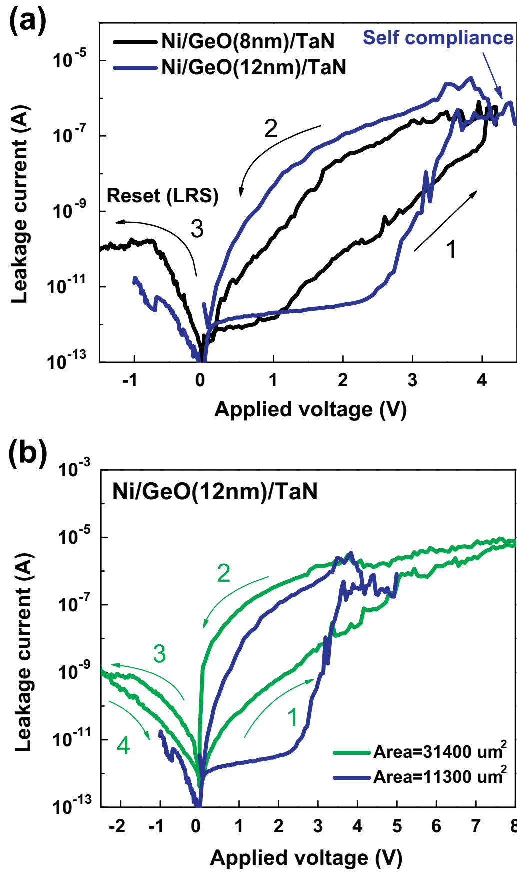

Fig. 1. Swept *I–V* curves of Ni/GeO_x/TaN RRAM with different (a) film thickness and (b) area dimension. The arrows indicate the bias sweeping direction.

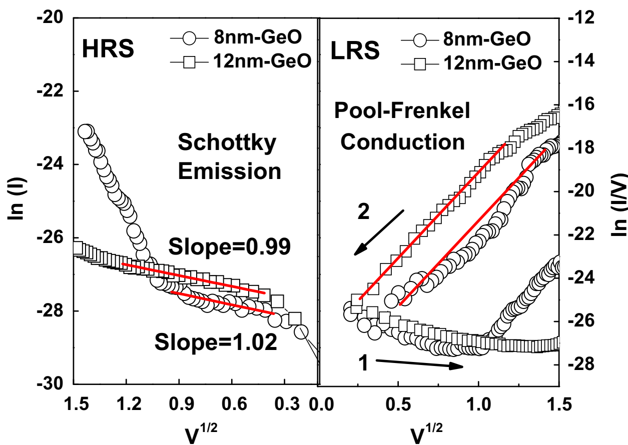

Fig. 2. *I–V* curves of HRS and LRS by fitting with Schottky emission and Poole–Frenkel conduction mechanism, respectively.

trodes. During set, a positive voltage is applied to top Ni and cause a high current flow. Since similar increasing current is also found in SiO_2 MOS capacitors by stress-induced leakage current (SILC) effect, the switching in RRAM may be related to electrons injection from low work-function bottom TaN to create defects and current conduction in GeO_x. This is quite different from the metallic filament switching in metal-oxide RRAM, since no metal exists in GeO_x. The RRAM with thicker 12 nm GeO_x shows a larger resistance window, a close set current of ~0.5 μA by self-compliance, and a much lower reset current of −5.4 pA at −0.68 V. The current variation during self-compliance may be due to electron trapping and de-trapping via GeO_x bulk defects. The dependence of GeO_x thickness on resistance window and set/reset currents indicate that the current conduction is related to bulk defects. In Fig. 1b, we can observe that the set and reset behaviors are dependence of different device sizes. From the device with large area of 31400um^2, the applied voltage of 8 V to form low-resistance state (LRS) is required and then recover to high-resistance state (HRS) by a voltage of −2.5 V which much larger than that of small-area device (11,300 μm^2). Meanwhile, the apparently higher set and reset currents contributed by defect-related size effect explain the importance of defect control in resistive GeO_x device again.

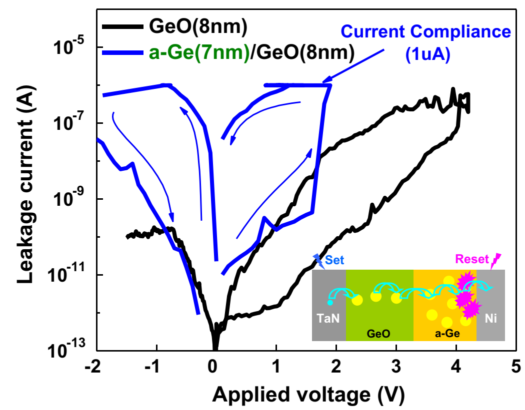

Fig. 3. Swept *I–V* curves of Ni/GeO_2/TaN and Ni/a–Ge/GeO_x/TaN RRAMs.

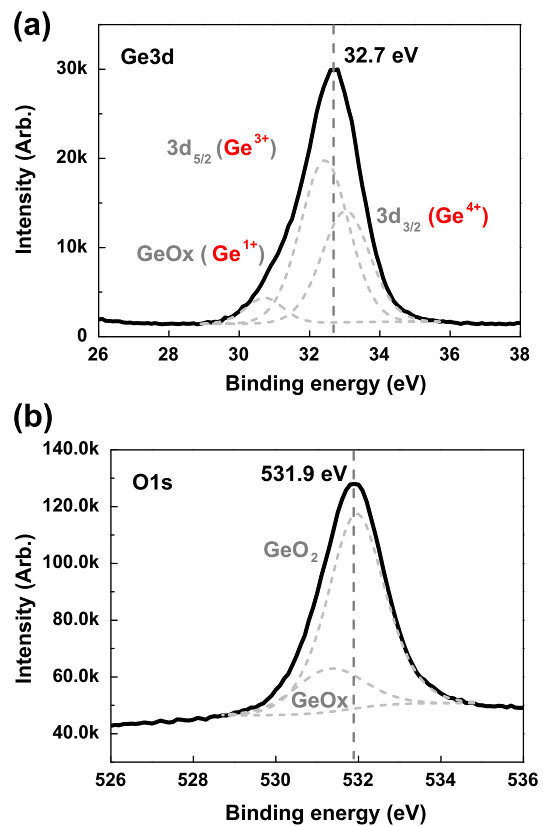

Fig. 4. The XPS spectra of: (a) Ge 3d and (b) O 1s core level in GeO_x.

To understand the resistance switching phenomenon in covalent-bond Ni/GeO_x/TaN RRAM, we have plotted the measured *ln*(*I*) and *ln*(*I*/*V*) as the function of $V^{1/2}$. As shown in Fig. 2, good

matching between measured and simulated data is reached for both HRS and LRS. The current conduction at HRS is governed by Schottky emission that is usually found in low leakage DRAM MIM devices [14]. The current conduction at LRS is ruled by Poole–Frenkel conduction, where the electrons are transported by hopping conduction [15] via defect traps within GeO_x. These traps can be generated by electron injection from low work-function TaN into GeO_x during set process.

To further explore the conduction mechanism, we fabricated the Ni/amorphous-Ge(a-Ge)/GeO_x/TaN RRAM device. The *I–V* switching characteristics and schematic diagram (inset) are shown in Fig. 3. The bilayer a-Ge/GeO_x RRAM exhibits the current-compliance LRS current of 1 μA, small set voltage of 1.6 V and large HRS/LRS ratio of >3 orders of magnitude. However, the current-compliance LRS current is also accompanied by a close reset current, which much larger than that of GeO_x RRAM. The switching mechanism can be supposed that the injected electrons hop via vacancies in a-Ge/GeO_x during set but the hopping paths cannot easily be annihilated by reverse bias current in a-Ge/GeO_x case due to excess vacancies near top Ni electrode. This experiment confirms the importance of unique GeO_x for self-compliance current and ultra-low reset current during set/reset operations.

The defects and chemical states of GeO_x were further examined by X-ray photoelectron spectroscopy (XPS). Fig. 4a and b show the XPS spectra of Ge 3d and O 1s core level in GeO_x film. The Ge 3d spectrum with triple deconvoluted peaks are assigned to the different oxidation state compounds of Ge^{1+}, Ge^{3+} ($3d_{5/2}$) and Ge^{4+} ($3d_{3/2}$), indicating the existence of non-stoichiometric GeO_x and oxygen vacancies in the matrix. Similar oxygen vacancies are also observed by O 1s spectrum with a slight shift of peak to lower binding energy GeO_x. These oxygen vacancies in GeO_x may form conductive paths for electron hopping transport during set operation.

To investigate high-temperature switching behaviors of GeO_x RRAM, the *I–V* characteristic at 100 °C was measured, shown in Fig. 5a. The current-compliance LRS current of 0.1 μA and forward bias of 1.7 V are applied for the set operation. The decreased set voltage and the ultra-low setting energy (0.17 μW) can be ascribed to occurrence of multi-conductive paths for electron hopping at high temperature 100 °C. Furthermore, the hopping paths still can be ruptured by a small reset current of ~8 nA at −0.6 V. The stable set and reset characteristics may be due to the resistance switching controlled by bulk-limited hopping conduction, even at the high temperature of 100 °C. In addition, the bipolar resistance switching also can be indentified by *C–V* curves, shown in Fig. 5b. The different capacitance densities at HRS and LRS explain that the free electrons hop along multiple conductive defects center and then affect interface charges, responsible for *C–V* characteristics [16].

In Fig. 6a, an increasing trend of current is measured for both LRS and HRS states. A still large HRS/LRS resistance window, greater than one order of magnitude, is still obtained at 125 °C. The increasing HRS current with temperature is predicted well by Schottky emission mechanism [14] with higher thermal energy to overcome the Schottky barrier. The increasing LRS current with increasing temperature shows a negative temperature coefficient that is opposite to the metallic filament conduction in metal-oxide RRAM [3]. Such negative temperature coefficient was found previously in highly defective Silicon (Si) via hopping conduction mechanism [15]. Fig. 6b shows the retention characteristics of Ni/GeO_x/TaN RRAM at elevated temperature of 85 °C. Stable HRS/LRS memory window is measured with retention time to 9×10^3 s.

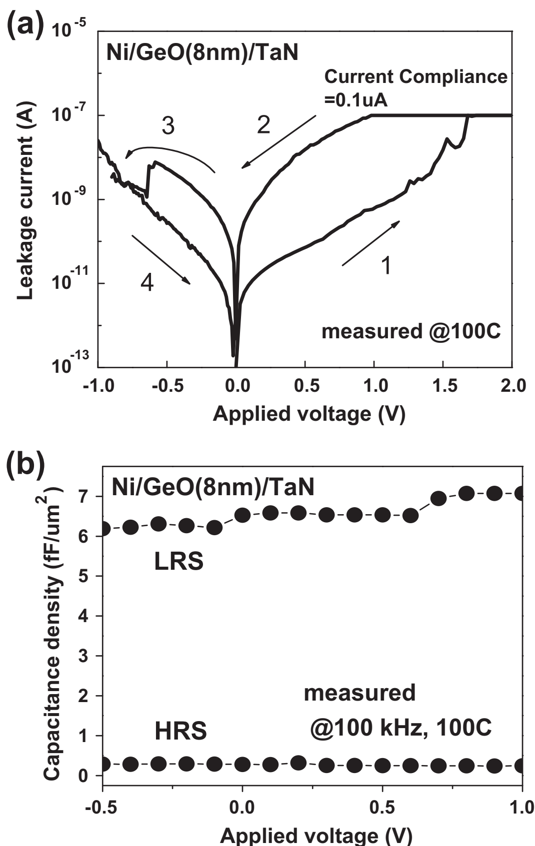

Fig. 5. (a) Swept *I–V* and (b) *C–V* characteristics of Ni/GeO_x/TaN RRAM, measured at 100 °C.

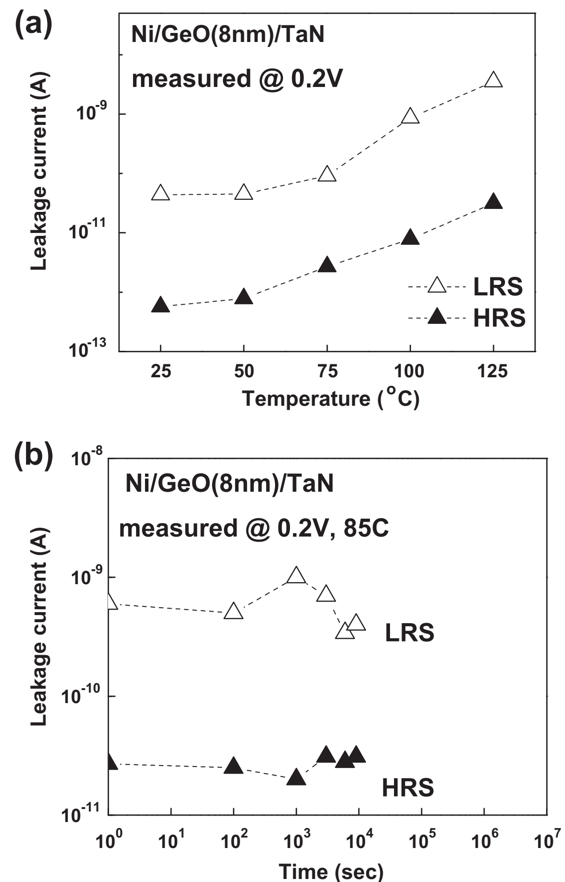

Fig. 6. (a) The temperature dependence of HRS/LRS and (b) 85 °C retention characteristics of Ni/GeO_x/TaN RRAM.

4. Conclusions

We have demonstrated an ultra-low power and cost-effective Ni/GeO_x/TaN RRAM. The low current at LRS is ruled by Poole–Frenkel conduction with electrons hopping via defect traps, which is also responsible for the low self-compliance current. This covalent-bond GeO_x as a host film or stacked layer should have the potential for future RRAM NVM application.

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