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Citation: Applied Physics Letters **102**, 062905 (2013); doi: 10.1063/1.4792316
View online: http://dx.doi.org/10.1063/1.4792316
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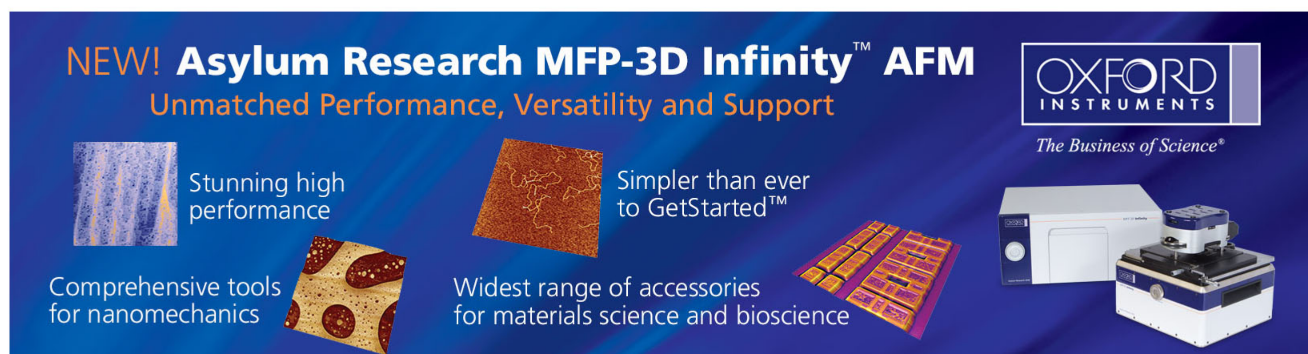

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Multilevel resistive switching memory with amorphous InGaZnO-based thin film

Ching-Hui Hsu,[1] Yang-Shun Fan,[2] and Po-Tsun Liu[1,a)]
[1]*Department of Photonics and Display Institute, National Chiao Tung University, 1001 Ta-Hsueh Rd., HsinChu 300, Taiwan*
[2]*Department of Photonics and Institute of Electro-Optical Engineering, National Chiao Tung University, 1001 Ta-Hsueh Rd., HsinChu 300, Taiwan*

(Received 28 November 2012; accepted 1 February 2013; published online 13 February 2013)

Multi-level storage capability of resistive random access memory (RRAM) using amorphous indium-gallium-zinc-oxide (InGaZnO) thin film is demonstrated by the TiN/Ti/InGaZnO/Pt device structure under different operation modes. The distinct four-level resistance states can be obtained by varying either the trigger voltage pulse or the compliance current. In addition, the RRAM devices exhibit superior characteristics of programming/erasing endurance and data retention for the application of multi-level nonvolatile memory technology. Physical transport mechanisms for the multi-level resistive switching characteristics are also deduced in this study. © *2013 American Institute of Physics*. [http://dx.doi.org/10.1063/1.4792316]

Nowadays, the prevailing and commercialized non-volatile memory (NVM) is FLASH memory. However, it is generally believed that the conventional FLASH memory is approaching its scaling limit. Metal oxide-based resistive random access memory (RRAM) is one of the competitive candidates for future NVM applications, owing to its simple structure, high storage density, low power consumption as well as fast switching operation.[1–3] Amorphous InGaZnO (a-IGZO) based RRAM devices have shown remarkable resistance switching characteristics.[4,5] Furthermore, using a-IGZO film for non-volatile memory devices is promising to be integrated with a-IGZO thin film transistor (TFT) periphery circuits in active-matrix flat panel displays (AMFPDs) to achieve system-on-panel (SoP) applications.[6,7] On the other hand, with the growing demands for high-capacity memory in electronic products, the capability of storing multiple bits in one device has become a significant criterion. The multi-level cell (MLC) could enhance the storage density, which means that the memory can store more data in a finite space.[8] In this work, the switching characteristics of RRAM device with TiN/Ti/IGZO/Pt structure were investigated, with the emphasis on multilevel memory application. The 4-state (2-bit) cell has been achieved by either controlling the compliance current (I_{cc}) or by varying the amplitude of the voltage pulses. We have confirmed that by varying the amplitude of 50 ns voltage pulses, the memory can be programmed to various distinguishable states.

RRAM devices with TiN/Ti/IGZO/Pt structures were fabricated at room temperature. The process sequence was as follows. First, the TiO_2 adhesion layer and the Pt bottom electrode were deposited on a SiO_2/Si substrate by electron-beam (e-beam) thermal evaporation. It was followed that a 40 nm-thick a-IGZO film was deposited by magnetron sputtering system and patterned by shadow masks with a diameter of 100 μm. Finally, a 10 nm-thick Ti film acting as oxygen-gettering layer followed by a 70 nm-thick TiN top electrode were deposited sequentially by the sputtering system. The electrical measurements were performed with Keithley 4200 semiconductor characterization analyzer and a dual-channel pulse generator card. Voltage bias was applied on the TiN top electrode and the Pt bottom electrode was grounded.

Figure 1 shows that the depth profile of X-ray photoelectron spectroscopy (XPS) for the TiN/Ti/IGZO/Pt multi-stack structure, and the inset depicts its cross-sectional transmission electron microscopy (TEM) image. It clearly appears that an interfacial layer (~2 nm) existed between the Ti layer and the IGZO from the TEM image, and confirmed to be composed of TiO_x by the XPS analysis. With this oxygen reservoir of TiO_x, the formation of oxygen-vacancy on the a-IGZO surface will be beneficial for further improvement in electrical switching performance of the a-IGZO-based RRAM device.[9,10]

The TiN/Ti/IGZO/Pt device exhibited a typical bipolar resistive switching characteristic, and can be characterized

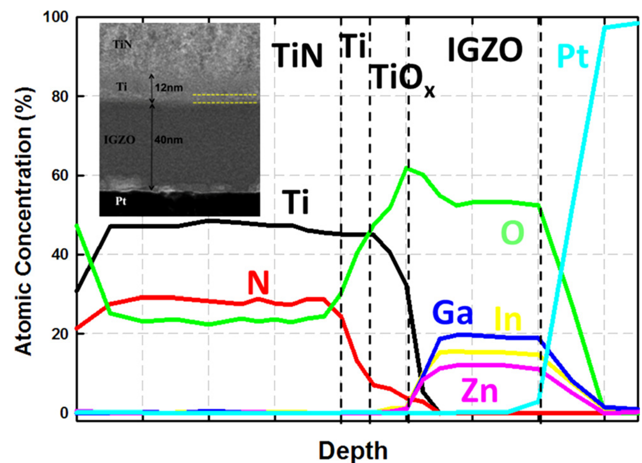

FIG. 1. XPS depth profile of the TiN/Ti/IGZO/Pt device. The inset shows the cross-sectional TEM image of the TiN/Ti/IGZO/Pt device.

a)Author to whom correspondence should be addressed. Electronic mail: ptliu@mail.nctu.edu.tw. Tel.: 886-3-5712121 ext. 52994. Fax: 886-3-5735601.

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with different compliance currents during the set process, as shown in Fig. 2. The set process was observed at positive voltages, while the reset process was observed at negative voltages. The resistance states can be controlled by properly setting the I_{cc} in the set process. Obviously, the higher the I_{cc} imposed on the device, the lower resistance value of ON-state could be reached. Four states can be clearly distinguished and the distributions of these four states are depicted in the inset of Fig. 2. These results demonstrated the promising application for multi-bit storage memory technology. Figure 3(a) shows the endurance of RRAM device under different compliance currents of 10 mA, 0.8 mA, and 0.2 mA, respectively, for 50 cycles. The resistances were monitored at 0.5 V. Under the I_{cc} of 10 mA, 0.8 mA, and 0.2 mA, the resistance of ON-state is called level 1, level 2, and level 3, respectively; and the resistance of the OFF-state is denoted as level 4. A sufficient margin of resistance ratio can be observed even after set/reset cycling stress tests. The smallest resistance window in this work is around 3.5, and these margins between each two different resistive levels are sufficient for circuit design.[11–13] In addition, the retention characteristics of these 4 states were demonstrated in Fig. 3(b). It indicated that each memory state was maintained stably and no degradation over 1000 s.

Considering the realistic operation for memory array application, electric-pulse-induced resistance (EPIR) switching test was also carried out on the RRAM device, as shown in Fig. 4. By controlling the amplitude of the set voltage pulses, three distinct lower resistance states can be produced (level 1, level 2, and level 3). Different positive voltage pulses of 1 V, 1.5 V, and 2.5 V with pulse width of 50 ns were applied to set the RRAM device into different ON-states. The reset operation was achieved by applying negative voltage pulse of -1.5 V with pulse width of 1 μs, and the resistance state of level 4 was produced. Both of the SET and RESET voltages are less than 3 V, exhibiting the benefit of low-voltage operation feature.

The physical transport mechanism for the resistive switching characteristics also was studied and deduced as follows. It is known that oxygen vacancies exist in the IGZO thin film naturally.[14,15] After the forming process, more oxygen vacancies in the IGZO layer were produced to activate

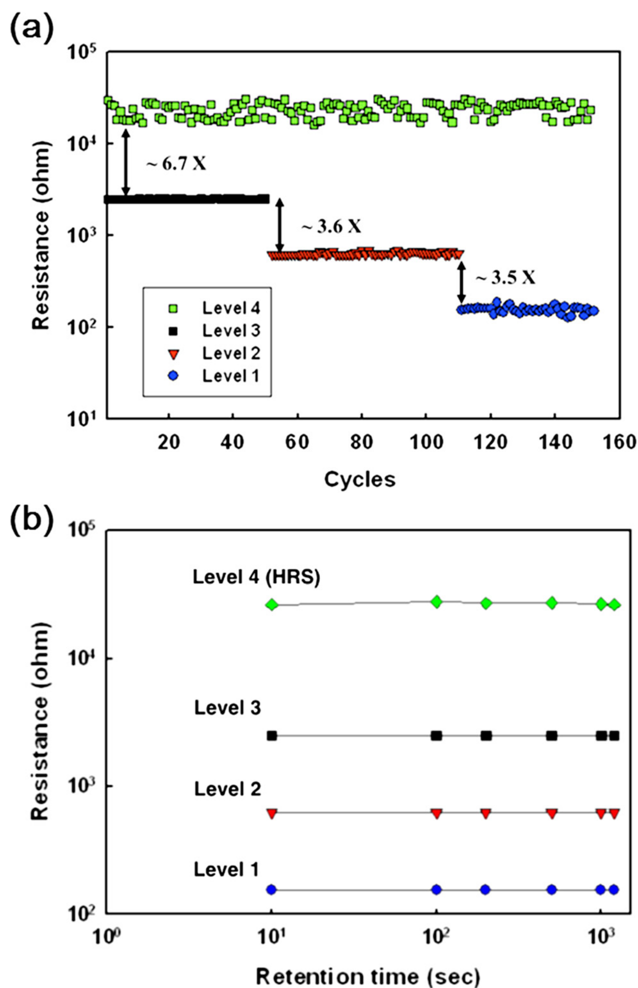

FIG. 3. (a) The resistances of the TiN/Ti/IGZO/Pt RRAM device over 150 cycles with different compliance currents. The smallest resistance window is around 3.5. (b) The retention characteristics of different resistance states for the TiN/Ti/IGZO/Pt RRAM device.

the resistance switching. When positive bias was applied on the TiN top electrode, the negatively charged oxygen ions would move to the Ti layer, and then oxidized at the anode, while the oxygen vacancies (metal ions) reduced at the cathode. Many localized conducing filaments were formed in the IGZO film, resulting to the lower resistance states. The positive resistance temperature coefficient of 4.67×10^{-3} K^{-1} for the RRAM device has been obtained in this work by

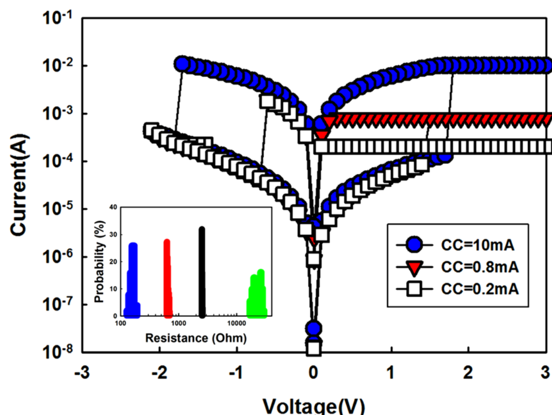

FIG. 2. The I-V curves of a IGZO RRAM device under different compliance currents of 0.2 mA, 0.8 mA, and 10 mA. The inset is the resistance distribution of different levels.

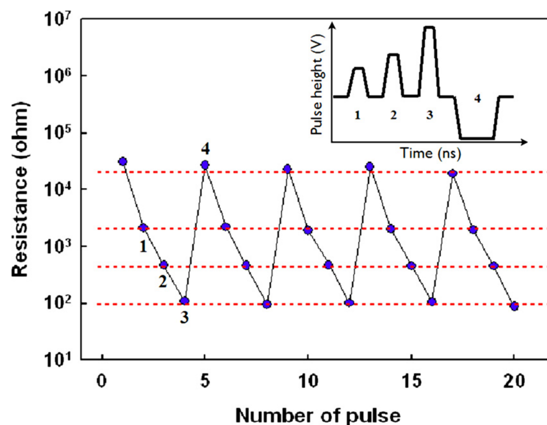

FIG. 4. EPIR switch testing on the TiN/Ti/IGZO/Pt RRAM device.

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variable temperature measurement. This can confirm the metallic filament conduction behavior occurred in the IGZO-based RRAM, which means that these conductive filaments may be composed of metal atoms. The formation and rupture of the conducting filaments were mainly due to the electrochemical migration of oxygen ions and oxygen vacancies, and thereby the bipolar switching behavior was observed. In addition, the intermediate ON-states might be the results of partial formation of tiny conducting filaments. The edges of thin filaments may have been oxidized by the small amount of oxygen, existed inside the filaments or their circumferences.[16] As a result, the degree of the filaments' formation led to the multi-level operation characteristics in the RRAM device.

In summary, we proposed the RRAM device with TiN/Ti/IGZO/Pt capacitor structure and demonstrated the stable MLC operation of 2-bits/cell by either varying the voltages of 50 ns pulses or controlling the compliance current. The benefit of MLC storage can further increase the memory capacity. Sufficient sensing margin for these 4 resistance states can also be observed in the RRAM device. The results indicated that the use of IGZO RRAM is promising for the MLC application in the next generation non-volatile memory. Also, its application to FPDs is beneficial for the integration with the transparent IGZO TFTs in SoP technology architecture.

The authors would like to thank the National Science Council of the Republic of China, Taiwan for financially supporting this research work under Contract No. NSC 100-2628-E-009-016-MY3.

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