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Performance Evaluation of InGaSb/AlSb P-Channel High-Hole-Mobility Transistor Faricated Using BCl$_3$ Dry Etching

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In this study, we present the fabrication and characterization of InGaSb/AlSb p-channel high-hole-mobility-transistor devices using inductively coupled plasma (ICP) etching with BCl$_3$ gas. Devices fabricated by the dry etching technique show good DC and RF performances. Radio-frequency (RF) performance for devices with different source-to-drain spacing (L_{SD}) and gate length (L_g) were investigated. The fabricated 80-nm-gate-length p-channel device with 2-µm L_{SD} exhibited a maximum drain current of 86.2 mA/mm with peak transconductance (g_m) of 64.5 mS/mm. The current gain cutoff frequency (f_T) was measured to be 15.8 GHz when the device was biased at $V_{DS} = -1.2$ V and $V_{GS} = 0.4$ V.

The III–V compound semiconductor quantum-well field effect transistors (QWFET) have attracted more attention as a substitution of the Si channel for advanced high-speed and low-power logic applications owing to the well-known characteristics of high electron mobility, high peak velocity and low effective mass.[1)] With the success in the development of III–V n-channel QWETs for low-power and high-speed logic applications,[2–4)] the development of p-type counterpart becomes an important issue to complete the complementary circuit technology.[5)] For this purpose, the In$_x$Ga$_{1-x}$Sb alloy system shows great potential since the GaSb and InSb materials have the highest bulk hole mobilities in III–V compounds. Besides, the significant valence band barrier for such alloy enables good quantum confinement.[6,7)] Application of the compressive strain to the In$_x$Ga$_{1-x}$Sb layer has been demonstrated to enhance the hole mobility due to band splitting in Si and SiGe p-MOSFETs.[8)]

Hole mobility at room temperature up to 1200 cm^2 V^{-1} s^{-1} through strained In$_x$Ga$_{1-x}$Sb/AlSb quantum well with optimum growth condition of epitaxial materials leading to good RF performance has been demonstrated.[9)] In this study, we investigate the effect of source-to-drain spacing (L_{SD}) and gate length (L_g) on the RF performance of the device. We observed an increase of 19% in the current-gain-cutoff-frequency (f_T) with fixed L_g when L_{SD} was reduced from 3 to 2 µm. On the other hand, with fixed L_{SD}, 28% increase in f_T was obtained when L_g was scaled down from 200 to 80 nm. The 80-nm gate-length device with 2-µm L_{SD} exhibited a measured f_T of 15.1 GHz when the device was biased at $V_{DS} = -1.2$ V and $V_{GS} = 0.4$ V.

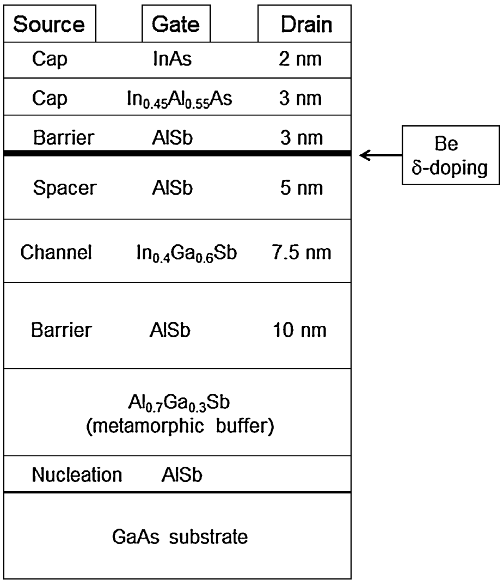

Fig. 1. Epitaxial structure of the InGaSb/AlSb p-channel quantum-well field effect transistors.

Figure 1 shows the epitaxial structure of the InGaSb p-channel QWFET. The InGaSb/Alsb heterostructure was grown on a semi-insulating 3-in. (001) GaAs substrate by solid-source molecular beam epitaxy (MBE). The AlSb/Al$_{0.7}$Ga$_{0.3}$Sb composite buffer layer was used to accommodate the lattice mismatch between substrate and channel layer. The biaxial compressive strain was formed by the AlSb/Al$_{0.7}$Ga$_{0.3}$Sb barrier layers. Modulation doping of $\sim 1 \times 10^{12}$ is achieved using planar Be-doped layer on top of the AlSb layer in order to increase the hole concentration. To enhance the hole mobility, the biaxial compressive strain provided by a lattice mismatch of approximately 1.8% between the AlSb/Al$_{0.7}$Ga$_{0.3}$Sb and the In$_{0.4}$Ga$_{0.6}$Sb channel layer was applied. The In$_{0.45}$Al$_{0.55}$As and InAs layers were capped to prevent air exposure and provide a chemically stable surface layer. Hall measurements exhibited a hole carrier concentration of 1.42×10^{12} cm^{-2} and a hole mobility of 895 cm^2 V^{-1} s^{-1}.

For device fabrication, mesa isolation was carried out by inductively coupled plasma (ICP) process using BCl$_3$ gas and the dry etching was stopped at Al$_{0.7}$Ga$_{0.3}$Sb buffer layer. Compared to Cl$_2$-based gases, adoption of BCl$_3$ gas in the dry etching process will lead to a well-controllable etching rate to obtain shallow mesa isolation. Detailed discussions can be found in our earlier work[10)] Pd/Pt/Au ohmic contacts were evaporated and subsequently annealed at 340 °C for 30 s in N$_2$ ambient, resulting in a low contact resistance of 1.81 Ω mm and a sheet resistance of 1371 Ω/sq. The Ti/Pt/Au metal-line gate was formed by E-beam lithography and lift-off techniques. Finally, a 100-nm-thick SiN$_x$ passivation layer was deposit by plasma-enhanced chemical vapor deposition (PECVD) to protect the devices.

Figure 2 shows the drain–source current (I_{DS}) as a function of drain–source voltage (V_{DS}) with gate–source

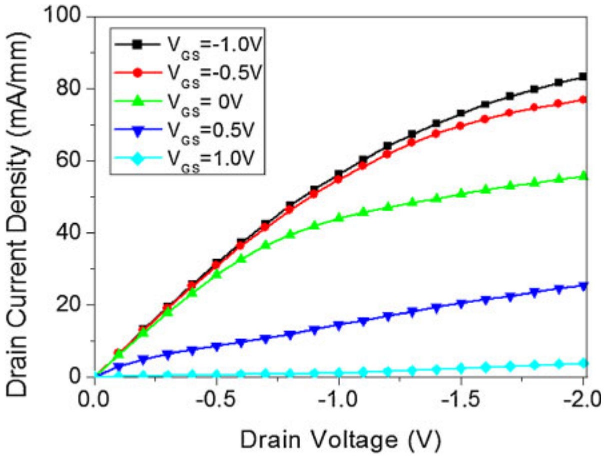

Fig. 2. (Color online) Drain–source current (I_{DS}) as a function of drain–source voltage (V_{DS}) with gate–source voltage (V_{GS}) varied from -1 to 1 V for the 80-nm-gate and 2 × 50-μm^2-width device.

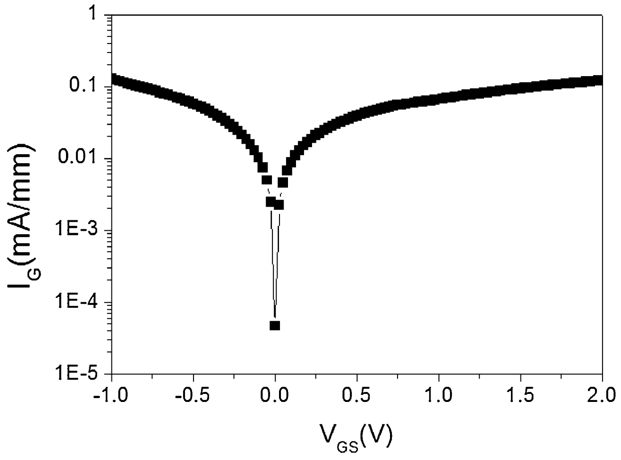

Fig. 4. The Schottky gate leakage as a function of gate bias for the 80-nm-gate and 2 × 50-μm^2-width device.

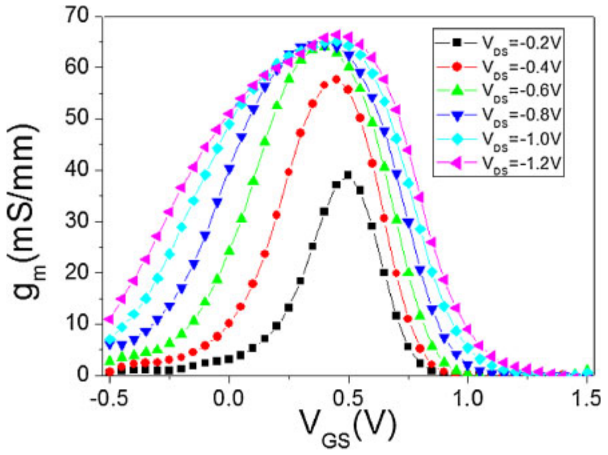

Fig. 3. (Color online) The DC transconductance (g_m) as a function of gate bias at different V_{DS} for the 80-nm-gate and 2 × 50-μm^2-width device.

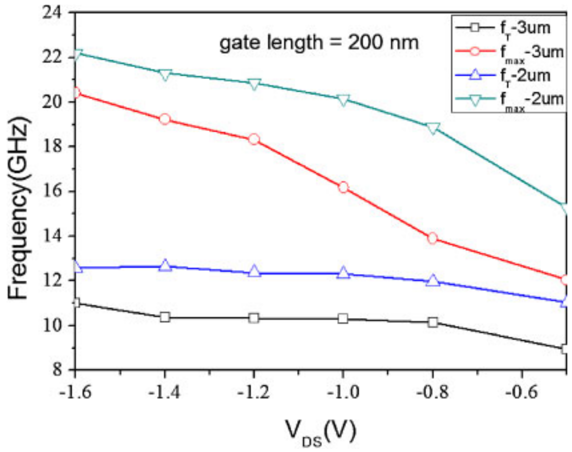

Fig. 5. (Color online) f_T and f_{max} as a function of drain voltage for the 200-nm 2 × 50-μm^2-width device with different source–drain spacing.

voltage (V_{GS}) varied from -1 to 1 V for the 80-nm-gate and 2 × 50-μm^2-width device. The device exhibits a maximum drain current density of 86.2 mA/mm at a gate bias of -1 V and a drain bias of -2 V. Figure 3 shows the DC transconductance (g_m) as a function of gate bias at different V_{DS} for the same device. A peak g_m of 64.5 mS/mm is observed, which is about 8% higher than that of the 200-nm device. The subthreshold slope of the device at $V_{DS} = -1.2$ V was extracted to be 106 mV/dec. The corresponding Schottky gate leakage as a function of gate bias for the same device is shown in Fig. 4.

The high-frequency performance of the device was characterized through *S*-parameter measurement over a frequency range of 1 to 80 GHz using an HP 8510 XF vector network analyzer. Standard load–reflection–reflection–match (LRRM) calibration procedure was performed before measurement. The extrinsic current-gain cutoff frequency (f_T) and maximum oscillation frequency (f_{max}) were extracted from measurement based on the usual -6 dB/octave slope. The 80-nm device with 2-μm L_{SD} exhibited f_T and f_{max} of 15.8 and 29.2 GHz at $V_{DS} = -1.2$ V, respectively. These results demonstrate the feasibility of BCl$_3$ dry etching for shallow mesa formation in InGaSb p-channel QWFET fabrication.

f_T and f_{max} as a function of drain voltage for the 200-nm 2 × 50-μm^2-width device with different source–drain spacing is shown in Fig. 5. The gate was biased at peak g_m for all the cases. An increase of 19% in f_T is observed when L_{SD} was reduced from 3 to 2 μm. Figure 6 shows the cases for the 2 × 50-μm^2-width device with different gate length when L_{SD} was fixed at 2 μm. We observe an increase of 28.3% in f_T when the gate length was scaled from 200 to 80 nm. Apparently, gate-length scaling is much more effective in boosting f_T. Such increase is almost comparable to the boost in f_T due to the increase of hole mobility.[1,8] From Figs. 5 and 6, we also observe that the variation of f_T with respect to the drain bias is not as drastic as that of f_{max}.

In conclusion, we have successfully fabricated p-channel QWFET device and characterized its performance. The effect of different source–drain spacing and gate-length on the RF performance was investigated. It is concluded that gate-length scaling is more effective than reduction of

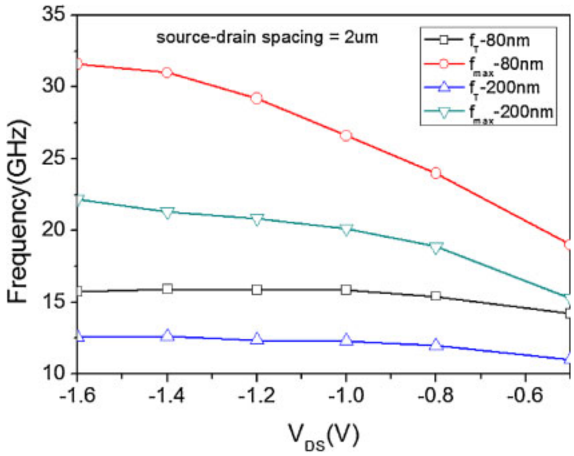

Fig. 6. (Color online) f_T and f_{max} as a function of drain voltage for the 2×50-μm^2-width device with different gate length when L_{SD} was fixed at 2 μm.

source–drain spacing. Further boost in the RF performance should be possible with device techniques such as T-shaped gate implementation, reduction of gate-to-channel distance and reduction of parasitics.

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