Design of Bidirectional and Low Power Consumption Gate Driver in Amorphous Silicon Technology for TFT-LCD Application

Guang-Ting Zheng, Po-Tsun Liu, *Senior Member, IEEE*, Meng-Chyi Wu, *Senior Member, IEEE*, Li-Wei Chu, *Member, IEEE*, and Meng-Chuan Yang

***Abstract*—A new gate driver has been designed and fabricated by amorphous silicon (a-Si) technology. With utilizing four clock signals in the design of gate driver on array (GOA), the pull-up transistor has ability for both output charging and discharging, and layout size of the proposed gate driver can be narrowed for bezel panel application. Moreover, lower duty cycle of clock signals can decrease static power loss to further reduce the overall power consumption of the proposed gate driver. The scan direction of the proposed gate driver can be adjusted by switching two direct control signals to present the reversal display of image. The proposed gate driver has been successfully demonstrated in a 4.5-inch WVGA (480 × RGB × 800) TFT-LCD panel and passed reliability tests of the supporting foundry.**

***Index Terms*—Amorphous silicon (a-Si), gate driver, thin-film transistor liquid crystal display (TFT-LCD).**

I. Introduction

IN RECENT YEARS, a variety of portable electronic devices have been introduced with small displays such as cellular phone and PDA (Personal Digital Assistants). Displays for portable electronic devices require high resolution, light-weight, and low power consumption. Therefore, the integrated gate driver using amorphous silicon (a-Si) technology for the TFT-LCD has become the main stream due to the mature manufacturing, low-cost processing, and elimination of the gate driver ICs [1]–[12]. Nevertheless, design of the integrated gate driver by a-Si encounters three main challenges which are the low field-effect mobility, low reliability issue under high voltage stress, and the lack of P-type transistor. In order to alleviate the low mobility restriction, the thousands micro-meter width of the main driving TFT is required to drive the gate line of the panel. But the large parasitic capacitance affects the performance of circuit. In addition, the reliability issue of the integrated gate driver is as well as a notable challenge. While a-Si TFT suffers the DC-bias shift which results from charge trapping and defect creation leads to shorten the life time of the integrated driver [13]–[17]. Besides, the structure of a-Si gate driver using only N-type transistor increase the difficulty of design for panel application.

So far, a-Si integrated gate driver was originated from Thomson's shifter register which was made up of four transistors and one capacitor merely [2], [3], and many methods have been developed to improve the circuit [5]–[8]. For the prior arts, the circuit style of diode connection degrades the output rise time due to the threshold voltage drop on gate voltage of pull-up transistor, hence the before work [18] proposed a high rising time gate driver with a threshold voltage drop cancellation technique that decreases output rise time by 24.6% for high resolution display application. However, the switching times of clock signals (Clk and XClk) with 50% duty cycle and large size of pull-up and pull-down transistors in before work caused high power consumption.

Besides, Chun *et al.* [19] developed the bidirectional gate driver circuit with a-Si:H technology to change direction of vertical scan depending on the polarity of two control signals. Furthermore, Lin *et al.* [20] proposed a bidirectional gate driver circuit using the carrier buffer TFT to select the direction of transfer and does not suffer from the shift in the threshold voltage.

In this work, the pull-up transistor is designed to has ability for both output charging and discharging with low duty cycle (25%) clock signals in proposed gate driver circuit, and the parasitic capacitances and layout size of gate driver are be narrowed for bezel panel application. Moreover, lower duty cycle of clock signals can decrease static power loss to further reduce the overall power consumption of the proposed gate driver. Besides, high performance bidirectional gate driver circuit is designed by simply switching two direct controlling signals with size reducing. The reversal display of image can easily be presented in proposed gate driver by only exchanging the polarity of control signals.

II. Operation of the Proposed Integrated Gate Driver

A. Proposed Integrated Gate Driver for Single Direction Scanning

The block diagram of the proposed low power integrated gate driver circuit is shown in Fig. 1(a), which is composed of the

Manuscript received May 31, 2012; revised August 05, 2012; accepted October 09, 2012. Date of publication January 14, 2013; date of current version February 11, 2013. This work was supported by Giantplus Technology Corporation, Taiwan, and supported in part by the National Science Council, Taiwan, under Contract NSC 100-2628-E-009-016-MY3.

G.-T. Zheng and M.-C. Wu are with the Department of Electronics & Engineering Institute, National Tsing-Hua University, Hsinchu 30078, Taiwan (e-mail: andygk2@hotmail.com; mcwu@ee.nthu.edu.tw).

P.-T. Liu is with the Department of Photonics & Display Institute, National Chiao-Tung University, Hsinchu 30078, Taiwan (e-mail: ptliu@mail.nctu.edu.tw).

L.-W. Chu and M.-C. Yang are with the Department of Photonics & Display Institute, National Chiao-Tung University, Hsinchu 30078, Taiwan (e-mail: bambool.eo95g@nctu.edu.tw; b943011028@student.nsysu.edu.tw).

Color versions of one or more of the figures are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/JDT.2012.2225406

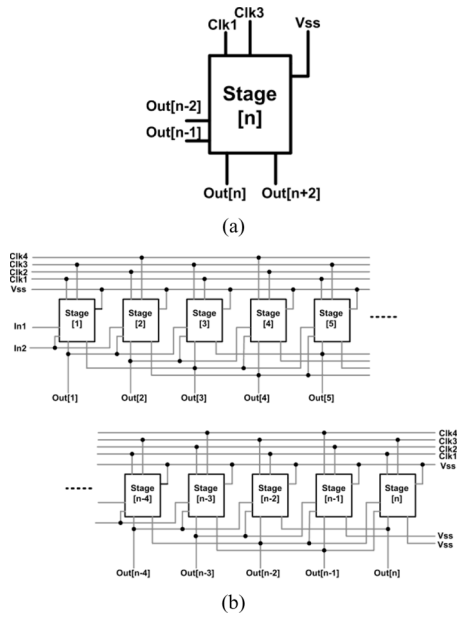


Fig. 1. (a) Block diagram and (b) connections between stages of the proposed circuit for TFT-LCD application.

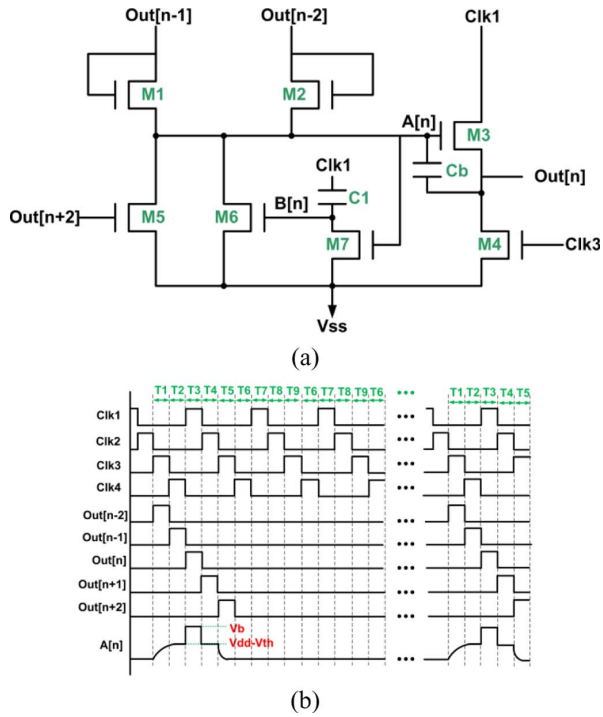


Fig. 2. (a) Schematic and (b) corresponding operation waveforms of proposed circuit.

input signals ($\mathrm{Out}[n-2]$ and $\mathrm{Out}[n-1]$), control signals (Clk1 and Clk3), feedback signal ($\mathrm{Out}[n+2]$), and output signal ($\mathrm{Out}[n]$). Fig. 1(b) depicts the connections among the proposed low power integrated gate driver circuit stages for TFT-LCD application. The block manipulation is activated while start signals (In1 and In2) input a high voltage level to $\mathrm{Stage}[1]$. A pulse signal is subsequently generated at $\mathrm{Out}[1]$ and being acted as one of start signals for $\mathrm{Stage}[2]$. Accordingly, sequential pulse signal can be periodically transferred stage by stage for feeding the whole gate lines of the pixel array in TFT-LCD.

Fig. 2(a) presents the schematic diagram of the proposed low power integrated gate driver with its corresponding waveforms in Fig. 2(b). The high and low voltage levels in Fig. 2(b) are defined as Vdd and Vss, respectively. Moreover, for the proposed circuit, the four clock signals have different phases and the duty of each clock signal is 25%. The operation can be divided into nine periods noted from T1 to T9. In the T1 period that Clk3 is high, M2, and M4 are turned on by Out[n-2] and Clk3. The other transistors are turned off. At this moment, $\mathrm{Out}[n]$ is Vss through M4 and $A[n]$ is charged by M2. Next, in the T2 period, only M1 is turned on and others are turned off. The $A[n]$ is charger higher due to the second time charging. At the meanwhile, the $\mathrm{Out}[n]$ is still connects to Vss because of the on state of M3. After two periods of charging at $A[n]$, the final voltage is completely charge to Vdd-Vth.

In the T3 period, M1, M2, M4, and M5 are turned off by $\mathrm{Out}[n-1]$, $\mathrm{Out}[n-2]$, Clk3, and $\mathrm{Out}[n+2]$. Clk1 becomes high voltage level and then $\mathrm{Out}[n]$ is charged by M3. At this moment, $A[n]$ is boosted through Cb from Vdd-Vth to a higher voltage level which is labeled as Vb in Fig. 2(b). The high $A[n]$ provides M3 charging $\mathrm{Out}[n]$ with large current which is relative to the width of M3 as well. On the other hand, M6 turns on slightly at the transient of Clk1 from Vss to Vdd. However, this turn on process is swift and turned off immediately because of M7 connects to high voltage ($A[n]$) previously.

In the T4 period, all the TFTs and voltages maintain their last state except the $\mathrm{Out}[n]$ discharges because Clk1 is low in this period as well as $A[n]$ decreases to Vdd-Vth caused by coupling from the capacitor Cb. In other words, M3 is the main role for charging and discharging as shown in Fig. 3, the width of M4 is narrowed and the layout of the proposed gate driver can be constructed with miniature size. Then, in T5 period, M4 and M5 are turned on by Clk3 and $\mathrm{Out}[n+2]$. Others keep at off states and $A[n]$ is discharged to Vss an $\mathrm{Out}[n]$ is maintaining at Vss because of M4. Although the discharge capacity of M5 is not strong enough, the speed of discharge doesn't influence the operation because Clk1 is at low voltage which is connected to $\mathrm{Out}[n]$ while $A[n]$ is at high voltage. The steps of delivering a gate line pulse at $\mathrm{Stage}[n]$ complete the remaining operation periods are used for the noise immunity.

In T6 period, the $\mathrm{Stage}[n]$ is stationary, $A[n]$ and $\mathrm{Out}[n]$ are kept at low voltage. Next period, T7, which Clk1 is high and results in noise, the $A[n]$ is coupled by Clk1 through parasitic capacitances and results in charging at $\mathrm{Out}[n]$. At meanwhile, M6 is used for eliminating the noise at $A[n]$. The Clk1 couples through C1, which is large enough to get high couple voltage at $B[n]$, and M6 is turned on by $B[n]$ so as to discharge the disturbance at $A[n]$.

In the T8 period, the Clk1 transits from high to low voltage level at the beginning of this period. The variation is coupled to $A[n]$ and affects $\mathrm{Out}[n]$, this makes voltages of $A[n]$ and $\mathrm{Out}[n]$ become slightly negative. Finally, in T9 period, M4 is turned on by Clk3 and then connects $\mathrm{Out}[n]$ with Vss, that is, make sure $\mathrm{Out}[n]$ is stable at low voltage level. Successively, the following periods replicate the steps from T6 to T9 orderly until the next start signals (In1 and In2) come up.

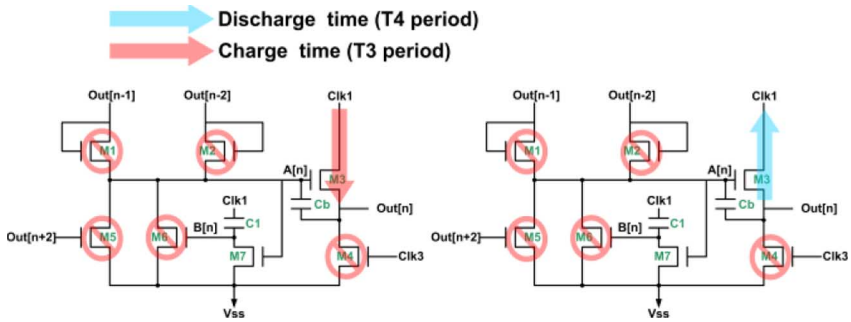


Fig. 3. Charge and discharge path by M3 for proposed circuit.

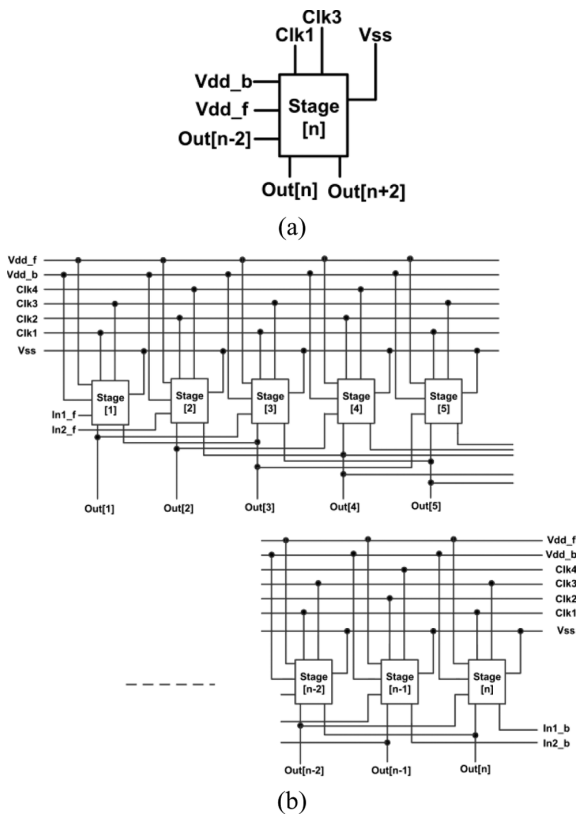


Fig. 4. (a) Block diagram and (b) connections between the stages of the proposed bidirectional gate drivers for TFT-LCD application.

B. Proposed Integrated Gate Driver for Bidirectional Scanning

The block diagram of the bidirectional gate driver is shown in Fig. 4(a), which is composed of one input signals ($\mathrm{Out}[n-2]$), control signals (Clk1, Clk3, Vdd_f and Vdd_b), feedback signals ($\mathrm{Out}[n+2]$), and output signals ($\mathrm{Out}[n]$). Fig. 4(b) depicts the connections of the driver blocks. For the forward scan direction, the block manipulation is activated while two start signals (In1_f and In2_f) input a high voltage level to $\mathrm{Stage}[1]$ and $\mathrm{Stage}[2]$. A pulse signal is subsequently generated at $\mathrm{Out}[1]$ and being acted as the start signal for $\mathrm{Stage}[2]$. Accordingly, sequential pulse signal can be periodically transferred stage by stage for feeding the whole gate lines of the pixel array in TFT-LCD. On the other hand, for the backward scanning, the start signals (In1_b and In2_b) are the impetus of the panel operation

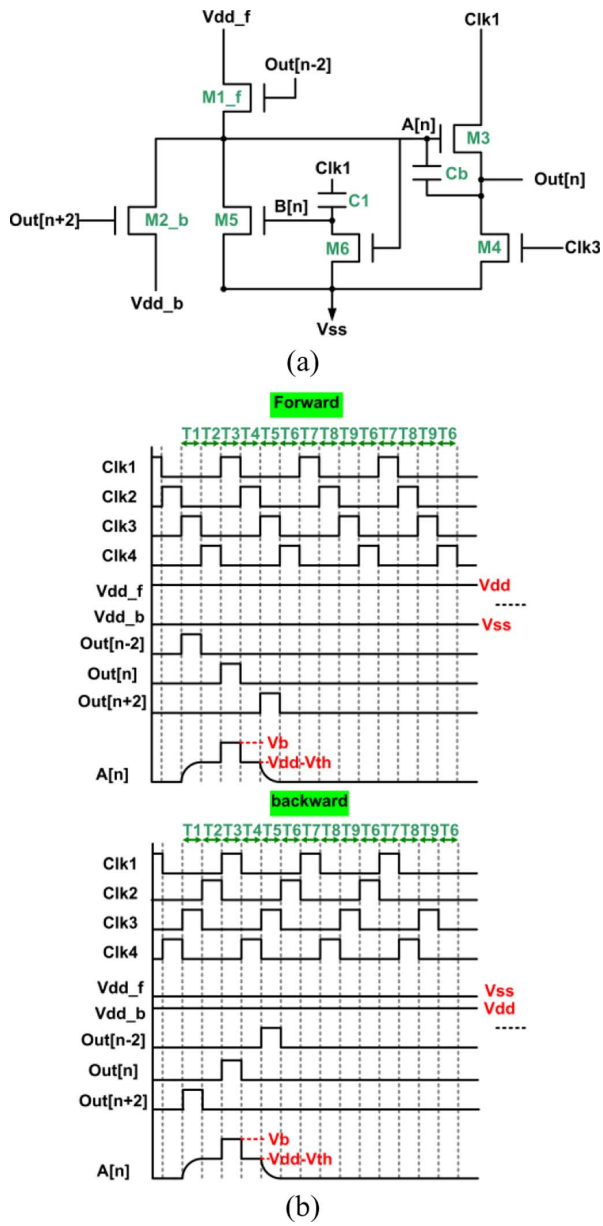


Fig. 5. (a) Schematic and (b) corresponding operation waveforms of bidirectional gate driver circuit.

at $\mathrm{Stage}[n]$ that is the last stage of the gate driver circuit. The $\mathrm{Out}[n]$ is the initiative signal of $\mathrm{Stage}[n-1]$, and then the gate pulse appear at $\mathrm{Out}[n-1]$. Repeatedly, the operation among

TABLE I
DEVICE PARAMETERS OF THE PROPOSED INTEGRATED GATE DRIVER

TFT aspect ratio W/L (μm/μm) (proposed gate driver circuit)			
M1	300/3	M5	100/3
M2	300/3	M6	100/3
M3	3000/3	M7	100/3
M4	300/3		
(proposed bidirectional gate driver circuit)			
M1_f	300/3	M4	300/3
M2_b	300/3	M6	100/3
M3	3000/3	M7	100/3
Capacitance (pF)			
C1	2	Cb	3

blocks is the same as the forward direction. The only difference is the opposite of the order of gate pulses.

Fig. 5(a) presents the schematic diagram of bidirectional gate driver circuit with its corresponding waveforms in Fig. 5(b). The high and low voltage levels in Fig. 5(b) are defined as Vdd and Vss, respectively. The operation of bidirectional gate driver circuit is similar to the original proposed circuit.

For forward scanning, the Vdd_f and Vdd_b are connected to Vdd and Vss, respectively. And the operation steps can be divided into nine periods, noted from T1 to T9. The T1 to T9 periods are the same as mentioned in Fig. 2 except the lack of M1. For the backward direction, the sequences of clock signals have been adjusted and the voltage level of Vdd_f and Vdd_b has to be exchanged. The operation is similar to forward direction where M2_b is used to charge the capacitor (Cb) in order to set node $A[n]$ to high voltage level, and $A[n]$ is reset by M1_f.

III. EXPERIMENTAL RESULTS AND DISCUSSION

A. Simulation of the Proposed Integrated Gate Driver

The proposed integrated gate driver was designed and verified by HSPICE simulation with RPI a-Si TFT model $(\text{Level} = 61)$ provided by the foundry. The field-effect mobility and threshold voltage are 0.369 $\text{cm}^2/\text{V} \cdot \text{s}$ and 4.019 V, respectively. Table I indicates the device parameter (channel width (W) to channel length (L) aspect ratio and capacitors) of the proposed gate driver with the output loadings of each stage are one capacitor (17 pF) in parallel with one resistor (10 MΩ). The width of M3 of the proposed gate driver is designed with thousands micrometer for faster to pulling up and down the output loading of oscilloscope.

The input signals are two start pulses (In1 and In2), four clock signals (Clk1, Clk2, Clk3, and Clk4), and ground signal (Vss) with voltage levels from 25 to 0 V. Notice that the pulse width of each clock signal is 40 μs with the operational period time of 160 μs means the clock duty is 25%. Furthermore, a quarter

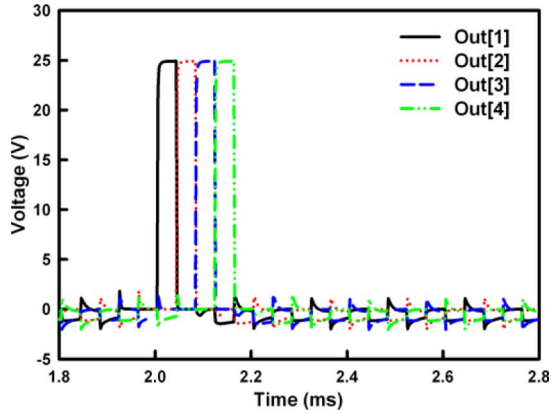


Fig. 6. Simulated waveforms of $\text{Out}[n]$ for the proposed circuit.

TABLE II
SIMULATED RESULTS OF THE PROPOSED CIRCUIT AT THE FIRST TO THE FOURTH OUTPUT

	Rising time (μs)	Falling time (μs)	Noise RMS (V)
Out[1]	1.065	0.586	0.813
Out[2]	1.052	0.651	0.833
Out[3]	1.103	0.593	0.872
Out[4]	1.082	0.593	0.871

of clock duty reduces the stress effect of prominent transistors cause of low stress time for TFT, especially the pull down transistor of M4.

1) Simulation of the Proposed Integrated Gate Driver for Single Direction Scanning: Fig. 6 illustrates the simulated $\text{Out}[n]$ waveforms of the proposed circuit from the first to the fourth stage. Sequential pulse signals have been successfully observed in Fig. 6 to verify the output function of proposed circuit. The rise time, fall time, and noise root mean square (RMS) voltage are represented in Table II, where the rise and fall times are defined by the time difference between 10% to 90% pulse voltage levels, the noise RMS is the root mean square voltage of $\text{Out}[n]$ from T6 to T9 periods.

The power consumption of GOA is calculated from the clock signals and it can be divided into two parts: dynamic and static power, which are shown as follows:

$$P = nACV^2 f + VI. \tag{1}$$

The first term is the dynamic power loss from clock signals' transition. Where A is the fraction of gate actively switching, C is the input loading capacitance of GOA cells, f is the frequency of clock, and n is the whole number of clocks in gate driver. In the proposed circuit, although the number of clocks is doubled, the frequency of clocks and the capacitance of the same clock signal are reduced by half. It means that the dynamic power is halved in the proposed gate driver. Moreover, the proposed circuit deserts the pull-down transistor in before works to reduce the overall parasitic capacitance of GOA cells, so the dynamic power consumption is substantially reduced cause of smaller input loading capacitance.

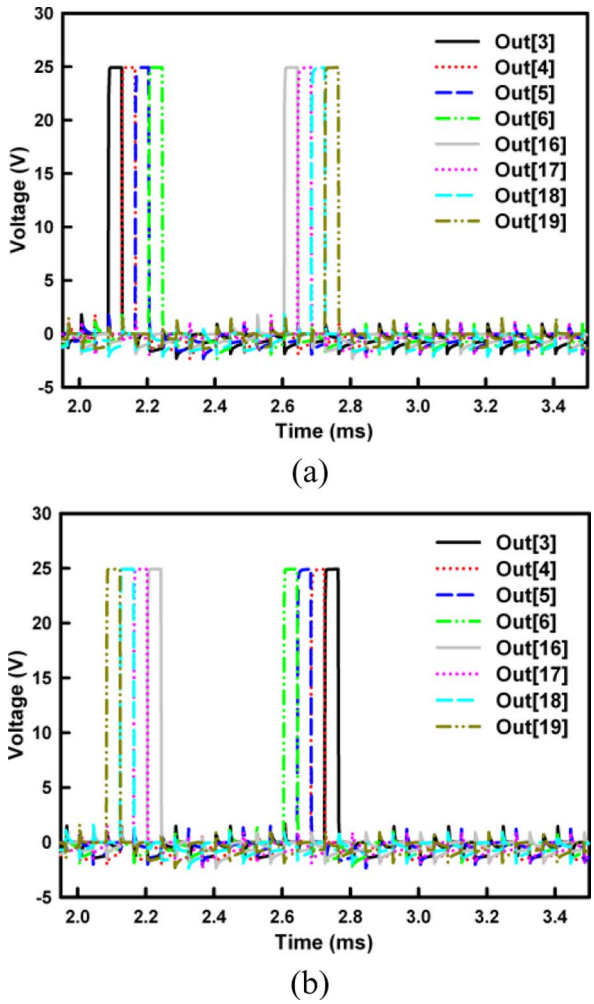


Fig. 7. Simulated output waveforms of bidirectional gate driver circuit at the outputs Out[3], Out[4], Out[5], Out[6], Out[16], Out[17], Out[18] and Out[19]. (a) Forward direction and (b) backward direction.

The second term presents the static power loss from the static current I and voltage source V and the main static power loss of GOA cells is from the leakage current of M3 (when $\mathrm{Out}[n] = \mathrm{Vss}$, $\mathrm{Clk1} = \mathrm{Vdd}$, and $A[n] = \mathrm{Vss}$ in Fig. 2(a)), which is operated in forward sub-threshold region and its formula can be depicted as [21]

$$I_{DS} = I_{0s}\frac{W}{L}e^{(V_{GS}-V_{Ts})/S_f} \tag{2}$$

where W and L are the effective channel width and channel length. V_{TS} denotes the boundary of the forward sub-threshold. Sf is the forward sub-threshold slope, $I_{0\mathrm{s}}$ is the magnitude of current in the sub-threshold region, and V_{GS} is gate to source voltage. For the TFT-LCD panel application, when switching transistor in pixel is turned off, the gate to source voltage of it is about -7 V and the leakage current is low. Nevertheless, when $\mathrm{Out}[n]$ of GOA is Vss, the gate to source voltage of M3 is about 0 V and it induces larger leakage current to result higher static power consumption of GOA cells. For this reason, the lower duty cycle of clock signals of the proposed gate driver (25%) will reduce the duration of high voltage of the pull-up transistor (M3) that can achieve lower static power consumption. Consequently, Table III shows the average power of the proposed circuit (12.57 mW) which is much lower than the before work (32.2 mW) [18], and the overall power reduction ratio is about 61%.

TABLE III
COMPARISON OF POWER SIMULATION BETWEEN PROPOSED CIRCUIT AND BEFORE WORKS

	Proposed circuit	Before work
Pavg(mW)	12.57	32.2

TABLE IV
SIMULATED RESULTS OF BIDIRECTIONAL GATE DRIVER CIRCUIT FOR FORWARD SCANNING AND BACKWARD SCANNING

	Rising time (μs)	Falling time (μs)	Noise RMS (V)
Out[3]	1.14	0.73	0.65
Out[4]	1.14	0.75	0.7
Out[5]	1.11	0.73	0.71
Out[6]	1.14	0.76	0.7
Out[16]	1.13	0.74	0.65
Out[17]	1.15	0.75	0.71
Out[18]	1.12	0.75	0.69
Out[19]	1.14	0.76	0.7
Forward scanning			
	Rising time (μs)	Falling time (μs)	Noise RMS (V)
Out[19]	1.11	0.77	0.65
Out[18]	1.12	0.74	0.6
Out[17]	1.11	0.73	0.7
Out[16]	1.14	0.72	0.65
Out[6]	1.15	0.72	0.7
Out[5]	1.12	0.74	0.6
Out[4]	1.14	0.73	0.65
Out[3]	1.14	0.72	0.65
Backward scanning			

2) Simulation of the Proposed Integrated Gate Driver for Bidirectional Scanning: Fig. 7(a) and (b) show the simulated waveforms of the proposed bidirectional gate driver circuit for forward and backward scanning. The simulated outputs results are shown in Table IV. Notices that the first outputs ($\mathrm{Out}[1]$ and $\mathrm{Out}[2]$) and final outputs ($\mathrm{Out}[20]$ and $\mathrm{Out}[21]$) are dummy stages and they are not shown in Fig. 7(a) and (b) Since the $A[n]$ of dummy stages has no extra source such as M2_b in Fig. 5(a) to discharge it, the $\mathrm{Out}[n]$ will be high if the Clk is in high period. Nevertheless, although the outputs of dummy stages are malfunction, there is no effect on the consequences of bidirectional gate driver circuit since they are not used to the gate lines of panel.

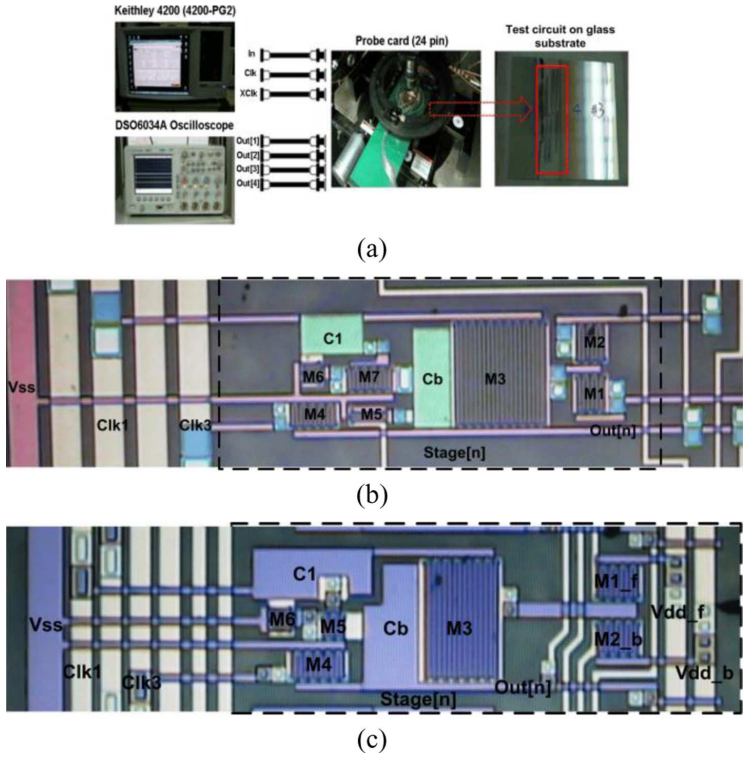


Fig. 8. (a) Measurement setups; (b) die photo of the proposed integrated gate driver; and (c) bidirectional gate driver for array testing.

B. Measurement of the Proposed Integrated Gate Driver

For array verification, one hundred integrated gate driver which are manufactured on glass substrate in amorphous silicon technology. As shown in Fig. 8(a), the measurement setups depict that the synchronous control signals (Clk, XClk, and In) are generated by the pulse card option for Keithley 4200 (4200-PG2), and the input range are set as 0 V to 25 V. Furthermore, digital oscilloscope is utilized to observe the output waveforms. The equivalent loading of its probes is one capacitor (17 pF) in parallel with one resistor (10 MΩ) which is equal to the simulation environment. Moreover, the probe card with 24 pins is applied for the connections between fabricated circuit and measurement equipments. Fig. 8(b) and (c) present the die photo of the proposed integrated gate driver and bidirectional gate driver circuit. Because the widths of M3 is designed with thousands micrometer for pulling up and down the output node ($\mathrm{Out}[n]$), the larger layout area is occupied by M3 in Fig. 8(b) and (c).

1) Measurement of the Proposed Integrated Gate Driver for Single Direction: Fig. 9(a) shows the measured output waveforms of the gate driver circuit for single direction from the first to fourth stages ($\mathrm{Out}[1]$, $\mathrm{Out}[2]$, $\mathrm{Out}[3]$, and $\mathrm{Out}[4]$) and $\mathrm{Out}[50]$, $\mathrm{Out}[100]$, $\mathrm{Out}[101]$, and $\mathrm{Out}[102]$ are shown in Fig. 9(b) The rising time, falling time, and noise RMS are represented in Table V.

2) Measurement of the Proposed Integrated Gate Driver for Single Direction: Fig. 10(a) and (c) shows the measured output waveforms of the bidirectional gate driver circuit from the first to fourth stages ($\mathrm{Out}[1]$, $\mathrm{Out}[2]$, $\mathrm{Out}[3]$, and $\mathrm{Out}[4]$) for the forward scanning and backward scanning. In addition, $\mathrm{Out}[50]$, $\mathrm{Out}[100]$, $\mathrm{Out}[101]$, and $\mathrm{Out}[102]$ are shown in Fig. 10(b) and (d). The rising time, falling time, and noise RMS are represented in Table VI.

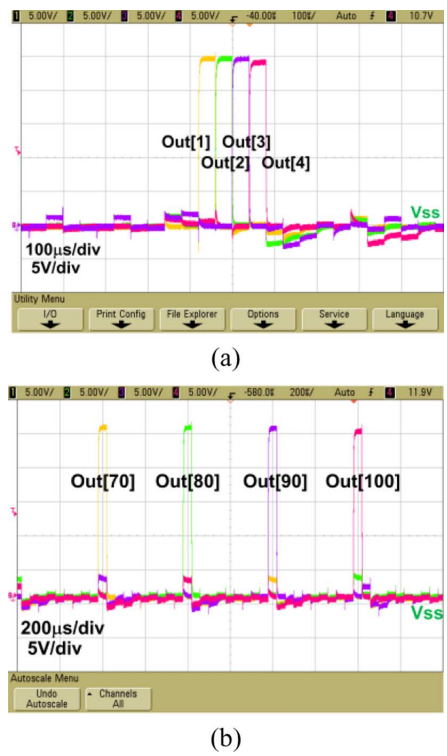


Fig. 9. Measured output waveforms of the proposed gate driver circuit at: (a) head stages ($\mathrm{Out}[1]$, $\mathrm{Out}[2]$, $\mathrm{Out}[3]$, and $\mathrm{Out}[4]$) and (b) tail stages ($\mathrm{Out}[70]$, $\mathrm{Out}[80]$, $\mathrm{Out}[90]$, $\mathrm{Out}[100]$).

Notice that in Fig. 10 the outputs of final two stages for backward scanning, $\mathrm{Out}[1]$ and $\mathrm{Out}[2]$, are malfunction because $A[n]$ has no extra source such as M2_b in Fig. 5(a) to discharge

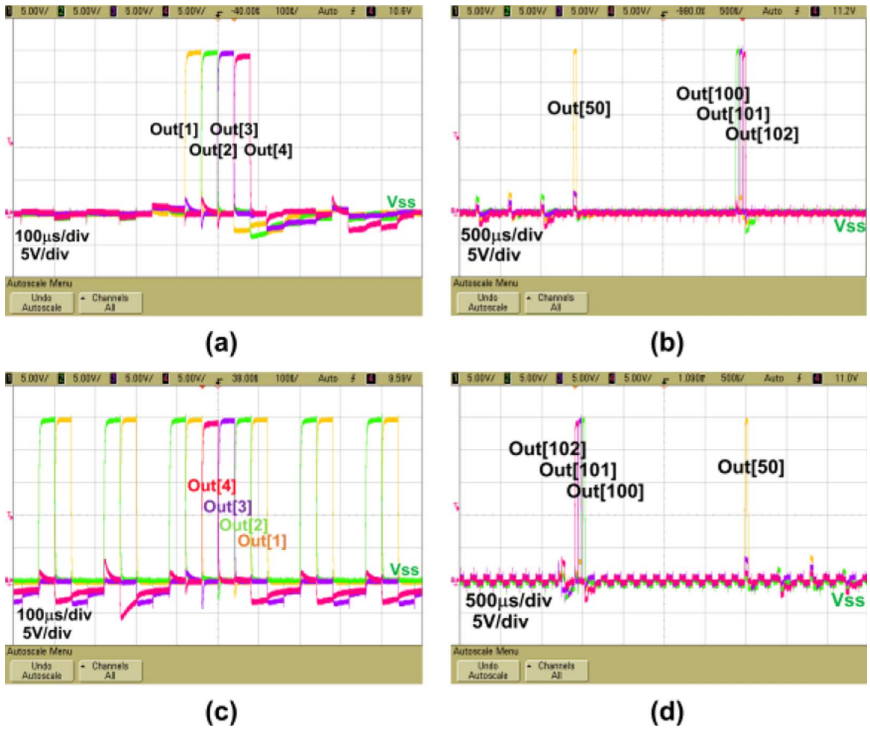


Fig. 10. Measured output waveforms of the bidirectional gate driver circuit by forward scanning for (a) (Out[1], Out[2], Out[3], and Out[4]) (b) Out[50], Out[100], Out[101] and Out[102]) and by backward scanning (c) (Out[1], Out[2], Out[3], and Out[4]) (b) Out[50], Out[100], Out[101] and Out[102]).

TABLE V
MEASURED RESULTS OF THE PROPOSED GATE DRIVER CIRCUIT AT THE HEAD STAGES (Out[1], Out[2], Out[3], AND Out[4]) (B) TAIL STAGES (Out[70], Out[80], Out[90], Out[100])

	Rising time (μs)	Falling time (μs)	Noise RMS (V)
Out[1]	1.92	1.55	0.23
Out[2]	2.3	1.5	0.5
Out[3]	1.85	1.4	0.75
Out[4]	1.98	1.46	0.47
Out[70]	2.09	1.54	0.5
Out[80]	2.22	1.62	0.5
Out[90]	2.2	1.59	0.25
Out[100]	2.34	1.75	0.59

TABLE VI
MEASURED RESULTS OF THE PROPOSED BIDIRECTIONAL GATE DRIVER CIRCUIT FOR FORWARD SCANNING AND BACKWARD SCANNING

	Rising time (μs)	Falling time (μs)	Noise RMS (V)
Out[1]	2.48	1.82	0.29
Out[2]	2.58	1.74	0.58
Out[3]	2.48	1.76	0.1
Out[4]	2.76	1.84	0.58
Out[50]	2.47	1.74	0.25
Out[100]	2.45	1.89	0.158
Out[101]	2.84	1.98	0.107
Out[102]	2.84	1.9	0.23
Forward scanning			
	Rising time (μs)	Falling time (μs)	Noise RMS (V)
Out[102]	1.11	0.77	0.45
Out[101]	1.12	0.74	0.58
Out[100]	1.11	0.73	0.43
Out[50]	1.13	0.72	0.7
Out[4]	1.14	0.72	0.7
Out[3]	1.11	0.73	1.8
Backward scanning			

it, therefore, the $\mathrm{Out}[n]$ will be high if the Clk is in high period. Although the outputs of dummy stages are malfunction, there is no effect on the consequences of bidirectional gate driver circuit since they are not used to the gate lines of panel.

C. Panel Integration of the Proposed Integrated Gate Driver

A 4.5-inch WVGA panel has been fabricated with the proposed integrated gate driver, and its specification is summarized in Table VII. The resolution of the panel is $480 \times \mathrm{RGB} \times 800$ with the contrast ratio of 1000:1 and the frame rate is 60 Hz, respectively.

Besides, the demonstrated 4.5-inch panels are passed the reliability tests of the supporting foundry for operating after the 1000 hours operation under $70^{\circ}\mathrm{C}$ and $-20^{\circ}\mathrm{C}$ conditions. Fig. 11 presents the photo of the proposed integrated gate drivers that are allocated at the both sides of pixel array in a 4.5-inch WVGA panel. The layout area of each stage is 950 μm$\times$207 μm under the layout optimization and the RC load

TABLE VII
THE SPECIFICATION OF A 4.5-INCH WVGA PANEL

	Specification
Panel size (mm*mm)	53.3*91.65
Resolution	480xRGBx800
Frame rate (Hz)	60
Pixel pitch (μm*μm)	103.5*103.5
Back light brightness (cd/m^2)	4000
Contrast ratio	1000:1
Integrated gate driver cell area (μm*μm)	950*207

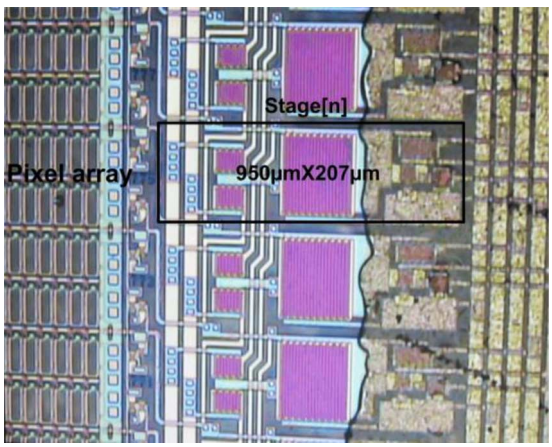
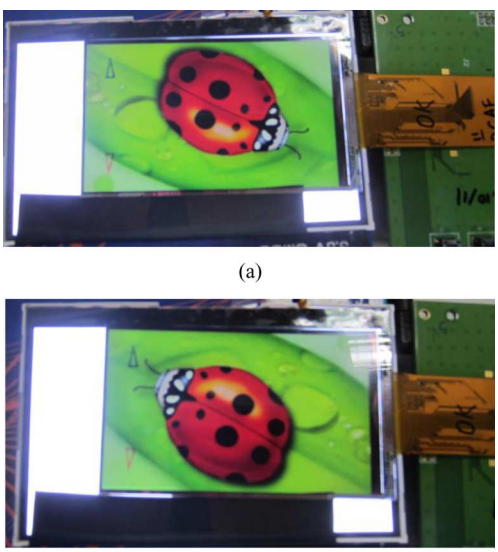


Fig. 11. Photo of the proposed integrated gate drivers that are allocated at the both sides of pixel array in a 4.5-inch WVGA panel.



(a)

(b)

Fig. 12. Display image of a 4.5-inch WVGA panel for: (a) forward direction and (b) backward directions.

for each stage of gate driver is 2.62 kΩ for resistance and 40.4 pF for capacitance. For the sizes of TFTs of gate driver on panel are the some as the simulated sizes of TFTs. Fig. 12(a) shows the display image for forward scanning and Fig. 12(b) shows the reversal display of image for backward scanning of proposed gate drivers.

IV. CONCLUSION

A new gate driver using a-Si TFT technology has been successfully designed and fabricated for TFT-LCD application. The proposed gate driver utilizes four clock signals and only one output charge/discharge TFT to narrow the pixel size and achieve power reduction about 61%. Besides, the scan direction of the proposed gate driver can be adjusted by switching two control signals to accomplish the bidirectional function and it is as well as demonstrated on 4.5-inch WVGA panel successfully. Therefore, the proposed gate driver is quite appropriate for integration into to the high resolution and low power TFT-LCD panels.

REFERENCES

[1] R. Huq and S. Weisbrod, "Phase clocked shift register with cross connecting between stages," U.S. Patent 5 434 899, Jul. 18, 1995.
[2] H. Lebrun, F. Maurice, J. Magarino, and N. Szydlo, "AMLCD with integrated drivers made with amorphous-silicon TFTs," *SID Dig. Tech. Papers*, pp. 403–406, 1995.
[3] F. Maurice, H. Lebrun, N. Szydlo, U. Rossini, and R. Chaudet, "High resolution projection valve with the amorphous silicon AMLCD technology," in *Proc. SPIE*, 1998, pp. 92–99.
[4] T.-C. Huang, K.-T. Cheng, H.-Y. Tseng, and C.-P. Kung, "Reliability analysis for flexible electronics: Case study of integrated a-Si:H TFT scan driver," *J. Emerg. Technol. Comput. Syst.*, vol. 4, no. 3, pp. 1–23, Aug. 2008.
[5] J.-H. Oh, J.-H. Hur, Y.-D. Son, K.-M. Kim, S.-H. Kim, E.-H. Kim, J.-W. Choi, S.-M. Hong, J.-O. Kim, B.-S. Bae, and J. Jang, "2.0 inch a-Si:H TFT-LCD with low noise integrated gate driver," *SID Dig. Tech. Papers*, pp. 942–945, 2005.
[6] S.-Y. Yoon, Y.-H. Jang, B. Kim, M.-D. Chun, H.-N. Cho, N.-W. Cho, C.-Y. Sohn, S.-H. Jo, C.-D. Kim, and I.-J. Chung, "Highly stable integrated gate driver circuit using a-Si TFT with dual pull-down structure," *SID Dig. Tech. Papers*, pp. 348–351, 2006.
[7] S. Edo, M. Wakagi, and S. Komura, ""A 2.2" QVGA a-Si TFT LCD with high reliability integrated gate driver," *SID Dig. Tech. Papers*, pp. 1551–1552, 2006.
[8] J.-W. Choi, J.-I. Kim, S.-H. Kim, and J. Jang, "Highly reliable amorphous silicon gate driver using stable center-offset thin-film transistors," *IEEE Trans. Electron Devices*, vol. 57, no. 9, pp. 2330–2334, Sep. 2010.
[9] C.-L. Lin, C.-D. Tu, M.-C. Chuang, and J.-S. Yu, "Design of bidirectional and highly stable integrated hydrogenated amorphous silicon gate driver circuits," *J. Display Technol.*, vol. 7, no. 1, pp. 10–18, Jan. 2011.
[10] B. Kim and S.-Y. Yoon, "Shift Register," United States Patent 7477226, Jan. 13, 2009.
[11] S.-H. Moon, "Shift register and driving method thereof," U.S. Patent 7 532 701, May 12, 2009.
[12] C.-L. Lin, C.-D. Tu, M.-C. Chuang, K.-W. Chou, and C.-C. Hung, "A highly stable a-Si:H TFT gate driver circuit with reducing clock duty ratio," *Sid Dig. Tech. papers*, pp. 1360–1362, 2010.
[13] M. Powell, "The physics of amorphous-silicon thin-film transistors," *IEEE Trans. Electron Devices*, vol. 36, no. 12, pp. 2753–2763, Dec. 1989.
[14] D. Allee, L. Clark, R. Shringarpure, S. Venugopal, Z.-P. Li, and E. Bawolek, "Degradation effects in a-Si:H thin film transistors and their impact on circuit performance," in *Proc. IRPS*, 2008, pp. 158–167.
[15] N. Ibaraki, M. Kigoshi, K. Fukuda, and J. Kigoshi, "Threshold voltage instability of a-Si:H TFTs in liquid crystal displays," *J. Non-Cryst. Solids*, vol. 115, no. 1–3, pp. 138–140, 1989.
[16] H. Cheng, C. Huang, J. Lin, and J. Kung, "The reliability of amorphous silicon thin film transistors for LCD under DC and AC stresses," in *Proc. Solid-State Integr. Circuit Technol.*, 1998, pp. 834–837.

[17] D. Allee, L. Clark, B. Vogt, R. Shringarpure, S. Venugopal, S. Uppili, K. Kaftanoglu, H. Shivalingaiah, Z.-P. Li, J. Fernando, E. Bawolek, and S. O'Rourke, "Circuit-level impact of a-Si:H thin-film-transistor degradation on effects," *IEEE Trans. Electron Devices*, vol. 56, no. 6, pp. 1166–1176, Jun. 2009.
[18] L.-W. Chu, P.-T. Liu, and M.-D. Ker, "Design of integrated gate driver with threshold voltage drop cancellation in amorphous silicon technology for TFT-LCD application," *J. Display Technol.*, vol. 7, no. 12, pp. 657–664, Dec. 2011.
[19] M. D. Chun, S. Y. Yoon, Y. H. Jang, K. S. Park, H. Y. Kim, B. Kim, H. N. Cho, S. C. Choi, T. W. Moon, N. W. Cho, S. H. Jo, C. Y. Sohn, C. D. Kim, and I. J. Chung, "Bi-directional integrated a-Si gate driver circuit for LCD panel with RGBW quad subpixels," in *Proc. ASID'06*, 2006, pp. 125–127.
[20] C.-L. Lin, C.-D. Tu, M.-C. Chuang, and J.-S. Yu, "Design of bidirectional and highly stable integrated hydrogenated amorphous silicon gate driver circuits," *J. Display Technol.*, vol. 7, no. 1, pp. 10–18, Jan. 2011.
[21] Y. Kuo, *Thin Film Transistors: Materials and Processes*. New York: Kluwer, 2004, vol. 1.

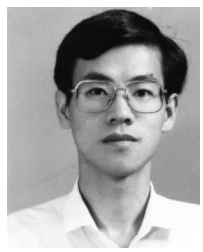
Guang-Ting Zheng received the B.S. degree from the Biomedical Engineering and Environmental Sciences, National Tsing Hua University, Taiwan, in 2008, and the M.S. degree in electro-optical engineering from National Chiao Tung University, Taiwan, in 2010. Since August 2010, he has been working toward the Ph.D. degree at the National Tsing Hua University.

His current research interests include the peripheral circuits integrated on panel for flat panel display applications

Po-Tsun Liu (A'06–SM'07) received the Ph.D. degree from the Institute of Electronics, National Chiao-Tung University (NCTU), Hsinchu, Taiwan, in 2000.

He is a professor and director at the Department of Photonics and Display Institute, NCTU, Taiwan. He also was a visiting professor at the Department of Electrical Engineering at Stanford University, CA, USA, from August 2008 to July 2009. In his specialty, he has made a great deal of pioneering contributions to ULSI technology, semiconductor memory devices and TFT-LCD Displays. In his previous researches on low-dielectric-constant (low-k) materials and copper interconnects, he utilized hydrogen plasma treatment technique for the first time to improve electrical characteristics of low-k silicate-based materials and to resist copper diffusion. In addition, he proposed a low-temperature supercritical carbon dioxide fluids ($SCCO_2$) technology for the first time to improve the dielectric characteristics of the sputter-deposited HfO_2 film by passivating trap states. His current researches focus on the advanced flat panel display device technologies, specialized in thin film transistors (TFTs), the advanced nano-scale semiconductor devices, nonvolatile memory devices, and nano-fabrication technologies. So far, he has published 150 articles of SCI international journals/letters, 80 international conference papers and obtained 17 U.S. patents and 46 Taiwan patents.

Dr. Liu is a member of Society for Information Display. Because of the prominent contributions, he was selected in Marquis Who's Who in the World (20th edition, 2003) and obtained 2007 Outstanding Young Electrical Engineer Award of Chinese Institute of Electrical Engineering. Furthermore, he has superior performance in teaching, and obtained twice Excellent Teaching Awards at NCTU.



Meng-Chyi Wu (A'03–SM'03) was born on November 17, 1957, in Taipei, Taiwan. He received the B.S., M.S., and Ph.D. degrees in electrical engineering from the National Cheng Kung University, Taiwan in 1981, 1983, and 1986, respectively.

He is a professor in the Electrical Engineering Department of the National Tsing Hua University. He has over 22 years of research experience on III–V compound semiconductors, material characterization, optoelectronic devices, and epitaxial techniques consisting of liquid-phase epitaxy, MOCVD, and MBE. He was first to fabricate red AlGaAs/InGaP LEDs in Taiwan, which helps the development of visible LEDs grown by MOCVD. He also fabricated the long-wavelength InGaAsP/InP and AlGaInAs/InP laser diodes (LDs), which contain ridge-waveguide, distributed feedback, and vertical surface-emitting structures, for fiber communication applications. He also fabricated the first high speed (10 GHz) InGaAs/InP and InGaP/GaAs p-i-n photodiodes (PDs) with enhanced wide spectral range of 0.6–1.7μm and 300–900 nm, respectively. In addition, he also integrated p-i-n photodiode with the ruby micro-ball-lens for the alignment tolerance enhancement. He also developed vertical organic thin-film transistors (OTFTs) and transparent conductive oxides for the applications on the optoelectronic devices and displays. He has published over 245 journal papers.

Li-Wei Chu (S'10–M'12) received the B.S. degree from the Department of Electrical Engineering, National Sun Yat-sen University, Taiwan, in 2006, and the M.S. degree in electro-optical engineering from National Chiao Tung University, Taiwan, in 2008. Since August 2008, he has been working toward the Ph.D. degree at the National Chiao Tung University.

His current research interests include the peripheral circuits integrated on panel for flat panel display applications and the design of 60 GHz ESD protection circuits in 65 nm CMOS process.

Meng-Chuan Yang received the B.S. degree from the Department of Electrical Engineering, National Sun Yat-sen University, Taiwan, in 2008, and the M.S. degree in electro-optical engineering from National Chiao Tung University, Taiwan, in 2010.

His current research interests include the peripheral circuits integrated on panel for flat panel display applications