Large-Swing-Tolerant ESD Protection Circuit for Gigahertz Power Amplifier in a 65-nm CMOS Process

Chun-Yu Lin, *Member, IEEE*, Shiang-Yu Tsai, Li-Wei Chu, *Student Member, IEEE*, and Ming-Dou Ker, *Fellow, IEEE*

***Abstract*—The signal swing at output pad of some radio-frequency (RF) power amplifiers (PAs) may be higher than the supply voltage. To protect the gigahertz large-swing power amplifier from electrostatic discharge (ESD) damage in nanoscale CMOS process, a large-swing-tolerant ESD protection circuit is presented in this paper. The proposed ESD protection circuit had been designed, fabricated, and characterized in a 65-nm CMOS process, where it can achieve low parasitic capacitance, large swing tolerance, high ESD robustness, and good latchup immunity. The proposed ESD protection circuit had been further applied to a 2.4-GHz PA to provide 3-kV human-body-model (HBM) ESD robustness without degrading the RF performances.**

***Index Terms*—Electrostatic discharge (ESD), power amplifier (PA), radio-frequency (RF), silicon-controlled rectifier (SCR).**

I. Introduction

WITH the potential for mass production, CMOS technologies have been used to implement radio-frequency (RF) circuits. The RF circuits realized in CMOS technologies are susceptible to electrostatic discharge (ESD) events that may damage the IC products. Therefore, on-chip ESD protection circuits must be added at the RF transceiver that may be stressed by ESD, including the input pads of low-noise amplifier (LNA) and the output pads of power amplifier (PA) [1]–[4]. Of course, adding ESD protection circuit causes RF performance degradation with several undesired effects [5], [6]. Parasitic capacitance of the ESD protection device is one of the most important design considerations for RF circuits. A typical specification for a gigahertz RF circuit on human-body-model (HBM)/machine-model (MM) ESD robustness and the maximum parasitic capacitance of ESD protection device are 2 kV/200 V and 200 fF, respectively [6]–[9]. The conventional double-diode ESD protection scheme with D_P (from input/output pad to V_{DD}) and D_N (from V_{SS} to input/output pad) has been generally used for gigahertz RF circuits, since it can meet the typical specification on ESD robustness and parasitic capacitance [1], [3]. The silicon-controlled rectifier (SCR) device has also been reported to be useful for RF ESD protection [3], [10], [11].

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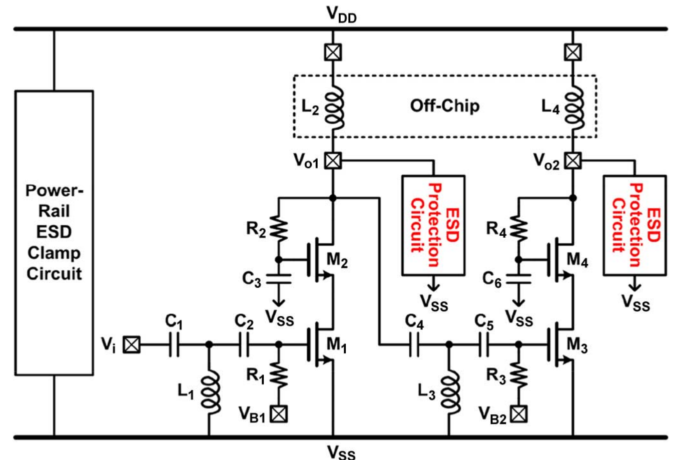

Fig. 1. Power amplifier with ESD protection design.

For some PAs, the signal swing at output pad may be as high as two to three times the supply voltage (V_{DD}). The conventional double-diode or SCR ESD protection designs with a diode from output pad to V_{DD} limits the maximum signal swing at RF output. Therefore, the PA needs large-swing-tolerant ESD protection circuit at its output pad, as shown in Fig. 1. Compared with high-voltage-tolerant ESD clamp circuits used for mixed-voltage I/O buffers [12]–[14], the large-swing-tolerant ESD protection circuit used for RF PA should also be carefully designed. To implement the ESD protection for the PA without limiting the maximum signal swing, some ESD protection designs have been presented. Some PAs have been realized with on-chip ESD protection inductors in their output matching network [4], [15]. For the PAs without on-chip ESD protection inductors [16], [17], a diode string between output pad and V_{DD} could be used [18], as shown in Fig. 2. Of course, this technique is adverse to ESD protection because the overall turn-on resistance and the clamping voltage of the diode string during ESD stresses are increased as well.

In this work, a novel large-swing-tolerant ESD protection circuit is proposed for effective ESD protection on gigahertz PA. This design can achieve low parasitic capacitance, large swing tolerance, high ESD robustness, and good latchup immunity.

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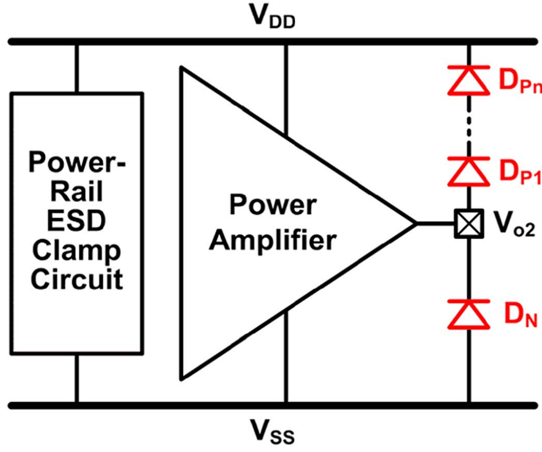

Fig. 2. Conventional ESD protection circuit.

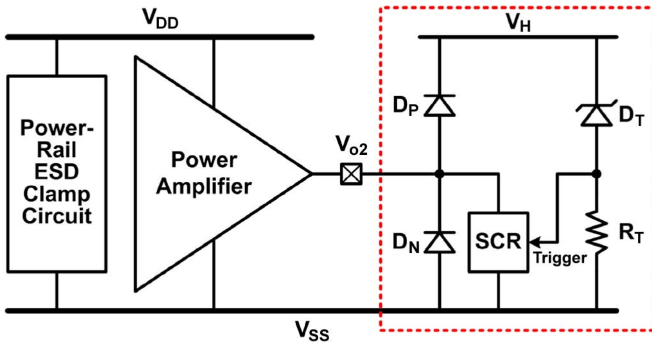

Fig. 3. Proposed ESD protection circuit.

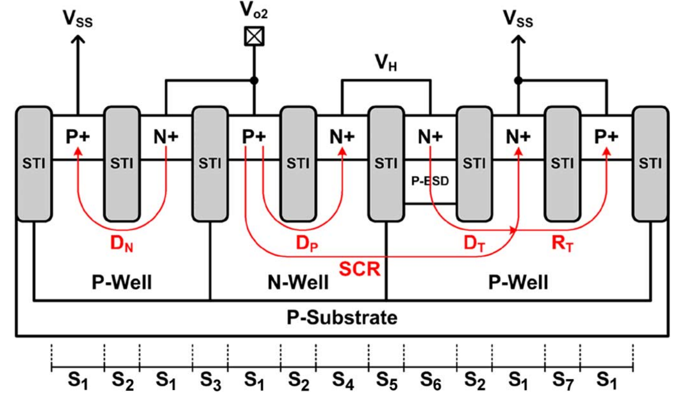

Fig. 4. Cross-sectional view of test circuit.

II. Design of Proposed ESD Protection Circuit

The new proposed ESD protection circuit utilizes diodes and an SCR as main ESD-current-discharging paths. The proposed ESD protection circuit is shown in Fig. 3, which consists of a P-type diode (D_P), a high-voltage node (V_H), an N-type diode (D_N), an SCR, a trigger diode (D_T), and a trigger resistor (R_T). The D_N and SCR provide the ESD paths between V_{o2} and V_{SS}. The power-rail ESD clamp circuit is used to provide the ESD paths between V_{DD} and V_{SS}. The V_H is an internal node, so the protection between V_H and V_{DD} is not needed. The proposed ESD protection circuit can also be used at V_{o1} pad.

The equivalent circuit of the SCR consists of the cross-coupled PNP and NPN BJTs. As ESD stresses from anode to cathode of the SCR are applied, the positive-feedback regenerative mechanism of PNP and NPN BJTs results in the SCR device becoming highly conductive to make the SCR very robust against ESD stresses [19]. However, the stand-alone SCR device has a drawback of higher turn-on voltage. To reduce the turn-on voltage, the trigger signal can be sent into the base terminal of the NPN BJT of SCR device. Once ESD stresses from anode to cathode of the SCR, the D_P and D_T will turn on first, and then the R_T will generate a high voltage to trigger the SCR.

While positive ESD charges stress to V_{o1} or V_{o2} with grounded V_{SS} (PS mode), the trigger signal is sent through the forward-biased D_P, reverse-breakdown D_T, and R_T to enhance the turn-on efficiency of SCR, and the ESD currents can be discharged through the SCR. As positive ESD charges stress to V_{o1} or V_{o2} with grounded V_{DD} (PD mode), the ESD currents can be discharged through the SCR to the floating V_{SS}, and then through the power-rail ESD clamp circuit to V_{DD}. While negative ESD charges stress to V_{o1} or V_{o2} with grounded V_{SS} (NS mode), the ESD currents can be discharged through the forward-biased D_N. As negative ESD charges stress to V_{o1} or V_{o2} with grounded V_{DD} (ND mode), the ESD currents can be discharged through the forward-biased D_N to the floating V_{SS}, and then through the power-rail ESD clamp circuit to V_{DD}. As ESD charges stress between V_{o1} and V_{o2} (pin-to-pin mode), the ESD currents can be discharged through the first SCR and the second forward-biased D_N. The proposed ESD protection circuit in Fig. 3 can provide the corresponding ESD paths.

Under normal RF circuit operating conditions, the V_H node is charged and kept at a high voltage by the output swing of the power amplifier; therefore, the D_P is kept off. Besides, the D_N and SCR are also kept off to prevent from the signal loss.

To realize the proposed design in silicon chip, a cross-sectional view of test circuit is shown in Fig. 4. All the components used in the proposed design are embedded in this structure. The D_P and D_N are realized by P+/N-well and N+/P-well junctions, respectively. The SCR path consists of P+, N-well, P-well, and N+. The D_T is realized by N+/P-ESD junction, where the P-ESD denotes the p-type ESD implantation [20]. The R_T is realized by the P-well resistor.

The dimensions of the test circuits are labeled as S_1, S_2, S_3, S_4, S_5, S_6, and S_7. The P+/N-well and N+/P-well junctions in the main ESD-current-discharging paths of D_N and SCR should be wide enough, so the S_1 is selected to 0.8 μm. The turn on voltage of SCR is mainly determined by the breakdown voltage of D_T. The test circuits with different dimensions are split to investigate the characteristics of the proposed ESD protection circuit, including the parasitic capacitance, ESD robustness, turn on voltage, and holding voltage. In the test circuit A, the dimensions are arranged as $S_1 = 0.8\ \mu$m, $S_2 = 0.3\ \mu$m, $S_3 = 0.3\ \mu$m, $S_4 = 0.2\ \mu$m, $S_5 = 0.3\ \mu$m, $S_6 = 0.4\ \mu$m, and $S_7 = 1\ \mu$m. In the test circuits B, C, D, E, F, and G, the dimensions are changed to $S_2 = 1\ \mu$m, $S_3 = 1\ \mu$m, $S_4 = 1\ \mu$m, $S_5 = 1\ \mu$m, $S_6 = 1\ \mu$m, and $S_7 = 0.5\ \mu$m, respectively. The device width (W) of the test circuits are kept at 40 μm, which is estimated to pass 2-kV HBM and 200-V MM ESD tests. All these dimensions of test circuits are listed in Table I.

TABLE I
DESIGN PARAMETERS AND MEASUREMENT RESULTS OF TEST CIRCUITS

<table>
<tr><th colspan="2" rowspan="2"></th><th colspan="7">Test Circuits</th></tr>
<tr><th>A</th><th>B</th><th>C</th><th>D</th><th>E</th><th>F</th><th>G</th></tr>
<tr><td rowspan="8">Design</td><td>S_1 (μm)</td><td colspan="7">0.8</td></tr>
<tr><td>S_2 (μm)</td><td>0.3</td><td>1</td><td colspan="5">0.3</td></tr>
<tr><td>S_3 (μm)</td><td colspan="2">0.3</td><td>1</td><td colspan="4">0.3</td></tr>
<tr><td>S_4 (μm)</td><td colspan="3">0.2</td><td>1</td><td colspan="3">0.2</td></tr>
<tr><td>S_5 (μm)</td><td colspan="4">0.3</td><td>1</td><td colspan="2">0.3</td></tr>
<tr><td>S_6 (μm)</td><td colspan="5">0.4</td><td>1</td><td>0.4</td></tr>
<tr><td>S_7 (μm)</td><td colspan="6">1</td><td>0.5</td></tr>
<tr><td>W (μm)</td><td colspan="7">40</td></tr>
<tr><td rowspan="6">Measurement</td><td>Parasitic Capacitance at 2.4 GHz (fF)</td><td>75.7</td><td>74.6</td><td>73.4</td><td>75.3</td><td>74.8</td><td>77.6</td><td>75.3</td></tr>
<tr><td>HBM ESD Robustness (kV)</td><td>3.25</td><td>3.25</td><td>3.25</td><td>3</td><td>3.25</td><td>3</td><td>3</td></tr>
<tr><td>MM ESD Robustness (V)</td><td>200</td><td>200</td><td>225</td><td>175</td><td>200</td><td>200</td><td>175</td></tr>
<tr><td>TLP V_{t1} (V)</td><td>8.04</td><td>8.65</td><td>8.08</td><td>8.25</td><td>7.99</td><td>7.97</td><td>8.18</td></tr>
<tr><td>TLP I_{t2} (A)</td><td>1.76</td><td>1.82</td><td>1.76</td><td>1.66</td><td>1.73</td><td>1.69</td><td>1.64</td></tr>
<tr><td>DC V_{hold} (V)</td><td>2.52</td><td>3.11</td><td>2.37</td><td>3.61</td><td>3.1</td><td>3.07</td><td>2.79</td></tr>
</table>

III. EXPERIMENTAL RESULTS OF PROPOSED ESD PROTECTION CIRCUIT

The test circuits have been fabricated in a 65-nm salicided CMOS process without using the silicide-blocking mask. To facilitate the on-wafer RF measurement, these test circuits are arranged with ground-signal-ground (G-S-G) style in layout.

A. Parasitic Capacitance

With the on-wafer measurement, the two-port S-parameters of the test circuits were measured by using the vector network analyzer. The source and load resistances to the test circuits are kept at 50 Ω. In order to extract the intrinsic characteristics of the test circuits in high frequencies, the parasitic effects of the G-S-G pads have been removed by using the de-embedding technique [21]. The parasitic capacitance of each test circuit can be extracted from the S-parameters. Fig. 5 shows the extracted parasitic capacitance of the test circuits from 0 to 20 GHz. The intrinsic parasitic capacitances of the test circuits are about 75 fF at 2.4 GHz.

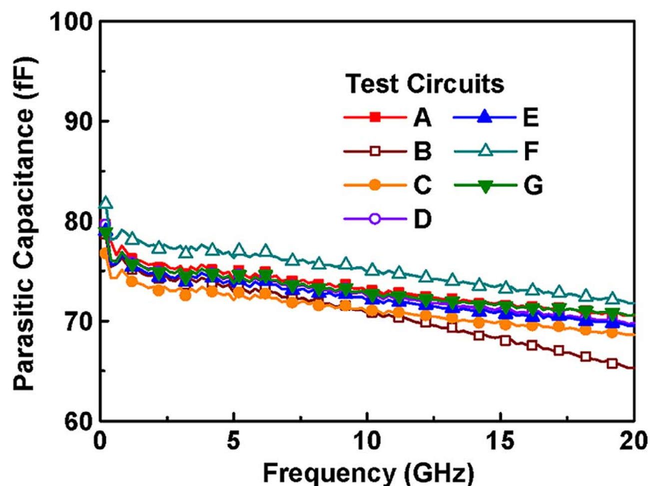

Fig. 5. Parasitic capacitance of test circuits.

B. ESD Robustness

The HBM and MM ESD robustness of the test circuits are evaluated by the ESD tester. The failure criterion is defined as the I–V curve seen between test pads shifting over 30% from its original curve after ESD stressed at every ESD test level. In other words, the leakage current under V_{DD} bias (2.5 V, in this work) will not increase over 30% if the test circuit is not failed after ESD stresses. The test circuits A, B, C, D, E, F, and G have about 3-kV HBM and about 200-V MM ESD robustness.

To investigate the turn-on behavior and the I–V characteristics in high-current regions of the ESD protection circuits, the transmission-line-pulsing (TLP) system with 10-ns rise time and 100-ns pulse width is used. The TLP-measured I–V characteristics are shown in Fig. 6. The trigger voltages (V_{t1}) of the test circuits are about 8 V, which means the ESD protection circuit can sustain up to 8-V signal swing. The secondary breakdown current (I_{t2}) of ESD protection circuit, which indicated the current-handling ability, can also be obtained from the TLP-measured I–V curve. All test circuits can achieve the I_{t2} of about 1.7-A.

C. Latchup Immunity

The dc I–V curves of the test devices are shown in Fig. 7. The holding voltages (V_{hold}) of the ESD protection circuits under dc measurement are lower than those under TLP measurement due to the self-heating effect [22]. The test circuits B, D, E, F, and G exhibit dc V_{hold} larger than V_{DD} (2.5 V) with at least 10% margin, which are very safe from latchup event. All these measured data are summarized in Table I.

D. Discussion

According to the experimental results, most of the test circuits achieve the targets of 2-kV HBM/200-V MM ESD robustness

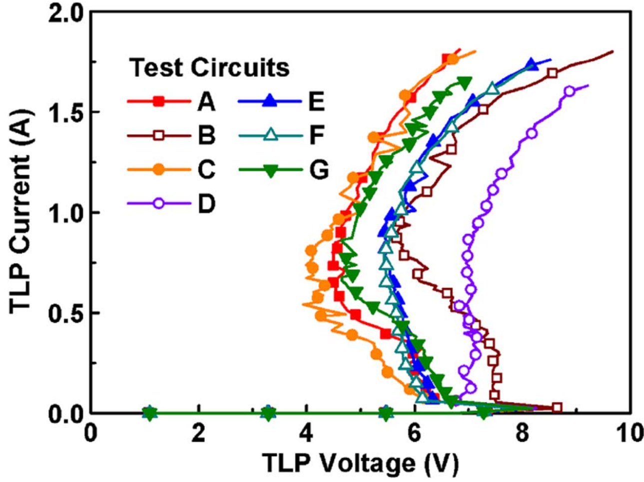

Fig. 6. TLP I–V curves of test circuits.

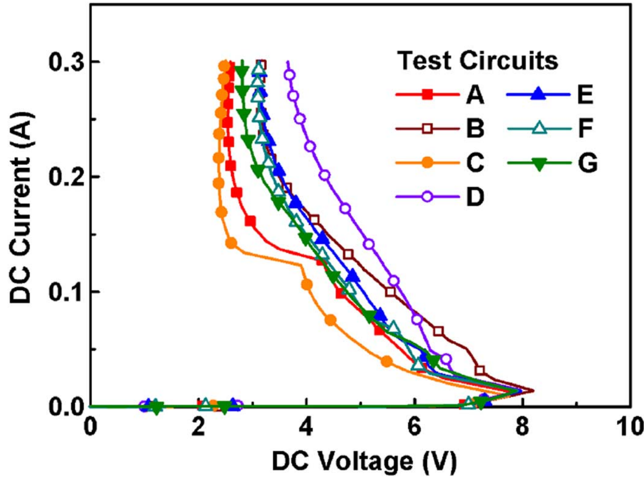

Fig. 7. DC I–V curves of test circuits.

and 8-V signal swing tolerance with only ~75-fF parasitic capacitance. Among the test circuits, the test circuit E with 74.8-fF parasitic capacitance, 3.25-kV HBM/200-V MM ESD robustness, 7.99-V TLP V_{t1}, 1.73-A TLP I_{t2}, and 3.1-V dc V_{hold} is much suitable for ESD protection on the PA.

IV. PA With Proposed ESD Protection Circuit

The proposed ESD protection circuit has been further applied to the PA shown in Fig. 1. The test circuit E is selected to protect the V_{o1} and V_{o2} pads of the PA.

A. PA Design and Implementation

The PA is designed to operate at 2.4 GHz with V_{DD} supply of 2.5 V. To sustain large signal swing, the PA utilizes the self-biased cascade topology [23]. The dimensions of devices used in the PA are listed in Table II. The simulated small-signal gain of the PA is 25 dB. The maximum output power is 23 dBm with a power gain of 30 dB and a PAE of 34%. The maximum drain voltage of M_4 is 5.97 V, and the maximum drain-to-gate and drain-to-source voltages of M_4 (M_3) are 2.28 V and 3.14 V (1.87 V and 2.83 V), respectively. With the simulated voltage and current waveforms, a reliability simulation result shows the PA can pass the lifetime >10 years.

TABLE II
Design Parameters of Power Amplifier

1st Stage		2nd Stage	
M_1 (μm/μm)	512/0.28	M_3 (μm/μm)	3072/0.28
M_2 (μm/μm)	512/0.28	M_4 (μm/μm)	3072/0.28
L_1 (nH)	5.62	L_3 (nH)	1.32
L_2 (nH)	2.80	L_4 (nH)	3.32
C_1 (pF)	0.32	C_4 (pF)	0.60
C_2 (pF)	0.32	C_5 (pF)	3.33
C_3 (pF)	2.41	C_6 (pF)	2.41
R_1 (kΩ)	5	R_3 (kΩ)	5
R_2 (kΩ)	2.5	R_4 (kΩ)	2.5

In some RF applications, the off-chip inductors are used due to the higher inductance and the better quality factor, as the L_2 and the L_4 used in Fig. 1. To simplify the test environment in this work, the L_2 and the L_4 are implemented on chip, but they did not directly connect to V_{DD}. Additional V_{DD}^* pads are used to connect the L_2 and the L_4 to V_{DD} supply under RF measurements, while the V_{DD}^* pads are floating under ESD tests. This arrangement can simulate the ESD test condition of PA with off-chip inductors.

The PA with and without ESD protection circuits have been fabricated in 65-nm CMOS process. Fig. 8 shows the chip photograph of the ESD-protected PA. The V_{o1}, V_{o2}, V_{DD}, and V_{SS} pads are arranged for ESD tests, while the V_i and V_{o2} pads in G-S-G style and the V_{DD}^*, V_{B1}, and V_{B2} in P-G-P style are arranged for RF measurements. The layout area of each PA is $1000 \times 1100\ \mu m^2$, including all pads. In the ESD-protected PA, the proposed ESD protection circuits are added beside the V_{o1} and V_{o2} pads, which does not increase the layout area.

B. RF Measurement Results Before ESD Tests

The RF characteristics are measured on wafer through G-S-G microwave probes. The input and output of PA were matched to 50 Ω. Each PA circuit operates with the 2.5-V V_{DD} supply and draws a total current of 420 mA. The used bias voltages V_{B1} and V_{B2} are all 0.9 V. The measured S_{11} and S_{21} parameters of the PAs are shown in Fig. 9. The peak power-gain frequencies of both PAs are shifted to about 2.65 GHz. The small-signal gains at 2.65 GHz are about 23 dB for two PAs. The input return losses for both PAs are about 20 dB at 2.65 GHz. The maximum output power of both PAs are about 22 dBm with power gain of 21 dB and PAE of 28%. The proposed ESD protection circuit does not degrade the RF performances of the PA.

C. RF Measurement Results After ESD Tests

To verify the ESD protection ability of the proposed ESD protection circuit, the RF performances of both PAs after ESD tests are re-measured. All PS, PD, NS, ND, and pin-to-pin modes of HBM ESD stresses are performed to the PAs.

The output power (P_{out}), power gain, and PAE of the PA without ESD protection circuit are severely degraded after 1-kV HBM ESD tests, as seen in Figs. 10–12. In contrast with the unprotected PA, the ESD-protected PA still works after 3-kV HBM ESD tests. The output power, power gain, and PAE of the PA with the proposed ESD protection circuits after HBM ESD tests are shown in Figs. 13–15, respectively.

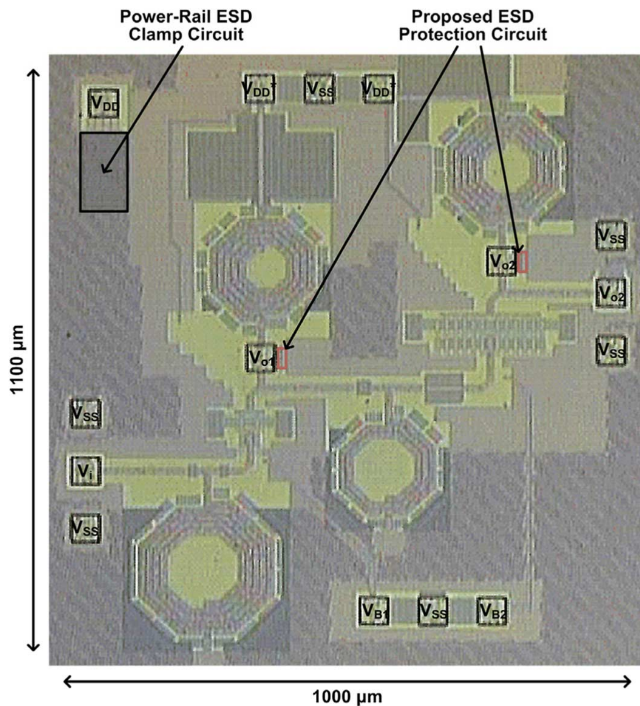

Fig. 8. Chip photograph of PA with proposed ESD protection circuit.

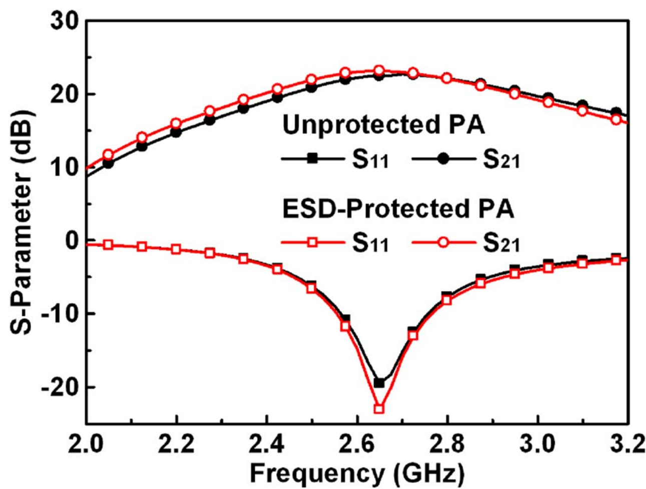

Fig. 9. S-parameters of PA with and without ESD protection circuit.

D. Very Fast TLP

To evaluate the effectiveness of the proposed ESD protection circuit in faster ESD-transient events, a very-fast-TLP (VFTLP) system with 0.2-ns rise time and 1-ns pulse width is used in this study. The VFTLP system can be used to capture the transient behavior of ESD protection circuits in the time domain of charged-device-model (CDM) ESD event [24]. The VFTLP-measured I–V characteristics of the PA with and without ESD protection circuits are shown in Fig. 16. The proposed ESD protection circuit is fast enough to be turned on under such a fast-transient pulse to improve the ESD robustness.

E. Failure Analysis

The ESD-protected PA after 4-kV HBM ESD test has failed. Fig. 17 shows the emission microscope (EMMI) analysis of the

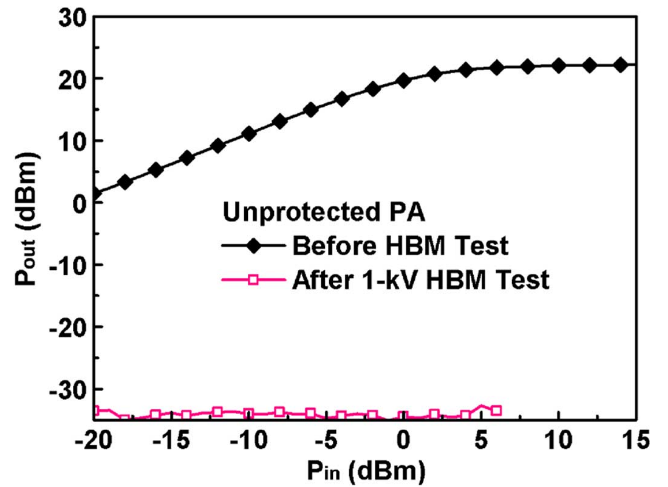

Fig. 10. P_{out} versus P_{in} of PA without ESD protection circuit.

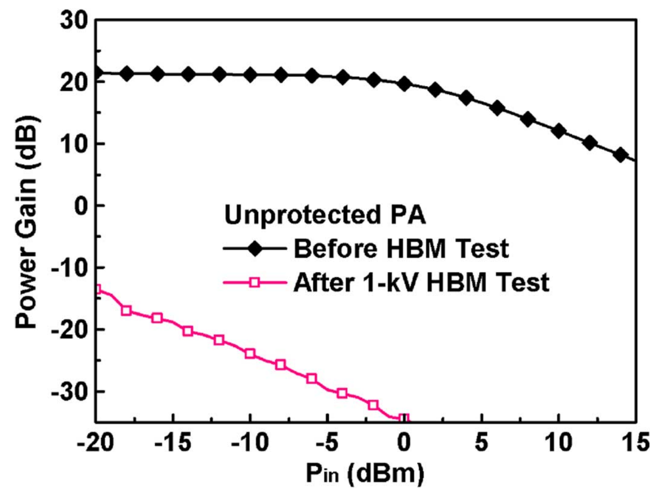

Fig. 11. Power gain versus P_{in} of PA without ESD protection circuit.

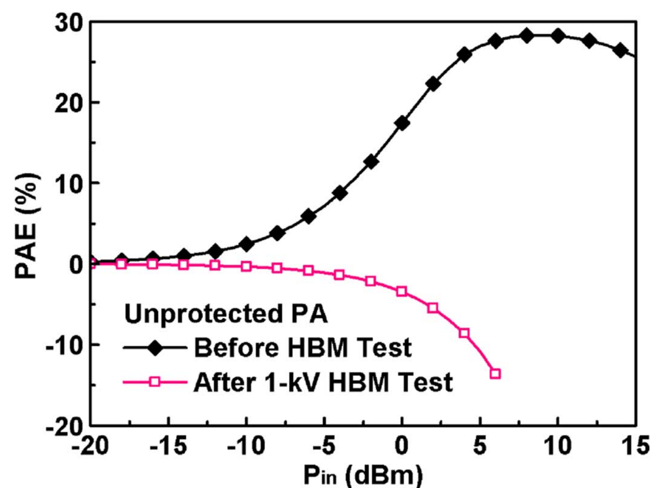

Fig. 12. PAE versus P_{in} of PA without ESD protection circuit.

PA with new proposed ESD protection circuits after 4-kV HBM ESD tests, where failure location is found in the ESD protection circuit beside V_{o1} pad. The proposed ESD protection circuit has

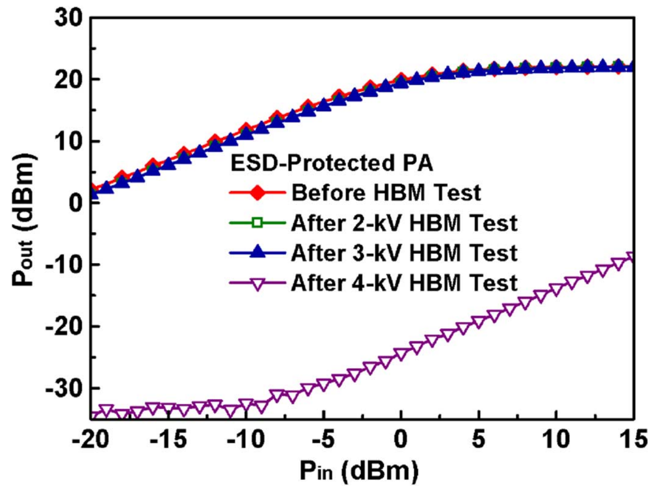

Fig. 13. P_{out} versus P_{in} of PA with ESD protection circuit.

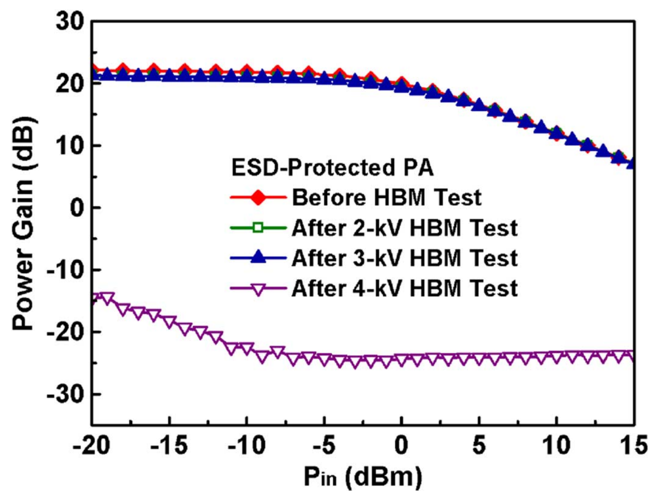

Fig. 14. Power gain versus P_{in} of PA with ESD protection circuit.

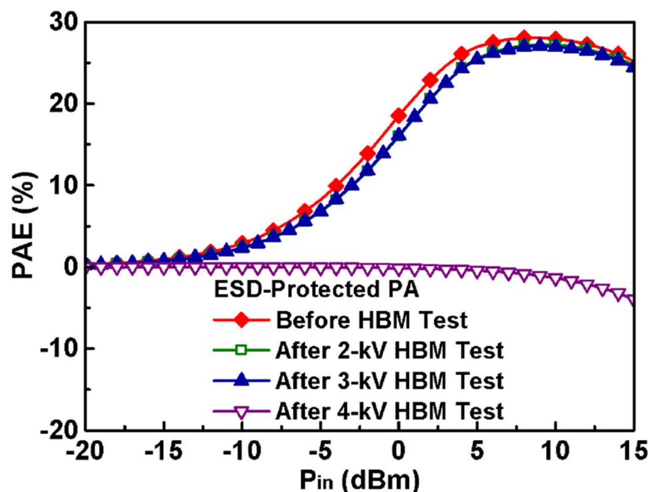

Fig. 15. PAE versus P_{in} of PA with ESD protection circuit.

been verified to protect the PA from ESD damage with 3-kV HBM ESD robustness.

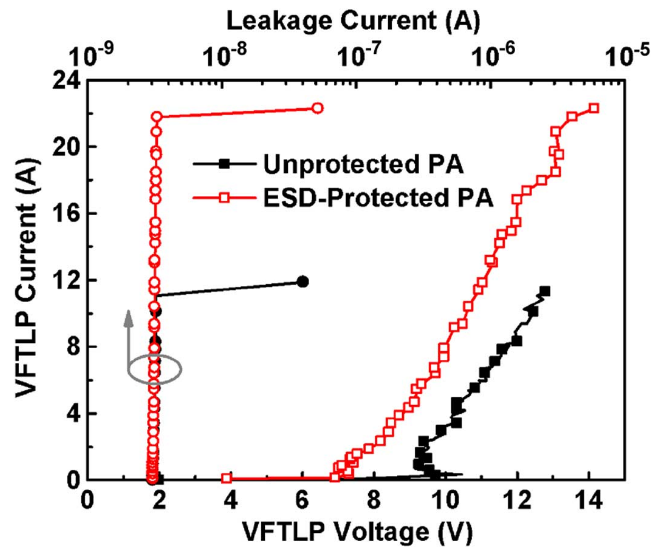

Fig. 16. Very-fast-TLP I–V curves of PA with and without ESD protection circuit.

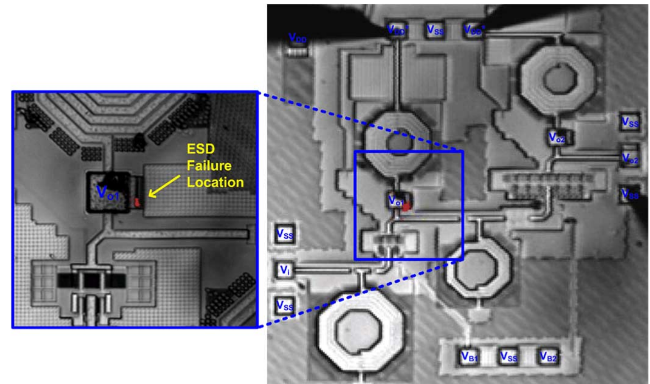

Fig. 17. EMMI photograph to show ESD failure location.

V. Conclusion

The new ESD protection circuit with low parasitic capacitance, large swing tolerance, high ESD robustness, and good latchup immunity has been developed for the gigahertz power amplifier. The test circuits have been designed, realized, fabricated, and characterized in a 65-nm CMOS process. Seven test circuits with different dimensions have been investigated, in which the test circuit E with 74.8-fF parasitic capacitance, 3.25-kV HBM/200-V MM ESD robustness, 7.99-V TLP-measured V_{t1}, 1.73-A TLP-measured I_{t2}, and 3.1-V dc V_{hold} has been applied to a 2.4-GHz PA. Measurement results verify the RF performances and confirm the ESD protection ability. The proposed ESD protection circuit provides 3-kV HBM ESD robustness without degrading the RF performances of PA, while the stand-alone PA even cannot sustain 1-kV HBM ESD tests. The proposed ESD protection circuit can be further applied to millimeter-wave power amplifiers, once they can be combined or co-designed.

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included Mr. M.-H. Song, Mr. C.-P. Jou, Mr. T.-H. Lu, Mr. J.-C. Tseng, Mr. M.-H. Tsai, Mr. T.-L. Hsu, Mr. P.-F. Hung, Mr. Y.-L. Wei, and Mr. T.-H. Chang.

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