IOPscience iopscience.iop.org

Home Search Collections Journals About Contact us My IOPscience

High On/Off Ratio and Very Low Leakage in p^+/n and n^+/p Germanium/Silicon Heterojunction Diodes

This content has been downloaded from IOPscience. Please scroll down to see the full text.

2013 Appl. Phys. Express 6 024001

(http://iopscience.iop.org/1882-0786/6/2/024001)

View the table of contents for this issue, or go to the journal homepage for more

Download details:

IP Address: 140.113.38.11
This content was downloaded on 26/04/2014 at 07:27

Please note that terms and conditions apply.

Applied Physics Express 6 (2013) 024001
http://dx.doi.org/10.7567/APEX.6.024001

High On/Off Ratio and Very Low Leakage in p⁺/n and n⁺/p Germanium/Silicon Heterojunction Diodes

Che-Wei Chen[1], Cheng-Ting Chung[1], Jyun-Chih Lin[1], Guang-Li Luo[2], and Chao-Hsin Chien[1,2]*

[1] Department of Electronics Engineering and Institute of Electronics, National Chiao Tung University, Hsinchu 300, Taiwan, R.O.C.
[2] National Nano Device Laboratories, Hsinchu 300, Taiwan, R.O.C.
E-mail: chchien@faculty.nctu.edu.tw

Received October 24, 2012; accepted January 3, 2013; published online January 25, 2013

We demonstrate the characteristics of p^+-Ge/n-Si and n^+-Ge/p-Si heterojunction diodes with a very high on/off ratio and very low leakage current using heteroepitaxial Ge grown directly on Si. The current ratio of p^+-Ge/n-Si and n^+-Ge/p-Si heterojunction is $\sim 5 \times 10^7$ and $\sim 3 \times 10^6$, respectively. The remarkably low off current density is 2.1 μA/cm² for p^+-Ge/n-Si and 19 μA/cm² for n^+-Ge/p-Si at a reverse bias of $|V_R| = \pm 1$ V, respectively. High on current density (125 A/cm² for p^+-Ge/n-Si and 54 A/cm² for n^+-Ge/p-Si) with a forward bias $|V_F| = \pm 1$ V is obtained with a GeO_2 passivation and an Al_2O_3 isolation. © 2013 The Japan Society of Applied Physics

Germanium (Ge) has been demonstrated as a promising candidate for monolithic integration with silicon metal–oxide–semiconductor field-effect transistors (Si MOSFET) and for expanding the function range of the complementary metal–oxide–semiconductor (CMOS) circuits.[1,2] However, to process needed to integrate Ge devices on a Si wafer for high performance applications is extremely challenging because of the 4.2% lattice mismatch between Ge and Si. Usually, a high temperature post-growth annealing is needed to achieve high quality hetero-epitaxial Ge films.[3,4] Moreover, fast n-type dopant diffusion[5] and relatively low dopant solubility[6] are serious issues during the activation in Ge, making high performance heterojunction diodes very difficult. In a past report,[7] p^+/n and n^+/p Ge junction diodes with poor I_{ON}/I_{OFF} ratio and high leakage current density were presented, while, p^+-Ge/n-Si and n^+-Ge/p-Si heterojunction diodes fabricated directly on the Si substrate with a high I_{ON}/I_{OFF} ratio and extremely low leakage current have not yet been demonstrated in the published literature.

In this letter, we demonstrate p^+-Ge/n-Si and n^+-Ge/p-Si heterojunction diodes with high performance and very low leakage current fabricated via heteroepitaxial growth of Ge directly on the Si substrate. We postulate the results of such a favorable I_{ON}/I_{OFF} ratio and low leakage current are due to two possible reasons. First is the inherent physical properties of Si and Ge. The large band gaps in Si contributes to reduced leakage current as a minority carrier; while the smaller band gap found in Ge leads to higher forward current. The second reason is misfit dislocations are not efficient generation and recombination centers since the leakage currents of our diodes are almost independent of applied bias. This approach presented here is very attractive for mass production.

Figure 1 is schematic illustration of the junction structure. The reason why we used a mesa structure is because this is more similar to the junction structure used in fin-type FETs (FinFETs). A undoped Ge film was grown at 420 °C on a 6-in. Si(100) substrate using an ultra high vacuum chemical vapor deposition (UHVCVD). The thicknesses of the Ge films were 120 and 160 nm for the n-Si substrate with a resistivity of 2–7 Ω cm and p-Si substrate with a resistivity of 15–25 Ω cm, respectively. The chamber temperature was raised to 900 °C for 10 min to execute thermal annealing in order to reduce the defect density. Etch-pit density counting

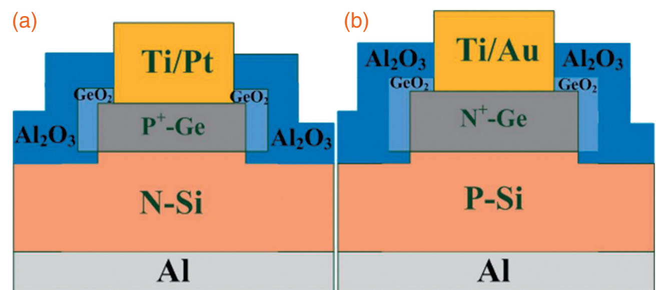

Fig. 1. (a) Schematic illustration of p^+-Ge/n-Si and (b) n^+-Ge/p-Si heterojunction diodes using a mesa structure with a GeO_2 surface passivation and an Al_2O_3 isolation.

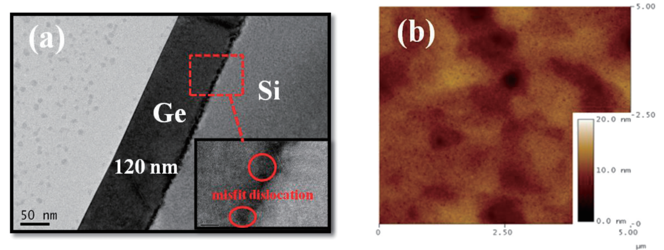

Fig. 2. (a) TEM image of a 120 nm blanket Ge film on the Si substrate showing very low threading dislocation density and smooth surface and magnification image from dash line indication (inset). (b) AFM morphology of the epitaxial Ge on the Si with RMS roughness of ~1.4 nm.

(EPD) is an effective method for measuring threading dislocation densities in the Ge/Si system.[3] To analyze the defect density in the grown films, we used an alternative sample, 4 μm Ge film on Si, because 120 and 160 nm Ge films used in the paper were too thin for EPD analysis. The dislocation density was estimated to be around 10^6–10^7 cm^{-2}. Figure 2(a) shows the transmission electron microscopy (TEM) image of 120 nm Ge film on the n-Si substrate with a low threading dislocation density. A uniform and smooth surface is also observed. In addition, we further confirmed the surface morphology of the Ge film by an atomic force microscopy (AFM) measurement, as shown in Fig. 2(b). The root mean square (RMS) surface roughness is 1.4 nm in a scanning area of 25 μm². To avoid the channeling effect, an oxide of 10 nm was deposited by plasma enhanced chemical vapor deposition (PECVD) on the two type substrates before an implanted region was defined. Boron ions (30 keV,

 © 2013 The Japan Society of Applied Physics

$1 \times 10^{15}\,\mathrm{cm}^{-2}$) and phosphorus ions (50 keV, 1×10^{15} cm^{-2}) were implanted in the active areas of heterojunction. A 100 nm PECVD oxide was deposited for suppressing dopant outdiffusion since the ion implantation damage would result in fast diffusion.[8,9] According to the results in the past reports,[8–11] we know boron has higher activation efficiency while phosphorus needs higher temperature to be activated. Dopant diffusion mechanisms and annihilation of defects in the Ge do influence the shallow junction formation and the leakage current. Activation was performed in nitrogen ambient for 10 s at 500 °C (p^+-Ge/n-Si) and for 10 s at 600 °C (n^+-Ge/p-Si). The heterojunction area ($625\,\mu\mathrm{m}^2$) was formed by using reactive ion etch (RIE) anisotropic etching in Cl_2/HBr ambient using oxide as a hard mask. The GeO_2 as surface passivation layer using rapid thermal oxidation (RTO) at 520 °C for 30 s and then an Al_2O_3 as isolation was performed after removing native oxide by atomic layer deposition (ALD). In particular, thermally grown GeO_2 can act as a good electrical passivation layer between Ge and high-κ dielectrics.[12] for the reduced interface state density and lower surface leakage current. Finally, Ti (5 nm)/ Pt (50 nm) contact for p^+-Ge/n-Si and Ti (5 nm)/ Au (50 nm) contact for n^+-Ge/p-Si heterojunction were deposited by sputtering.

Figure 3(a) shows secondary ion mass spectrometry (SIMS) dopant profiles of the p^+-Ge/n-Si heterojunction diode before and after RTA. The dashed line indicates the thickness of the epi-Ge layer. After the RTA process, the boron dopants were hardly redistributed and no deeper diffusion was observed. This result was similar to that in the former report; the pairing of boron with the defects has a high binding energy so that the atoms are almost immobile.[13] Moreover, we think most of the dopants residing in the Si region remain inactive since the thermal energy of low temperature RTA used in this work was insufficient to activate the dopants. Figure 3(b) shows the SIMS dopant profiles of the n^+-Ge/p-Si heterojunction diode. A slight diffusion of phosphorous dopants is observed after the annealing due to the relatively higher thermal budget required for the n-type dopant activation in Ge.[9]

Recently, there are many articles focusing on the Ge junction diode being published. Park et al.[14] reported on a Ge p^+/n junction diode on an Si substrate using metal-induced dopant activation (MIDA) technique with on/off ratio $\sim 2.1 \times 10^4$, in which on current density (J_{ON}) was $<100\,\mathrm{A/cm^2}$ at $V = 1$ V and off current density (J_{OFF}) was $>1\,\mathrm{mA/cm^2}$ at $V = -1$ V. Yu et al.[15] also reported the selective growth method epi-Ge p^+/n junction diode on the Si using the selective multiple hydrogen anneals for hetero-epitaxy (MHAH) technique. The diode had J_{OFF} of $>10^{-4}$ $\mathrm{A/cm^2}$ at $V = -1$ V and J_{ON} of $\sim 1\,\mathrm{A/cm^2}$ at $V = 1$ V with on/off ratio $<10^4$. Eneman et al.[16] presented an analysis of junction leakage in the heavily doped p^+/n Ge junctions on the Si substrate. A higher counterdoping increased the electric field in the junction and led to higher junction leakage so that the J_{OFF} was $10^{-2}\,\mathrm{A/cm^2}$ at $V = -1$ V without halo implantation. Gity et al.[17] had a study on the p-Ge/n^+-Si diode structure by the direct wafer bonding technique. Due to the fact that most of the depletion region was built inside the p-Ge, a very high J_{OFF} ($\sim 0.12\,\mathrm{A/cm^2}$ at $V = -1$ V) was produced by the generation and recombination process within the Ge. Hence, an on/off ratio of $<10^4$ was demonstrated. Figure 4(a) shows the current–voltage (I–V) characteristic of our p^+-Ge/n-Si heterojunction diode (area: $625\,\mu\mathrm{m}^2$) with a very high on/off ratio $>10^7$ and a very high J_{ON} ($125\,\mathrm{A/cm^2}$ at $V = 1$ V). Cumulative probability versus leakage current density (at $V = -1$ V) is shown excellent uniform distribution of leakage current density in the inset of Fig. 4(a). Also an extremely low J_{OFF} ($2.1\,\mu\mathrm{A/cm^2}$ at $V = -1$ V), which is at least two orders of magnitude smaller than those reported in the above literature, is presented even though a large number of misfit dislocations existing at the Ge/Si interface due to lattice mismatch have been clearly seen in the inset of Fig. 2(a). Misfit dislocations were basically caused by the lattice mismatch between Ge and Si. With Ge being heavily doped and Si lightly doped of p^+-Ge/n-Si heterojunction, most of the depletion region is built inside the n-Si side. Thus, the band to band tunneling (BTBT) leakage current in Ge is effectively suppressed. Moreover, the J_{OFF} is nearly independent of reverse bias, which remains at 1–$2\,\mu\mathrm{A/cm^2}$ current level, indicating the leakage current does not come from trap generation mechanism. Thus, we speculate that the energy level of misfit dislocations is not located at and/or near the middle of band gap, which means the misfit dislocations are not efficient generation and recombination centers. In the modern advanced circuits, huge power consumption is a great concern. The junction leakage certainly

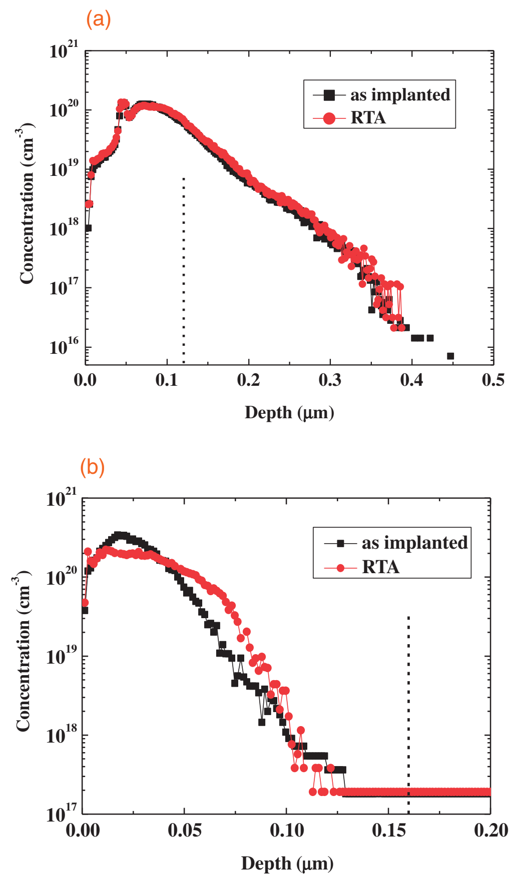

Fig. 3. (a) SIMS depth profile of the p^+-Ge/n-Si heterojunction diode with RTA (500 °C 10 s in N_2 + 520 °C 30 s in O_2). (b) SIMS depth profile of the n^+-Ge/p-Si heterojunction diode with RTA (600 °C 10 s in N_2 + 520 °C 30 s in O_2). and the dashed line indicates the epi-Ge layer thickness.

© 2013 The Japan Society of Applied Physics

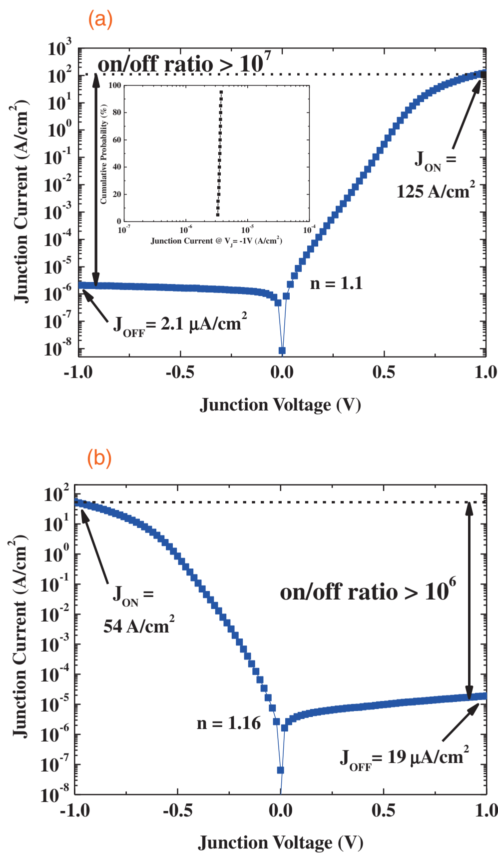

Fig. 4. (a) I–V characteristic of p$^+$-Ge/n-Si heterojunction diode (area: 625 μm^2) with high $I_{ON}/I_{OFF} > 10^7$ and cumulative probability versus leakage current density at junction voltage of -1 V (inset). (b) I–V characteristic of n$^+$-Ge/p-Si heterojunction diode (area: 625 μm^2) with high $I_{ON}/I_{OFF} > 10^6$.

contributes to the off state power consumption. So, our heterojunction with extremely low off current density is very attractive from the viewpoint of power consumption. The ideality factor of our p$^+$-Ge/n-Si heterojunction is ~1.1.

Yu et al.[18] reported the Ge n$^+$/p junction diode using in situ doped epitaxial growth on the Si substrate at 600 °C having an on/off ratio = 1.1×10^4 and J_{OFF} of $\sim 10^{-2}$ A/cm^2 at $V = 1$ V. Also, Park et al.[7] reported the Ge n$^+$/p junction diode formed on the Si substrate by Co MIDA technique with on/off ratio $\sim 3.7 \times 10^2$, $J_{OFF} \sim 7 \times 10^{-1}$ A/cm^2, and $J_{ON} \sim 3 \times 10^2$ A/cm^2 at $|V| = \pm 1$ V. Thareja et al.[19] had a study on the n$^+$/p Ge junction diode using laser annealing technique. The junction diode had J_{OFF} of $\sim 10^{-2}$ A/cm^2, J_{ON} of $\sim 2 \times 10^1$ A/cm^2 at $|V| = \pm 1$ V and an on/off ratio of $\sim 2 \times 10^3$. Jamil et al.[20] also had a study on the n$^+$/p Ge junction diode, which was formed by rapid thermal diffusion of spin-on dopants. The diode had J_{OFF} of $\sim 2 \times 10^{-4}$ A/cm^2, J_{ON} of $\sim 10^2$ A/cm^2 at $|V| = \pm 1$ V and an on/off ratio of $\sim 10^6$. Even though the on/off ratio was the best in the literature, the junction formed by their proposed technique was very deep. Figure 4(b) shows the electrical characteristic of our n$^+$-Ge/p-Si heterojunction diode (area: 625 μm^2) with high on/off ratio $> 10^6$ and a high J_{ON} (54 A/cm^2 at $V = -1$ V). On current density level is similar to those in the literatures, which implies the sufficient dopant activation in our heterojunction. Nevertheless, the on current of n$^+$-Ge/p-Si is slightly lower than the p$^+$-Ge/n-Si heterojunction. Maybe this is due to the fact that the implantation induced defects are very difficult to be annihilated.[10] Thanks to the reduction of the depletion region area in a mesa structure because the depletion region of p$^+$-Ge/i-Ge and i-Ge/n-Si can be eliminated as compared with that in the planar heterojunction structure. The off current density (19 μA/cm^2 at $V = 1$ V) is at least one order of magnitude lower than those reported in the above literature with a shallower (~100 nm) junction depth. This is the same as the situation in the p$^+$-Ge/n-Si heterojunction, the off current is nearly independent of reverse bias so that we think our speculation regarding misfit dislocations is convincing. The ideality factor of our n$^+$-Ge/p-Si heterojunction is ~1.16 at low forward voltages.

In conclusion, we have demonstrated p$^+$-Ge/n-Si and n$^+$-Ge/p-Si heterojunction diodes directly on the Si substrate using the mesa structure. Both p$^+$-Ge/n-Si and n$^+$-Ge/p-Si heterojunction diodes depict very high on/off ratios, which are $\sim 5 \times 10^7$ and $\sim 3 \times 10^6$, respectively. Significantly low off current density is 2.1 μA/cm^2 for p$^+$-Ge/n-Si and 19 μA/cm^2 for n$^+$-Ge/p-Si at $|V_R| = \pm 1$ V. A high on current of 125 A/cm^2 for p$^+$-Ge/n-Si and near the unity ideality factor were observed. Finally, our results for heterojunction diodes shed light on realizing high performance and low off current density Ge MOSFET for future CMOS circuits and more importantly the devices can be made on the large diameter Si wafers.

1) S. Assefa, F. Xia, and Y. A. Vlasov: Nature **464** (2010) 80.
2) J. Feng, Y. Liu, P. B. Griffin, and J. D. Plummer: IEEE Electron Device Lett. **27** (2006) 911.
3) H. Luan, D. R. Lim, K. K. Lee, K. M. Chen, J. G. Sandland, K. Wada, and L. C. Kimerling: Appl. Phys. Lett. **75** (1999) 2909.
4) J. Michel, J. Liu, and L. C. Kimerling: Nat. Photonics **4** (2010) 527.
5) C. O. Chui and K. C. Saraswat: *Germanium-Based Technologies: From Materials to Devices* (Elsevier, Amsterdam, 2007), p. 173.
6) F. A. Trumbore: Bell Syst. Tech. J. **39** (1960) 205.
7) J.-H. Park, D. Kuzum, H.-Y. Yu, and K. C. Saraswat: IEEE Trans. Electron Devices **58** (2011) 2394.
8) C. O. Chui, L. Kulig, J. Moran, W. Tsai, and K. C. Saraswat: Appl. Phys. Lett. **87** (2005) 091909.
9) C. O. Chui, K. Gopalakrishnan, P. B. Griffin, J. D. Plummer, and K. C. Saraswat: Appl. Phys. Lett. **83** (2003) 3275.
10) Y.-L. Chao and J. C. S. Woo: IEEE Trans. Electron Devices **57** (2010) 665.
11) C.-C. Cheng, C.-H. Chien, G.-L. Luo, C.-L. Lin, H.-S. Chen, J.-C. Liu, C.-C. Kei, C.-N. Hsiao, and C.-Y. Chang: IEEE Trans. Electron Devices **56** (2009) 1681.
12) A. Delabie, F. Bellenger, M. Houssa, T. Conard, S. V. Elshocht, M. Aymax, M. Heyns, and M. Meuris: Appl. Phys. Lett. **91** (2007) 082904.
13) S. Uppal, A. F. W. Willoughby, J. M. Bonar, A. G. R. Evans, N. E. B. Cowern, R. Morris, and M. G. Dowsett: J. Appl. Phys. **90** (2001) 4293.
14) J.-H. Park, D. Kuzum, M. Tada, and K. C. Saraswat: Appl. Phys. Lett. **93** (2008) 193507.
15) H.-Y. Yu, M. Ishibashi, J.-H. Park, M. Kobayashi, and K. C. Saraswat: IEEE Electron Device Lett. **30** (2009) 675.
16) G. Eneman, M. Wiot, A. Brugère, O. S. I. Casain, S. Sonde, D. P. Brunco, B. D. Jaeger, A. Satta, G. Hellings, K. D. Meyer, C. Claeys, M. Meuris, M. M. Heyns, and E. Simoen: IEEE Trans. Electron Devices **55** (2008) 2287.
17) F. Gity, K. Y. Byun, K.-H. Lee, K. Cherkaoui, J. M. Hayes, A. P. Morrison, C. Colinge, and B. Corbett: Appl. Phys. Lett. **100** (2012) 092102.
18) H.-Y. Yu, Y. Nishi, K. C. Saraswat, S.-L. Cheng, and P. B. Griffin: IEEE Electron Device Lett. **30** (2009) 1002.
19) G. Thareja, S. Chopra, B. Adams, Y. Kim, S. Moffatt, and K. C. Saraswat: IEEE Electron Device Lett. **32** (2011) 838.
20) M. Jamil, J. Mantey, E. U. Onyegam, G. D. Carpenter, E. Tutuc, and S. K. Banerjee: IEEE Electron Device Lett. **32** (2011) 1203.

© 2013 The Japan Society of Applied Physics