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A nanostructured micellar diblock copolymer layer affects the memory characteristics and packing of pentacene molecules in non-volatile organic field-effect transistor memory devices†

Chia-Min Chen, Chih-Ming Liu, Ming-Chang Tsai, Hsiu-Cheng Chen and Kung-Hwa Wei*

Organic field-effect transistor (OFET) memory devices incorporating the copolymer polystyrene-*block*-poly(4-vinylpyridine) (PS_{56k}-*b*-$P4VP_{8k}$) layer, which features a thickness-dependent micellar nanostructure (P4VP-core, PS-shell), as a charge trapping layer can exhibit tunable memory windows for p-channel applications. For instance, the memory window increased substantially from 7.8 V for the device incorporating a 60 nm thick PS_{56k}-*b*-$P4VP_{8k}$ layer to 21 V for the device incorporating a 27 nm thick layer, an increase of more than 2.5 times. Using simultaneous synchrotron grazing-incidence small-angle X-ray scattering and wide-angle X-ray scattering to probe the nanostructured micellar PS_{56k}-*b*-$P4VP_{8k}$ layer and the pentacene layer positioned directly on the top of the copolymer layers, respectively, we were able to elucidate the structural characteristics of the bilayer and to correlate their effects with the memory performances of devices with similar architectures. For the PS_{56k}-*b*-$P4VP_{8k}$ layers, we found that the inter-micelle distance and their lateral arrangements depended on the layer thickness: the thickness of the PS shells in the lateral direction decreased upon increasing the layer thickness, as did the memory window for the OFET device that incorporated the PS_{56k}-*b*-$P4VP_{8k}$ layers, showing a strong dependence of the threshold voltage shifts (*i.e.*, memory window) on the distance between the micelles. Additionally, for the molecular packing of the pentacene layer positioned on the copolymer layer, we found that the PS_{56k}-*b*-$P4VP_{8k}$ layers affected not only the orientation of the pentacene molecules but also their grain sizes, thereby affecting the hole mobility of the memory devices. These results suggest that tuning the micellar nanostructure of the block copolymer thin film that was used as a trapping layer can be a simple and effective way for optimizing the memory window and affecting the hole mobility of OFET memory devices.

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Introduction

Research into organic non-volatile memory (ONVM) takes advantage of the good scalability, flexibility, and light weight of organic materials and the ability to perform manufacturing processes at low cost.[1–9] Among the various categories of organic memory cells, organic field-effect transistor (OFET) memory devices possessing non-volatile memory are promising candidates for future applications because of their nondestructive reading behavior and direct integrated circuit architectural compatibility.[4–9] An OFET memory device is a modified OFET device that incorporates additional charge trapping layers, comprising metal or semiconductor domains immersed in a dielectric layer between the semiconducting layer (*e.g.*, a pentacene layer) and the insulating layer. Charge can be stored or erased in the trapping layer by applying gate voltages with different biases. The charge trapping layer can be formed by using (i) nanoparticles (NPs) or nanostructures inside a dielectric layer to act as discrete charge storage centers[4–6] or (ii) pure polymers that are chargeable.[7–9] For example, the charge trapping element can be formed from metal NPs dispersed in a polymer dielectric. These layers can then be coated onto the device through solution processing.

Diblock copolymers are self-assembling soft materials that can form a variety of ordered structures (*e.g.*, lamellae, hexagonal cylinders, spheres) having periodic thicknesses ranging between 10 and 200 nm.[10] The incorporation of NPs within well-ordered block copolymers (BCPs) is a versatile approach for preparing the charge-trapping layer. Recently, much attention has been focused on the development of BCP–metal NP composites for ONVM

Department of Materials Science and Engineering, National Chiao Tung, University, 1001 Ta Hsueh Road, Hsinchu, 30050, Taiwan, ROC. E-mail: khwei@mail.nctu.edu.tw; Fax: +886-3-5724727; Tel: +886-3-5731771

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devices, including resistor-,[11] capacitor-,[12,13] and OFET-type memory devices,[14–16] because of the combination of the tunable electron trapping ability of metal NPs and the various types of nanostructured BCPs that self-assemble with NPs into ordered structures. Few reports, however, describe the effects of BCP thin films with various ordered structures on the memory characteristics (*e.g.*, memory window, mobility) of OFET memory devices. The amphiphilic diblock copolymer PS_{56k}-*b*-$P4VP_{8k}$ has a long PS block and a relatively short P4VP block; it self-assembles into micelle-like objects when dissolved in a selective good solvent for the PS block.[17–19] In this study, we used thin films of this nanostructured block copolymer as trapping layers and probed their effects on the resultant memory windows and mobility, as determined by pentacene packing, in OFET-type memory devices. Optimizing the surface morphology and lateral ordering of a BCP on a substrate in a device is critical for enabling the application of such charge trapping layers in organic-based floating gate nonvolatile memory devices. The morphologies of thin layers of BCPs are commonly probed using transmission electron microscopy (TEM) and atomic force microscopy (AFM), but these techniques provide only a localized view of the structural information of the surface. Grazing-incidence small-angle X-ray scattering (GISAXS) is a powerful tool for investigating the global structures of thin films of several square millimeters in area,[20–23] with the ability of unearthing buried or inner structures within a film. GISAXS scattering curves can therefore provide quantitative information regarding the form and structure factors of BCP thin films, thereby revealing nanostructural morphologies within the plane of an object deposited on a substrate.

In this study, we used various layer thicknesses of the diblock copolymer PS_{56k}-*b*-$P4VP_{8k}$ to form charge trapping layers featuring different nanostructures in OFET memory devices, thereby allowing tuning of the memory window and affecting mobility (through packing of pentacene molecules) for p-channel applications of OFET memory devices. Through simultaneous synchrotron GISAXS and grazing-incidence wide-angle X-ray scattering (GIWAXS) analyses on pentacene–PS_{56k}-*b*-$P4VP_{8k}$ bilayer structures, we could not only decipher the nanostructure of the PS_{56k}-*b*-$P4VP_{8k}$ trapping layer but also determine the molecular packing of the pentacene layer, which determined the electric charge fill-in and discharge, positioned directly on the top of the PS_{56k}-*b*-$P4VP_{8k}$ layer, respectively. This allows us to correlate the structure effects of these features with the memory characteristics of the devices with similar architectures. By combining AFM imaging with GISAXS profiling, we found that nanostructured PS_{56k}-*b*-$P4VP_{8k}$ films can have tunable P4VP-core–PS-shell micellar distance, and the structure of micelles was altered substantially at different layer thicknesses, obtained by spin-coating at various solution concentrations. We also used GIWAXS to reveal that the packing order of the pentacene phase increases upon addition of a thin PS_{56k}-*b*-$P4VP_{8k}$ layer, obtained at low solution concentration, and then decreases when incorporating a thicker PS_{56k}-*b*-$P4VP_{8k}$ layer, obtained at high solution concentration. From the device perspectives such as in the programming/erasing operation of the OFET devices, we observed reversible shifts in the threshold voltage (V_t), and examined the effects of the various layer thicknesses of the PS_{56k}-*b*-$P4VP_{8k}$ thin films on the mobilities (μ), on/off current ratios, degrees of V_t shifting, and the numbers of transferred charges (Δn) of the memory devices. Our experimental results suggest that tuning the distance between nanostructured micelles that consist of P4VP-cores and PS-shells and their internal structures in PS_{56k}-*b*-$P4VP_{8k}$ films can greatly influence the memory properties of OFET-type memory devices and the molecular packing of the stacked pentacene molecules on the top of the PS_{56k}-*b*-$P4VP_{8k}$ films, thereby affecting the hole mobility of the devices.

Experimental

Materials and sample preparation

Asymmetric linear PS-*b*-P4VP diblock copolymers (M_n^{PS} = 56 kg mol^{-1}; M_n^{P4VP} = 8 kg mol^{-1}; polydispersity index = 1.07; denoted as PS_{56k}-*b*-$P4VP_{8k}$) were purchased from Polymer Source and used as polymer electrets. The volume fractions of the PS (f^{PS}) and P4VP (f^{P4VP}) blocks in PS_{56k}-*b*-$P4VP_{8k}$ were 0.88 and 0.12, respectively. Bare SiO_2/Si substrates were cleaned with deionized water, acetone and isopropyl alcohol for 20 min (each) in an ultrasonic bath and dried under flowing N_2 gas. Measured amounts of the PS_{56k}-*b*-$P4VP_{8k}$ powder were dissolved in toluene and stirred overnight to form homogeneous solutions. Micellar films of PS_{56k}-*b*-$P4VP_{8k}$ with various thicknesses on the wafer substrates were prepared through spin-coating (5000 rpm, 60 s) from toluene solutions of PS_{56k}-*b*-$P4VP_{8k}$ at concentrations in the range of 0.1–0.5 wt%. The BCP thin films were then placed in a chamber under vacuum (10^{-6} torr) at room temperature for 24 h to remove residual solvents. The thicknesses of the BCP thin films (charge-trapping layers) were measured using a Veeco Dektak 150 surface profilometer.

Atomic force microscopy

To observe the nanostructures and morphologies of the BCP and pentacene films, the surface of the thin films was characterized at room temperature using an atomic force microscope (Veeco diInnova or Nanoscope IIIa) operated in tapping mode and employing NANOSENSORS Si cantilevers (resonance frequency: 130 kHz); the scanning rate was 1 Hz and the image resolution was 512 × 512 pixels. AFM images of the BCP and pentacene films were recorded over scan areas of 1 μm × 1 μm and 2 μm × 2 μm, respectively.

Simultaneous grazing-incidence small-angle and wide-angle X-ray scattering

To characterize the nanostructures of the BCP films, GISAXS measurements were conducted at the BL23A SWAXS end station of the National Synchrotron Radiation Research Center in Taiwan. The angle of incidence of each X-ray beam (α_i) was 0.2°, set between the critical angles of the PS_{56k}-*b*-$P4VP_{8k}$ films ($\alpha_{c,f}$) and of the SiO_2/Si substrates ($\alpha_{c,s}$). The X-ray beam energy and the sample-to-detector distance were 6 keV and 2.9 m, respectively. The scattering vectors q_x and q_z in these patterns were calibrated using silver behenate. GISAXS profiles were obtained from the corresponding GISAXS images along the in-plane

direction q_x at the specular beam position; q_x and q_z are the components of the scattering wave vector (defined by $4\pi\lambda^{-1}\sin\theta$, with the scattering angle 2θ) in the in-plane and out-of-plane directions, respectively. 2D GISAXS patterns were recorded using an MAR CCD detector (frame size: 1024 pixels × 1024 pixels) positioned at the end of a vacuum flight tube. PEAKFIT software was used to fit the peak center (q) of the GIWAXS data in the first- and second-order diffraction peaks, employing a Gaussian + Lorenz area function to fit the model.

Device fabrication

A heavily doped n-type silicon (n^+-Si) wafer and a 200 nm thick thermally oxidized SiO_2 film were used as the gate and dielectric of the OFET memory, respectively. The SiO_2/Si substrates were cut into 2 × 2 cm^2 pieces by mechanical scribing. Prior to deposition, the substrates were cleaned with acetone and isopropanol in an ultrasonic bath. The pure PS_{56k}-*b*-$P4VP_{8k}$ diblock copolymers were dissolved in toluene at weight fractions in the range of 0.1–0.5 wt% and then spin-coated (5000 rpm, 60 s) onto the 200 nm thick SiO_2 layer (C_i = 17.275 nF cm^{-2}). The wafers were then quickly transferred to a vacuum chamber for deposition of the active layer. Films (thickness: 45 nm) of pentacene (Sigma-Aldrich; used without further purification) were deposited through thermal evaporation onto heavily doped thermally oxidized (100) Si substrates at a growth rate of 0.2 Å s^{-1} and a base pressure of 6 × 10^{-6} torr. Finally, 40 nm thick Au films were thermally evaporated onto the pentacene films through a shadow mask to form the S/D electrodes; the length and width of each channel were 250 and 2000 μm, respectively. The electrical characteristics of the devices were measured, using a Keithley 4200 semiconductor parameter analyzer, at room temperature under N_2 inside a glove box.

Results and discussion

Memory performance of pentacene-based OFETs that incorporate block copolymer thin films

Fig. 1 provides the schematic representation of the fabricated pentacene-based OFET memory devices (device structure: Si/SiO_2/PS_{56k}-*b*-$P4VP_{8k}$/pentacene/Au source–drain). We used a bottom gate/top contact configuration for our OFET devices, with films of PS_{56k}-*b*-$P4VP_{8k}$ of various layer thicknesses as charge trapping layers to tune the memory window for p-channel applications. Highly doped n-type Si (100) wafers were the substrates. A 200 nm thick SiO_2 layer as a gate dielectric was thermally grown onto the Si substrates. The diblock copolymer PS_{56k}-*b*-$P4VP_{8k}$ forms micellar structures when dissolved in toluene, due to preferential solubility of the nonpolar PS block in toluene, with the almost-insoluble P4VP block collapsing to form the cores of the micelles. When we evaporated the solvent, the consolidated PS_{56k}-*b*-$P4VP_{8k}$ thin film exhibited micellar morphology. Next, we rapidly transferred the wafer presenting the micellar film of the diblock copolymer to a vacuum chamber for deposition of a 45 nm thick pentacene layer (deposition rate: 0.2 Å s^{-1}). Finally, a 40 nm thick Au film was thermally evaporated onto the pentacene film

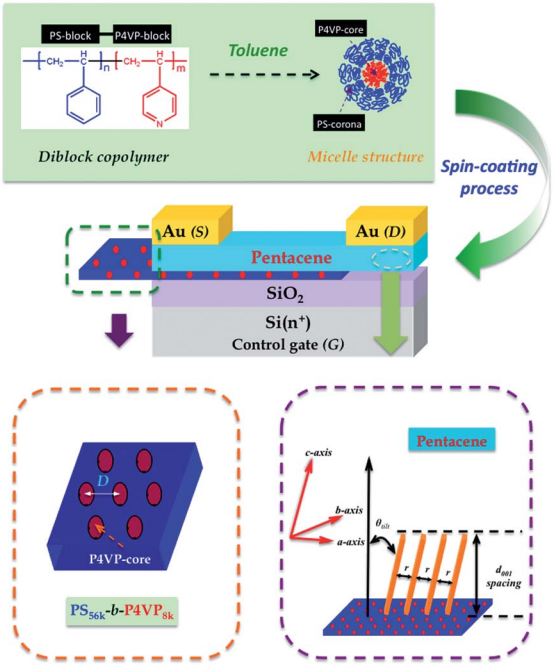

Fig. 1 Schematic representation of the structure of an OFET memory device incorporating a charge-trapping asymmetric PS_{56k}-*b*-$P4VP_{8k}$ copolymer layer possessing a micellar structure. The mean spacing (D) between the P4VP cores was determined from the GISAXS profiles. Schematic cross-sectional views of pentacene molecules reveal the herringbone structure along the *c* axis. The values of θ_{tilt} and the intermolecular distance r are defined.

through a shadow mask with a channel length (L) and width (W) of 250 and 2000 μm, respectively, to form the source and drain (S/D) electrodes. Further details concerning the fabrication of this device are described in the Experimental section. Fig. S1† presents the electrical output characteristics of the devices; Table 1 summarizes the electrical performance.

We obtained the OFET parameters—field-effect mobilities, on/off ratios (I_{on}/I_{off}), and threshold voltages (V_t)—for these devices by using eqn (1) in the saturation regime:[24,25]

$$I_{ds} = \frac{1}{2}\frac{W}{L}\mu_{FET}C_i(V_g - V_t)^2 \quad (1)$$

where I_{ds} is the S/D current, W is the width of the channel, L is the length of the channel, μ_{FET} is the field-effect mobility, C_i is the capacitance per unit area of the gate insulator, V_g is the gate voltage, and V_t is the threshold voltage. Fig. 2a–e present the V_t shifts in the transfer curves of the OFET-type memory devices incorporating various layer thicknesses of PS_{56k}-*b*-$P4VP_{8k}$ as charge trapping layers. We controlled the layer thicknesses of PS_{56k}-*b*-$P4VP_{8k}$ by varying the concentration of the polymer in solution; when we spun solutions of PS_{56k}-*b*-$P4VP_{8k}$ in toluene onto Si/SiO_2 substrates at concentrations of 0.1, 0.2, 0.3, 0.4, and 0.5 wt%, we obtained corresponding film thicknesses of 27, 32, 35, 52, and 60 nm, respectively, as determined from α-step measurements. These curves in Fig. 2 reveal reversible shifts in the value of V_t when a fixed forward and reverse V_g sweeps of ±60 V was applied *via* a relatively short switching time of 3 s. Based on the reversible shifts in V_t observed after two cycles of

Table 1 Measured fundamental OFET-type memory characteristics: field-effect mobility (μ_{FET}), on/off ratio (I_{on}/I_{off}), threshold voltage (V_t), V_t shift, amount of transferred charge (Δn), and thickness (t) of diblock copolymer films on the SiO_2 layers in OFET devices

	μ_{FET} ($cm^2\ V^{-1}\ s^{-1}$)	I_{on}/I_{off}	Initial V_t (V)	V_t shift (V)	Δn	t^a (nm)
Bare SiO_2	0.38 ± 0.01	10^5	−4.8 ± 0.8	Negligible	Negligible	0
PS_{56k}-*b*-$P4VP_{8k}$-0.1 wt%	0.46 ± 0.03	10^5	−1.5 ± 0.3	21.1 ± 0.3	2.28×10^{12}	27 ± 1.0
PS_{56k}-*b*-$P4VP_{8k}$-0.2 wt%	0.36 ± 0.06	10^5	−2.3 ± 0.6	18.0 ± 0.1	1.94×10^{12}	32 ± 0.3
PS_{56k}-*b*-$P4VP_{8k}$-0.3 wt%	0.31 ± 0.01	10^5	−4.2 ± 0.1	17.6 ± 0.2	1.90×10^{12}	35 ± 0.5
PS_{56k}-*b*-$P4VP_{8k}$-0.4 wt%	0.17 ± 0.06	10^5	−4.3 ± 0.7	12.5 ± 0.2	1.35×10^{12}	52 ± 0.7
PS_{56k}-*b*-$P4VP_{8k}$-0.5 wt%	0.10 ± 0.01	10^5	−4.4 ± 0.6	7.8 ± 0.3	0.84×10^{12}	60 ± 1.5

[a] The nine-blank-spaces method and the α-step were used to measure the thickness of the PS_{56k}-*b*-$P4VP_{8k}$ films.

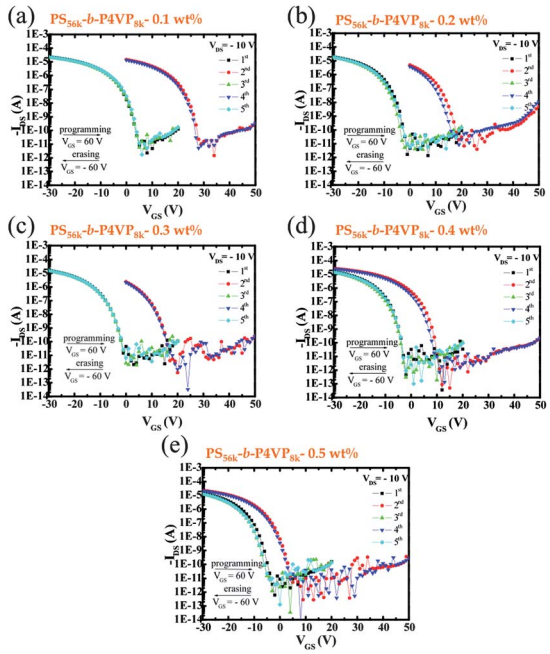

Fig. 2 Threshold voltage shifts in the transfer curves of OFET memory devices incorporating films of the charge-trapping PS_{56k}-*b*-$P4VP_{8k}$ copolymer that had been spun from toluene solutions at (a) 0.1, (b) 0.2, (c) 0.3, (d) 0.4, and (e) 0.5 wt%.

programming and erasing sweeps, we determined the characteristics of the ONVM devices. The values of V_t in these OFET devices could be controlled systemically and reversibly upon application of an appropriate external gate bias, causing a dramatic change in the drain current (I_d) by five orders of magnitude. Fig. S1a–e† display the output characteristics—plots of the S/D current (I_{ds}) with respect to the S/D voltage (V_{ds})—for our OFETs featuring various layer thicknesses of phase-separated PS_{56k}-*b*-$P4VP_{8k}$ as the charge trapping layer, with gate voltages (V_g) ranging from 0 to −10 V at the step of −2 V. All of these devices were subject to a programmed gate bias of +60 V and erasing gate bias of −60 V within a period of 3 s.

We observed no positive V_t shift in the bare SiO_2 device, indicating that the OFET lacking the PS_{56k}-*b*-$P4VP_{8k}$ layer did not trap any charge in the gate insulator. As indicated in Fig. 2a, when we inserted the 27 nm thick PS_{56k}-*b*-$P4VP_{8k}$ layer (from 0.1 wt% solution) between the pentacene and SiO_2 layers, the OFET threshold voltage shifted to the positive regime, with a value of the V_t shift of approximately 21 V. Moreover, Fig. 2b reveals that the presence of the 32 nm thick PS_{56k}-*b*-$P4VP_{8k}$ layer (from 0.2 wt% solution) between the pentacene and SiO_2 layers also caused the OFET threshold voltage to shift to the positive regime, with a value of the V_t shift of approximately 18 V, which is somewhat less than that of the device incorporating the 27 nm thick PS_{56k}-*b*-$P4VP_{8k}$ layer. Fig. 2c–e reveal that the V_t shifts in the devices incorporating the 35, 52, and 60 nm thick PS_{56k}-*b*-$P4VP_{8k}$ layers were 17.6, 12.5, and 7.8 V, respectively. Thus, the memory windows of these OFET memory devices decreased upon increasing the thickness of the incorporated PS_{56k}-*b*-$P4VP_{8k}$ layer, and we conclude that the memory window could be tuned by varying the thickness of the nanostructured PS_{56k}-*b*-$P4VP_{8k}$ as the charge trapping layer. We speculate that the memory effect of this device incorporating the asymmetric PS_{56k}-*b*-$P4VP_{8k}$ thin film was due to electron trapping by the P4VP domains in the PS matrix. Table 1 lists the measured values of the typical field-effect mobility (μ_{FET}), initial V_t, and I_{on}/I_{off}, as determined from the conventional characterization eqn (1) and the thickness (t) of the diblock copolymer films onto the SiO_2 layer in the OFET devices. We calculated the amount of transferred charge (Δn) from the shift in V_t after the programming process, according to the equation[26]

$$\Delta n = \frac{\Delta V_t C_i}{e} \quad (2)$$

where e, ΔV_t, and C_i are the element charge, the shift in V_t, and the capacitance of the gate dielectric, respectively. According to eqn (2), the amount of transferred charge was proportional to the threshold voltage shift and the capacitance of the gate dielectric. The amount of transferred charge indicated that the relative number of electrons that were trapped in the P4VP spheres of the PS matrix of the PS_{56k}-*b*-$P4VP_{8k}$ layer.

Table 1 indicates that both V_t shift and Δn decreased upon increasing the thickness of the PS_{56k}-*b*-$P4VP_{8k}$ layer, with the largest amount of transferred charge and the greatest threshold voltage shift being those for the device incorporating the 27 nm thick PS_{56k}-*b*-$P4VP_{8k}$ layer. In theory, increasing the thickness of the PS_{56k}-*b*-$P4VP_{8k}$ layer did not change the density of the P4VP domains in the film, but it did increase the absolute number of the P4VP domains because we used the same diblock copolymer in each case (mass ratio conservation). Note that the threshold voltage shift varies linearly with the reciprocal of the PS_{56k}-*b*-$P4VP_{8k}$ layer thickness. We suspect that this memory window

variation was due to the changes in the PS shell thickness that surrounds the P4VP core in the micellar PS_{56k}-b-$P4VP_{8k}$ layer when its layer thickness varied since the memory window was resulted from the relative number of charges that were trapped in the P4VP domains that are surrounded by the insulating PS shells. Moreover, the field-effect hole mobilities of the devices incorporating thin (27 nm) and thick (52 and 60 nm) PS_{56k}-*b*-$P4VP_{8k}$ layers were slightly larger and smaller, respectively, than those obtained without any block copolymer film, suggesting that the addition of PS_{56k}-*b*-$P4VP_{8k}$ layers of different thicknesses also affected the pentacene layer in these p-channel OFETs devices to some extent. Hence, to decipher the intricate micellar morphologies of the PS_{56k}-*b*-$P4VP_{8k}$ thin films, we used atomic force microscopy (AFM) and synchrotron small-angle X-ray scattering (SAXS) to probe the surface and internal structures of PS_{56k}-*b*-$P4VP_{8k}$ films, respectively, on SiO_2/Si substrates that had been processed under the same conditions as those used to prepare the OFET memory devices.

Micellar morphology of PS_{56k}-*b*-$P4VP_{8k}$ with various thicknesses on SiO_2/Si substrates

Fig. 3 presents AFM topographic images (1 μm × 1 μm) of PS_{56k}-*b*-$P4VP_{8k}$ films that had been spun onto bare SiO_2 substrates from solutions at concentrations from 0.1 to 0.5 wt%. Fig. 3a and b reveal ordered micelles in the PS_{56k}-*b*-$P4VP_{8k}$ films spun from 0.1 and 0.2 wt% solutions, respectively; Fig. 3c and d exhibit some disordering of the diblock copolymer micelle films deposited at 0.3 and 0.5 wt%, respectively. The spatial arrangements of the micelles went from ordered packing of large-diameter micelles with hexagonal order (0.1 wt%, Fig. 3a) to random spherical micelles of small-diameter micelles with closely packed density (0.5 wt%, Fig. 3d). The distance between the micelles decreased and the thickness of the PS_{56k}-*b*-$P4VP_{8k}$ layer increased upon increasing the concentration of the solution. No coalescence of the PS shell–P4VP core micelles to form ribbon-like nanostructures, through inter-micelle fusion, occurred in these thin films.[27] We identified two regimes for the polydispersity of the radius of micelles: (i) remaining small for micellar films less than 32 nm thick (spun from solutions having concentrations of less than 0.2 wt%), and (ii) remaining large for micellar films between 35 and 60 nm thick (when spun from solutions having concentrations of 0.3–0.5 wt%). The increase in the size distribution of the micelles was due to their deformation along the lateral direction. Fig. 3e presents the corresponding three-dimensional AFM image of the 32 nm thick PS_{56k}-*b*-$P4VP_{8k}$ film that had been spun from the 0.2 wt% solution and reveals that the height of the relief microstructures was approximately 30 nm. We assume that the bottom of each truncated micelle formed a quasi-two-dimensional circular mat, whereas the upper half retained a hemispherical cap shape. A circular mat looped around each hemisphere; we suspected that it comprised mainly PS chains, with each micelle still being composed of a P4VP core and a PS shell. For gaining an understanding of the larger representative structures (several square millimeters) in these layers and being similar to the device structure, we also elucidated the internal structures of the PS_{56k}-*b*-$P4VP_{8k}$ layers and the molecular packing of the pentacene layers on the PS_{56k}-*b*-$P4VP_{8k}$ layers through simultaneous synchrotron GISAXS and GIWAXS analyses, respectively. In this way, we can correlate the packing of pentacene directly to the surface structure of the PS_{56k}-*b*-$P4VP_{8k}$ layer. Fig. 4 displays the schematic drawing of the set-up for simultaneous synchrotron GISAXS and GIWAXS analyses of the pentacene–PS_{56k}-*b*-$P4VP_{8k}$ bilayer samples that are deposited on the SiO_2/Si substrate, with the thicknesses and processing conditions of both layers resembling those used in OFET memory devices.

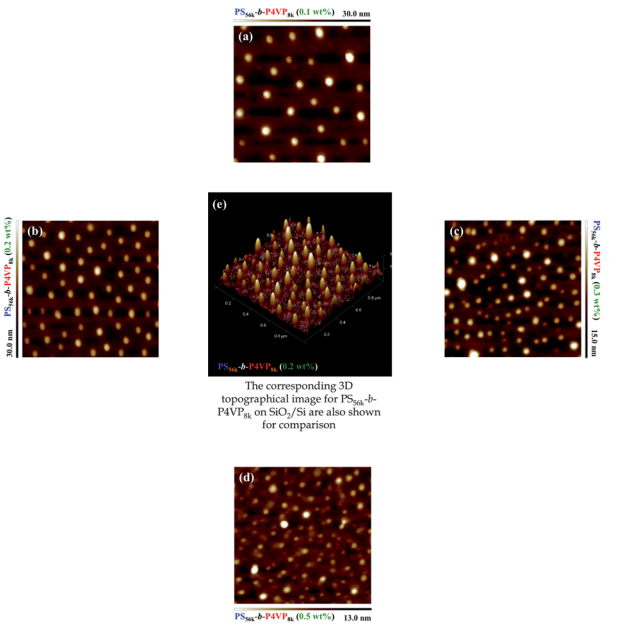

Fig. 3 (a–d) Representative AFM images (1 μm × 1 μm) of PS_{56k}-*b*-$P4VP_{8k}$ films on SiO_2/Si substrates, spun from toluene solutions at concentrations of (a) 0.1, (b) 0.2, (c) 0.3, and (d) 0.5 wt%. Bright spots (local highlands) represent P4VP cores. (e) Center image, 3D AFM tomography of the as-spun PS_{56k}-*b*-$P4VP_{8k}$ film obtained from the 0.2 wt% polymer solution, revealing the real space of ordered micelles, having a quasi-2D circular mat structure and a hemispherical cap shape, on the surface of a homogeneous layer of PS_{56k}-*b*-$P4VP_{8k}$ chains anchored to the SiO_2/Si substrate.

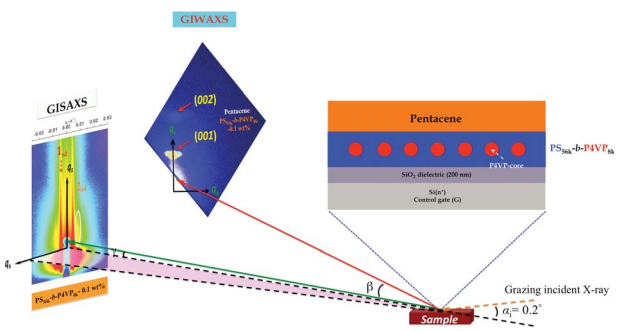

Fig. 4 Schematic representation of the simultaneous GISAXS and GIWAXS set-up; q_z and q_x denote X-ray scattering in the out-of-plane and in-plane directions, respectively. The sample is placed horizontally and the angle of incidence (α_i) is 0.2°. A two-dimensional detector collects the small-angle scattered intensity, and an image plate detector collects the wide-angle scatter intensity.

Fig. 5a–e display two-dimensional (2D) GISAXS patterns of the PS_{56k}-*b*-$P4VP_{8k}$ layer in the bilayer samples. These 2D GISAXS patterns did not feature any ring-band scattering characteristics of monodisperse full spheres on a solid, excluding the possibility of the existence of monodisperse full spheres. In addition, no Kiessig fringes,[28] which are associated with resonant diffuse scattering, were evident in the 2D GISAXS patterns of these PS_{56k}-*b*-$P4VP_{8k}$ films, indicating the absence of interfacial correlation at both interfaces of the PS_{56k}-*b*-$P4VP_{8k}$ films. This absence of correlated interfaces indicates that the roughness at the free surface of the micellar films was dominated only by the hemispherical-cap contour of the truncated spheres, and not by the underlying SiO_2/Si substrate.[29] Fig. 5a also reveals two symmetric sets of narrow Bragg diffraction streaks parallel to the q_z direction in the 2D GISAXS pattern of the 27 nm thick PS_{56k}-*b*-$P4VP_{8k}$ film that had been spun from the solution at 0.1 wt%, indicating the existence of a monolayer of micelles with long-range hexagonal order on the substrates. Moreover, Fig. 5b–e reveal that the intensity of the inclined diffuse scattering rods in the GISAXS patterns of the PS_{56k}-*b*-$P4VP_{8k}$ films gradually weakened upon increasing film thickness from 32 to 60 nm (the solution concentration from 0.2 to 0.5 wt%); we ascribe this weakening to the shape and size variations of the micelles, caused by their deformation along the lateral direction. These results are consistent with the AFM topographic images in Fig. 3c and d. Fig. 5f reveals the hierarchical arrangement of the PS and P4VP phases in the PS_{56k}-*b*-$P4VP_{8k}$ layers obtained from the corresponding in-plane GISAXS profiles, which feature peaks that are consistent with those expected for 2D hexagonal packing (*i.e.*, a peak position ratio of $1 : 3^{1/2} : 2$ for the first three peaks).[30] The Bragg diffraction streaks in the in-plane GISAXS profiles shifted continuously to larger values of q_x upon increasing the layer thickness (or the concentration of the spun solution).

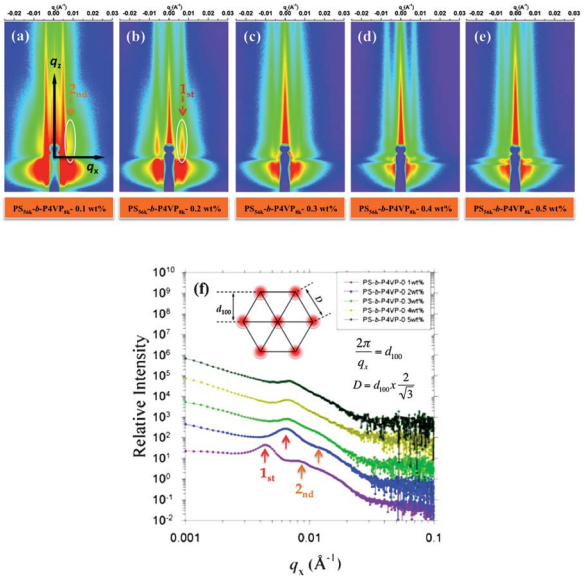

Fig. 5 (a–e) Measured 2D GISAXS patterns of micelles on SiO_2/Si substrates spun from toluene solutions containing PS_{56k}-*b*-$P4VP_{8k}$ at concentrations of (a) 0.1, (b) 0.2, (c) 0.3, (d) 0.4, and (e) 0.5 wt%. (f) In-plane GISAXS profiles for films of the PS_{56k}-*b*-$P4VP_{8k}$ layer, deposited at concentrations of 0.1, 0.2, 0.3, 0.4, and 0.5 wt%. Red and orange arrows indicate selective scattering peaks from the hexagonally ordered copolymer micelle cores in the lower-q_x region. Curves were analyzed using a 2D hexagonal lattice function. Inset: equations for calculating the mean spacing (D) in 2D hexagonal lattice.

We estimated the mean spacings [$D = (4/3)^{1/2} d_{100}$] between the P4VP cores in the 27 and 32 nm thick PS_{56k}-*b*-$P4VP_{8k}$ films from their first peak positions (q_x = 0.00435 and 0.00653 Å^{-1}, respectively) to be approximately 167 and 111 nm, respectively. This shift indicates a decrease in the inter-micelle spacing between the P4VP cores in the PS phase upon increasing the thickness of these layers, consistent with the topographic AFM images in Fig. 3a and b. Fig. 5f also reveals that the Bragg diffraction streaks for the 35–60 nm thick PS_{56k}-*b*-$P4VP_{8k}$ films remained at about the same position (q_x = 0.00653–0.00681 Å^{-1}), indicating that the values of D (108–106 nm) and the structures of the PS_{56k}-*b*-$P4VP_{8k}$ micelles were relatively insensitive to the change in the film thickness.[31] These values of the mean spacing D were significantly lower than that for the 27 nm thick PS_{56k}-*b*-$P4VP_{8k}$ film. Hence, further increases in the layer thickness from 35 nm to 52 nm led to greater superposition of the ring-banded maps, consequently increasing the thickness of the sub-layer that consists of free PS_{56k}-*b*-$P4VP_{8k}$ chains at the SiO_2/Si substrate interface and decreasing the distance between the micelles.

Structural characteristics of the pentacene molecules on the PS_{56k}-*b*-$P4VP_{8k}$ layer

To determine the effect of the PS_{56k}-*b*-$P4VP_{8k}$ layer on the molecular packing of the pentacene film deposited upon it, we performed GIWAXS analyses of samples having the configuration pentacene/PS_{56k}-*b*-$P4VP_{8k}$/SiO_2/Si, as shown in Fig. 4. Fig. 6 displays 2D GIWAXS patterns for the deposited pentacene layers, with q_z and q_x denoting X-ray scattering in the out-of-plane and in-plane directions, respectively. The scattering intensity in the out-of-plane direction, $I(q_z)$, for the pentacene films deposited on PS_{56k}-*b*-$P4VP_{8k}$ layers of various thicknesses was recorded with an image of the reciprocal space (q-space) of the sample surface using an image plate detector.[32] The presence of only (001) and (002) reflections (at q_z = 4.15 and 8.55 nm^{-1}, respectively) in the X-ray diffraction patterns of the deposited pentacene layer (thickness: *ca.* 45 nm) on PS_{56k}-*b*-$P4VP_{8k}$ layers on SiO_2/Si substrates indicated that the pentacene molecules were slightly tilted from the out-of-plane direction, *c*-axis, and that the pentacene crystals in the thin films were oriented with their (001) and (002) planes parallel to the surface of the PS_{56k}-*b*-$P4VP_{8k}$ layers.[33,34] All peaks corresponding to (00l, l = 1, 2) planes arose from the packing of pentacene molecules in the thin film phase, characterized by an interplanar spacing d_{001} of 15.4 ± 0.4 Å in the pentacene films. Furthermore, we did not observe any triclinic bulk phase of pentacene, which would have exhibited a vertical periodicity of 14.5 Å, in our GIWAXS profiles.[35]

Fig. 6g reveals that the pentacene films that had been deposited on the PS_{56k}-*b*-$P4VP_{8k}$ films processed from solutions having concentrations of 0.1–0.3 and 0.4–0.5 wt% exhibited higher and lower first-order diffraction peak intensities,

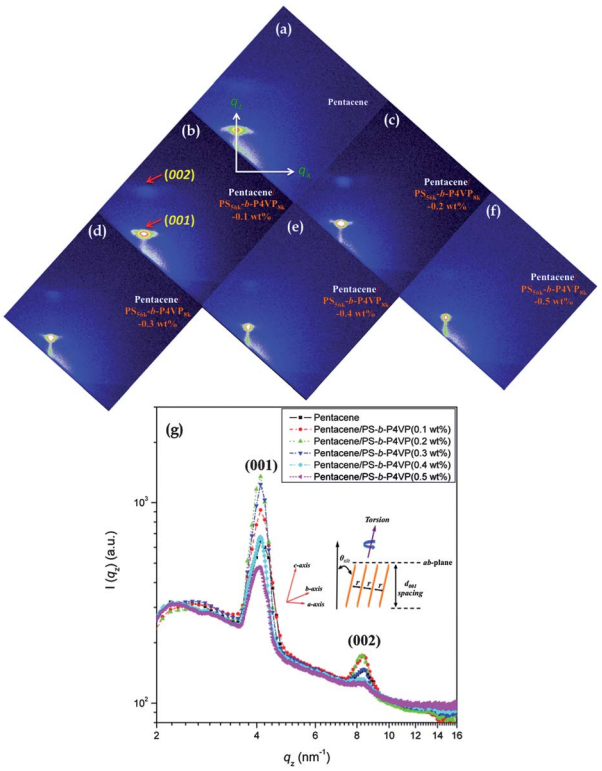

Fig. 6 Out-of-plane GIWAXS 2D patterns of pentacene on PS_{56k}-*b*-$P4VP_{8k}$ films on SiO_2/Si substrates, spun from toluene solutions containing micelles at concentrations of (b) 0.1, (c) 0.2, (d) 0.3, (e) 0.4, and (f) 0.5 wt%. In (a), q_x and q_z are the in-plane and out-of-plane components of the momentum transfer vector q, respectively. The (001) and (002) reflections of the pentacene, located at values of q_z of 4.15 and 8.55 nm^{-1}, respectively, represent the degrees of packing of the pentacene molecules in the thin films.

respectively, than those of the pentacene films that had been deposited directly on the SiO_2/Si substrate. The torsion angle, in the *ab* plane, as determined by the shape of the 2D scattering pattern, between pentacene molecules decreased upon increasing the PS_{56k}-*b*-$P4VP_{8k}$ layer thickness, leading to less-ordered packing in the deposited pentacene layer, as revealed by comparing Fig. 6b and f (from elliptic to circular shape scattering pattern). The similar values of d_{001} imply similar packing of pentacene molecules in the *ab* plane, which is regarded as the high-mobility plane for hole transport in pentacene-based OFETs. Furthermore, the tilt angle (θ_{tilt}) of the pentacene molecules, from the *c*-axis toward the *a*-axis determined by the peak position, was almost constant (all (001) peaks located at $q_z = 4.15$ nm^{-1}) for the pentacene layer deposited on the PS_{56k}-*b*-$P4VP_{8k}$ layers processed from solutions at concentrations of 0.1–0.4 wt%. Notably, however, the value of θ_{tilt} obtained from the 0.5 wt% solution was different because of the presence of a small component of a second phase (at $q_z = 4.28$ nm^{-1}), being similar to those from our GIWAXS profiles of pentacene in the absence of a PS_{56k}-*b*-$P4VP_{8k}$ film. Thus, the packing of the pentacene units in our system was dominated more by the torsion angle than by θ_{tilt}.

Fig. 7 presents AFM images of pentacene films on PS_{56k}-*b*-$P4VP_{8k}$ layers of various thicknesses on SiO_2/Si substrates. Fig. 7a displays a pentacene film deposited through thermal evaporation onto a heavily doped thermally oxidized (100) Si substrate.[36] This 2 μm × 2 μm scan reveals a highly textured film with large dendritic grains extending over several microns, whereas Fig. 7b–f reveal that the grains of the pentacene films on the PS_{56k}-*b*-$P4VP_{8k}$ layers tended to be smaller than those of pentacene films on bare SiO_2/Si substrates. In particular, the grain sizes in the pentacene film on the 27 nm thick PS_{56k}-*b*-$P4VP_{8k}$ film were smaller than those on the bare SiO_2 and the 32–60 nm thick PS_{56k}-*b*-$P4VP_{8k}$ films. From Table 1, however, the highest value of μ_{FET} was that measured from the device incorporating the 27 nm thick PS_{56k}-*b*-$P4VP_{8k}$ layer, with the hole mobility decreasing upon increasing the layer thickness. This order of the hole mobilities might not have been due only to the transferred morphology of pentacene onto the PS_{56k}-*b*-$P4VP_{8k}$ layers. The structural quality of the organic semiconductor is a key parameter toward achieving a high field-effect mobility,[37] with the conducting channel appearing within the first several molecular monolayers close to the organic semiconductor–insulating layer interface.[38] The literature suggests that the values of μ_{FET} should be limited by the sum of the surface density of traps at the grain boundaries (N_{bound}) and the surface density of traps at the organic–insulating layer interface (N_{OI}), with the degree of charge trapping in the channel region dominated not by the grain boundaries but by the organic–insulating layer interface.[39] In such a case, the value of μ_{FET} would be more independent of the grain size; indeed, this phenomenon is evident in Fig. 7c–f. Comparing the OFETs incorporating 35–60 nm thick PS_{56k}-*b*-$P4VP_{8k}$ layers to those incorporating 27–32 nm thick PS_{56k}-*b*-$P4VP_{8k}$ layers, we observe that the value of μ_{FET} was smaller for the former, but the grain

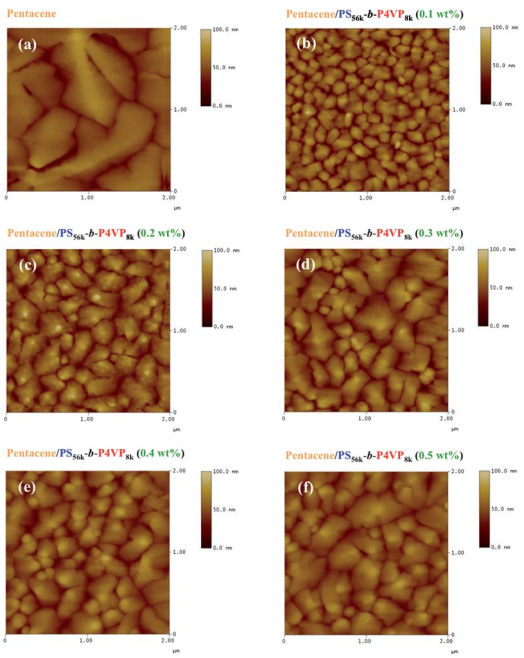

Fig. 7 2 μm × 2 μm AFM topographic images of (a) pentacene on SiO_2/Si substrates and pentacene on micellar PS_{56k}-*b*-$P4VP_{8k}$ layers spun from solutions at concentrations (b) 0.1, (c) 0.2, (d) 0.3, (e) 0.4, and (f) 0.5 wt%.

size was slightly larger, implying N_{bound} remained much lower than N_{OI}. In some cases, OFETs with smaller pentacene grain sizes exhibit greater values of μ_{FET} owing to the fact that the surface energy of the underneath layer appeared to strongly influence the morphology of pentacene films and the growth mode. For example, Stranski–Krastanov growth with large, dendritic pentacene grains occurred at high surface energy, whereas three-dimensional (3D) island growth with small pentacene grains occurred at low surface energy; the carrier mobility of OFETs with small, 3D pentacene grains was higher than that of corresponding OFETs with large, terrace-structured grains.[40]

For our present series of thin pentacene films on PS_{56k}-*b*-$P4VP_{8k}$ layers with various thicknesses, we find that pentacene growth on the high-surface-energy SiO_2 dielectrics resulted in large, dendritic grains, whereas that on the low-surface-energy PS_{56k}-*b*-$P4VP_{8k}$ layer led to interconnection between the pentacene grains, with gradual lateral growth of the grains causing the vacant spaces between the grains to be filled. Hence, the higher mobility of the OFETs incorporating the low-surface-energy 27 nm thick PS_{56k}-*b*-$P4VP_{8k}$ trapping layer might have been achieved as a result of the interconnection of and tight packing between pentacene grains. This result is in agreement with previous literature where some groups have reported that self-assembled monolayer formation on SiO_2 can lead to OFET devices featuring pentacene films with smaller grain sizes and exhibiting improved carrier mobility.[41,42] Although the pentacene films on the thicker PS_{56k}-*b*-$P4VP_{8k}$ layers that had been prepared at 0.2–0.5 wt% featured larger grain sizes, the corresponding carrier mobilities were lower. We suspect that the large voids and incomplete layers in the pentacene layer over the thicker PS_{56k}-*b*-$P4VP_{8k}$ layer could limit the transport of charge carriers and decrease the carrier mobility, despite the formation of larger grains in the pentacene films on the thicker PS_{56k}-*b*-$P4VP_{8k}$ films. In our system, the relationship between the grain size of the pentacene film on the PS_{56k}-*b*-$P4VP_{8k}$ layer was dominated by the ordering of micelles, which results in increased realignment in intermolecular ordering of pentacene that has a tilt angle to the perpendicular direction to the surface of the PS_{56k}-*b*-$P4VP_{8k}$ films. Upon increasing the layer thickness, however, the degree of realignment of pentacene molecules decreased because of the limited torsion angle. The greater degree of torsion between the pentacene molecules resulted in the enhanced molecular packing of the pentacene films on the PS_{56k}-*b*-$P4VP_{8k}$ layers that we prepared. These results indicate that the surface energy of the PS_{56k}-*b*-$P4VP_{8k}$ charge trapping layer can dominate the structure of the pentacene layer.

Fig. 8a and b present schematic representations of the structure of the pentacene–PS_{56k}-*b*-$P4VP_{8k}$ bilayer on SiO_2/Si with a thin and a thick PS_{56k}-*b*-$P4VP_{8k}$ layer, respectively. From the GISAXS results and AFM images, we conclude that, for these PS_{56k}-*b*-$P4VP_{8k}$ micelles on SiO_2/Si substrates, the mean radius (R) of P4VP cores remained approximately constant, while the inter-micelle spacing and their height (H) decreased and the thickness of the homogeneous layer (L) increased upon increasing the layer thickness (concentration of the spun solution). Moreover, Fig. 8a and b reveal several prominent features

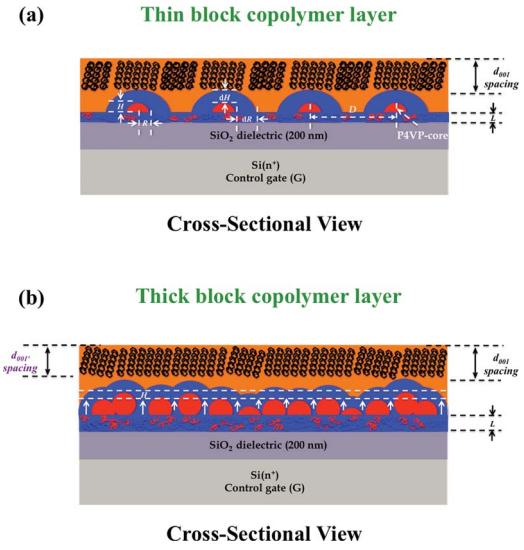

Fig. 8 Schematic illustrations of (a) pentacene on a thin micellar PS_{56k}-*b*-$P4VP_{8k}$ layer and (b) pentacene on a thick micellar PS_{56k}-*b*-$P4VP_{8k}$ layer. The PS_{56k}-*b*-$P4VP_{8k}$ layer consists of P4VP core–PS shell micelles on top of a homogeneous layer of free PS_{56k}-*b*-$P4VP_{8k}$ chains anchored to SiO_2/Si substrates. Labels dR, dH, L, and D denote respectively the thicknesses of PS shells in the normal and parallel directions to the substrates, the thickness of a homogeneous layer underneath the micelles, and the mean spacing between the neighboring two P4VP-cores, respectively.

in the detailed micellar structure. First, the PS shells had anisotropic thickness; the PS shell thickness normal to the substrate (dH) remained nearly unchanged, whereas that along the substrate (dR) decreased upon increasing the thickness of the film. Fig. 8a represents such an ordered PS_{56k}-*b*-$P4VP_{8k}$ micellar thin layer structure, while Fig. 8b shows that the hemispherical caps of micelles were in contact with their neighbors and forced themselves into strings and disordered domains for a thick PS_{56k}-*b*-$P4VP_{8k}$ layer. The coexistence of these features accounts for the increased disorder of the core–shell micelles in the PS_{56k}-*b*-$P4VP_{8k}$ films and, as a result, the morphology of a dense monolayer of PS shell–P4VP core micelles resembled a monolayer of bumps placed on a thick continuous layer. More importantly, the close arrangement of these micelles leads to a reduced PS shell thickness, dR, between the neighboring two micelles along the substrate, which is serving as a barrier for retaining the trapped charges. Accordingly, this reduced PS shell thickness along the substrate direction mainly accounts for the decreased memory window of the OFET memory devices incorporating the PS_{56k}-*b*-$P4VP_{8k}$ layers upon increasing the film thickness because the ability of the P4VP core to retain the trapped charges deteriorated as charges can readily tunnel through a thinner PS shell. Specifically, the memory window decreased substantially from 21 to 7.8 V for the PS_{56k}-*b*-$P4VP_{8k}$ films that had layer thicknesses of 27 and 60 nm, respectively. For a PS_{56k}-*b*-$P4VP_{8k}$ layer spun from a solution having a concentration of less than 0.1 wt% (*i.e.*, thinner than 27 nm), incomplete surface coverage (pin holes) of the SiO_2 layer will result, making it unsuitable as a trapping layer. Fig. 9 presents the non-volatile memory application; the measurements of the program/erase speed and the retention time of our device were carried out. Fig. 9a and b presents the

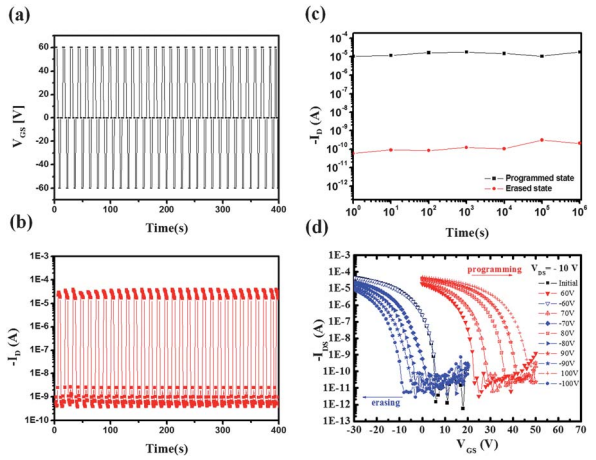

Fig. 9 (a) Program/erase bias pulses of ±60 V were repeatedly applied to the bottom-gate electrode for 5 s (programming: $V_g = 60$ V and $V_d = -10$ V and erasing: $V_g = -60$ V and $V_d = -10$ V). (b) Reversible switching of a pentacene OFET memory utilizing the 27 nm thick PS_{56k}-*b*-$P4VP_{8k}$ film for on- and off-current states. (c) The retention time for the 27 nm thick PS_{56k}-*b*-$P4VP_{8k}$ memory device in the programmed/erased states under ambient conditions at room temperature. The dotted line is an extrapolation of the measured data for the retention capability to determine the long-term reliability of the memory devices. (d) Shifts in transfer curves at $V_d = -10$ V for the 27 nm thick PS_{56k}-*b*-$P4VP_{8k}$ OFET memory device, where $V_g = 60$, 70, 80, 90, 100 V and $V_g = -60$, −70, −80, −90, −100 V were applied for 3 s for programming and erasing, respectively.

reversible switching behavior of a pentacene OFET memory utilizing 27 nm thick PS_{56k}-*b*-$P4VP_{8k}$, in a series of programming and erasing processes. The retention time of the shifted characteristics after programming and erasing operations is presented in Fig. 9c; the curves in Fig. 9c indicate that the retention time is more than 10^6 s, which is our experiment duration, with the on/off ratio maintained at 10^5. At the same time, the effects of different programmed/erased voltages on the 27 nm thick PS_{56k}-*b*-$P4VP_{8k}$ memory cell are displayed in Fig. 9d, which shows that the memory window increases with the programmed voltages, indicating its good potential for applications.

Conclusions

The memory windows in OFET-type memory devices for p-channel applications can be tuned through varying the thickness of an incorporated PS_{56k}-*b*-$P4VP_{8k}$ micellar layer, merely by varying the concentration of its deposition solution. The P4VP core–PS shell micelles retained their cap-like structures, with the distance between them decreasing upon increasing the layer thickness of the PS_{56k}-*b*-$P4VP_{8k}$ film; in contrast, the thickness of the PS shell along the in-plane direction decreased substantially, resulting in a decrease in the electron trapping ability of the PS_{56k}-*b*-$P4VP_{8k}$ layers and the memory window of the devices. In addition, the molecular packing and torsion angles of pentacene films formed on the PS_{56k}-*b*-$P4VP_{8k}$ films were all strongly affected by the thickness of the underlying PS_{56k}-*b*-$P4VP_{8k}$ micellar layer. The relationship between the grain sizes in the pentacene films and the thickness of the PS_{56k}-*b*-$P4VP_{8k}$ films was dominated by the ordering of the packing of the spherical micelles, due to increased realignment in the intermolecular ordering perpendicular to the surface of the film as a result of the torsion of the pentacene molecules.

Acknowledgements

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