Perturbation On-Time (POT) Technique in Power Factor Correction (PFC) Controller for Low Total Harmonic Distortion and High Power Factor

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***Abstract*—The proposed perturbation on-time technique suppresses total harmonic distortion (THD) and, thus, improves the power factor in the power factor correction (PFC) controller. Besides, the adaptive control of the minimum off time by the proposed inhibit time control can improve efficiency even at low ac input voltage. Therefore, highly integrated PFC converter fabricated in the TSMC 800-V ultrahigh voltage process can achieve low THD of 6%, high PF of 99%, and high efficiency of 95% at the output power of 90 W.**

***Index Terms*—Inhibit time (IT) control, nonnegative-voltage zero current detector (NNV-ZCD), perturbation on time (POT), power factor correction (PFC), ultrahigh voltage (UHV).**

I. Introduction

THE input line current is basically shaped by the power factor correction (PFC) controller to be the replica of the input line voltage and exactly in phase with it. If the value of the power factor (PF) is not 100%, it results in power losses, harmonics that travel down the neutral line, and disruption of other devices connected to the line. Therefore, today's electrical equipment must comply with the European Norm EN61000−3−2, which applies to most electrical appliances with an input power of 80 W or greater. Conventional passive PFC techniques with large external inductors and capacitors only achieve a PF of about 75%. This PF cannot meet the requirement of EN61000−3−2. In other words, the implementation of an active PFC controller in today's power equipment is necessary to comply with regulatory requirements.

The conventional PFC as depicted in Fig. 1 uses the boost topology with the boundary conduction mode (BCM) technique [1]–[5] to guarantee high PF value due to the in-phase line voltage and inductor currents. The conventional BCM technique can simplify circuit complexity but have high root-mean-square (rms) current in the inductor. In the conventional BCM technique, the error amplifier (EA) can set up the output power level through the error signal $V_{\rm EAO}$. The comparator compares the saw-tooth signal with $V_{\rm EAO}$ to determine the on-time period. On the other hand, the off-time period is determined by the detection of the zero inductor current. That is, the power N-type MOSFET is inherently turned ON with a zero current switching (ZCS) mechanism. The switching loss is effectively decreased because the diode reverse recovery is eliminated. Therefore, an accurate zero current detection (ZCD) circuit is needed in the ZCS operation for high efficiency. Here, the energy in the auxiliary windings can be used to find the zero current condition by the ZCD circuit in order to avoid facing ultrahigh voltage (UHV). The ZCD circuit will detect the zero inductor current from the auxiliary windings through the signal $V_{\rm DET}$ to trigger the set-reset (SR) latch high to restart the next switching cycle.

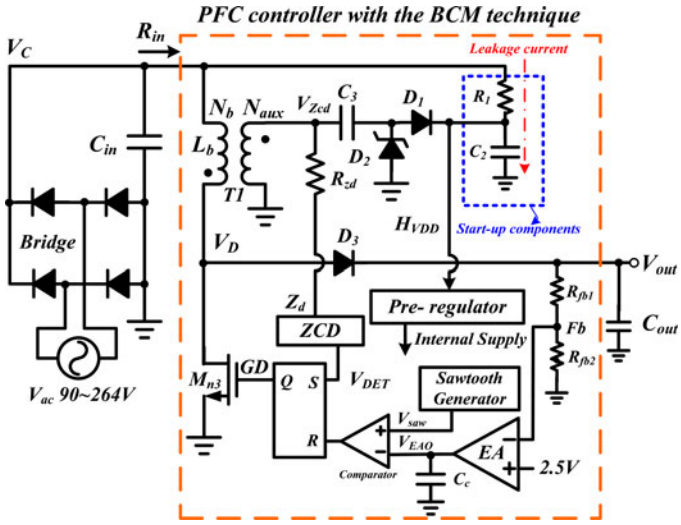

Fig. 1. Conventional PFC architecture with the BCM control technique.

Thus, the auxiliary windings with the number of $N_{\rm aux}$ turns are used to detect the zero inductor current if primary windings with the number of N_b turns have an equivalent inductor value of L_b. Once the power N-type MOSFET is turned ON, the inductor current $i_{\rm Lb}$ is equal to the line current $i_{\rm ac}$ shown in (1), which is proportional to the product of the line voltage $V_{\rm ac}$ and the on-time value $t_{\rm on}$

$$i_{L_b} = i_{\rm ac} = \frac{V_c}{L_b} \cdot t_{\rm on} \text{ where } V_c = |V_m \sin \omega t| . \quad (1)$$

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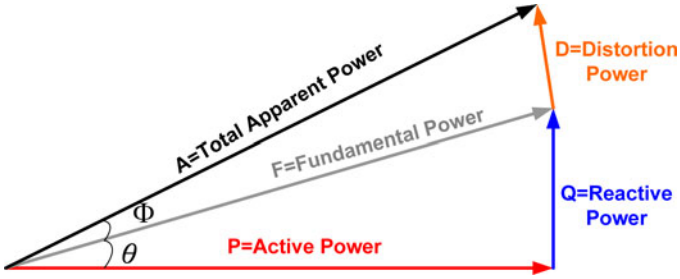

Fig. 2. Relationship between active power, reactive power, and distortion power.

V_c is the voltage across the input capacitor $C_{\rm in}$ and V_m is the peak value of the input ac source. Therefore, if the values of V_m, L_b, and $t_{\rm on}$ are constant, the line current will be in phase with the line voltage as expressed in (2) with a constant M

$$i_{\rm ac} = M \cdot \sin \omega t \text{ where } M = \frac{V_m \cdot t_{on}}{L_b}. \tag{2}$$

Through the control of the inductor current $i_{\rm Lb}$, the in-phase characteristic between line voltage and line current can be guaranteed to achieve high PF value. As a result, the fix on-time control is adopted by the conventional PFC controller to modulate the input resistance seen at the ac source nearly equal to a constant value [6]–[10].

As illustrated in (3), PF value is not only determined by the value of cos θ, which is decided by the angle between line voltage and current, but also by the value of cosΦ, which is affected by the total harmonic distortion (THD) value

$$\text{PF} = \cos\theta \cos\Phi = \frac{P}{A} \text{ and } \text{THD} = \frac{D}{F} = \tan\Phi. \tag{3}$$

P is the active power, A is the total apparent power, D is distortion power, and F is the fundamental power. In conventional active PFC controller design, the target of in-phase line voltage and current simply ensures the value cos θ is equal to 1. That is, the reactive power can be reduced to zero by controlling the line current and ensure it is in phase with the line voltage. However, the THD value will still deteriorate the PF value owing to the existence of distortion power. Fig. 2 depicts the relationship among active power, reactive power, and distortion power. Obviously, the reduction in THD becomes more important if high PF is demanded in a high-quality power delivery system. Specifically, minimized THD results in a small angle of Φ and a low distortion power. Therefore, in this paper, the proposed active PFC controller not only reduces the value of θ through the in-phase line voltage and current, but also reduces the value of THD through the perturbation on-time (POT) technique. Besides, the minimum off time is also adaptively adjusted by the proposed inhibit time (IT) control for high efficiency to reduce power consumption effectively even at low ac input voltage.

The organization of this paper is as follows. Section II introduces the design concept based on the PF and the THD. Section III introduces the architecture of the proposed PFC technique with POT and IT controllers. The circuit implementation is shown in Section IV. Experimental results are shown in Section V. Finally, a conclusion is made in Section VI.

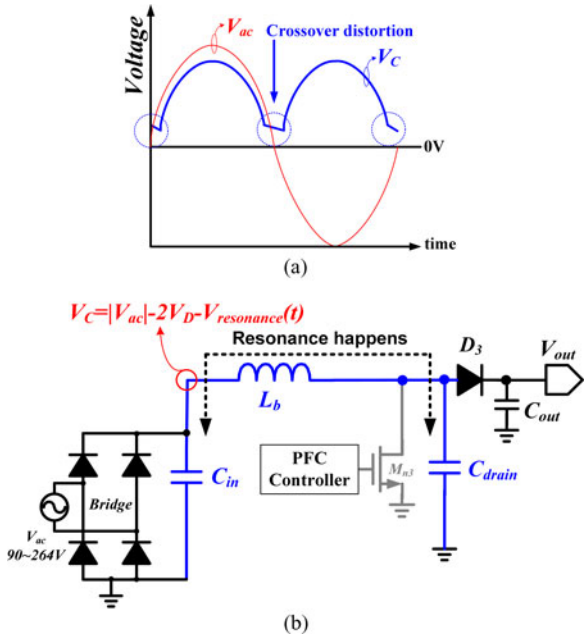

Fig. 3. (a) Crossover distortion of V_c. (b) Parasitic resonant path.

II. Design Concept Based on the PF and the THD

Fig. 3 shows that how the PF and the THD are deteriorated. At first, the residual charge stored in $C_{\rm in}$ results in a large voltage V_C across $C_{\rm in}$. $C_{\rm in}$ cannot be charged since nonzero voltage at V_C results in the diodes of the bridge work in the reverse-biasing condition if the input line voltage is lower than V_C. That is, large V_C value will block the line current flowing from the ac source to charge $C_{\rm in}$. Thus, the PF will be deteriorated due to no conduction angle, which is referred to as "crossover distortion." Crossover distortion cannot be eliminated completely even with $C_{\rm in} = 0$ owing to the diode forward voltage V_D of the bridge rectifier. Crossover distortion around the origin will make the phase shift between line voltage and current similar to the sudden rise of input equivalent resistance. After passing through the origin area, the system will return to in phase by the PFC system. Certainly, the flat portion in the line current anticipates and deteriorates the THD.

Due to the finite $C_{\rm in}$ and V_D, V_C will be distorted as depicted in Fig. 3(a). Without discharging the charge on V_C, the energy stored in the inductor cannot be transferred to the output. Fig. 4(a) shows V_C around the zero crossing with different $C_{\rm in}$ values if the power N-type MOSFET capacitance is neglected. V_C strays from the ideal haversine when the line phase angle is $\Phi_{C\,\rm in}$ radians away from π. The input equivalent circuits of the PFC just look like a parallel connection of a resistor and a capacitor as shown in Fig. 1. The input current can be derived as follows:

$$i_{\rm ac} = \left(j \cdot \omega \cdot C_{\rm in} + \frac{1}{R_{\rm in}}\right) \cdot V_{\rm ac} = \left(j \cdot 2\pi f_L \cdot C_{\rm in} + \frac{1}{R_{\rm in}}\right) \cdot V_{\rm ac}. \tag{4}$$

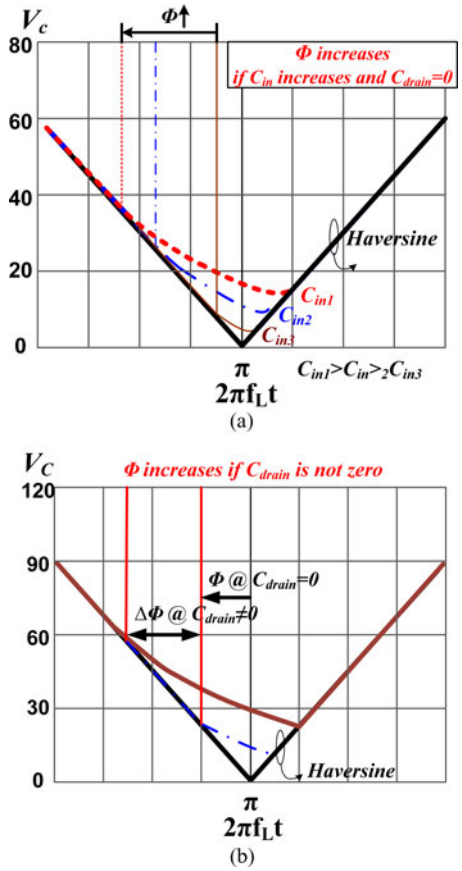

Fig. 4. Crossover distortion effect around the zero-crossing when (a) different value of $C_{\rm in}$ is used and (b) larger $C_{\rm drain}$ is used.

The expression of $\Phi_{C\,\rm in}$ is shown as follows:

$$\Phi_{C\rm in} \approx \tan\Phi_{C\rm in} = 2\cdot\pi\cdot f_L\cdot C_{\rm in}\cdot R_{\rm in},\ \text{where}\ R_{\rm in} = \frac{V_{\rm ac}^2}{P_{\rm in}} \tag{5}$$

where f_L is the line frequency, $R_{\rm in}$ is the equivalent large-signal resistance seen from the PFC controller input, $V_{\rm ac}$ is the line voltage, and $P_{\rm in}$ is the input power of the PFC controller. The voltage on $C_{\rm in}$ will stray from the haversine slightly after the line phase angle equals $\pi - \Phi_{C\,\rm in}$ depending on how much $R_{\rm in}$ increases.

Secondly, in Fig. 3(b), the THD will become larger owing to the resonant circuit formed by L_b, $C_{\rm in}$, and the drain capacitance $C_{\rm drain}$ (which includes power N-type MOSFET parasitic capacitance, boost inductor's parasitic capacitance, and boost diode's junction capacitance). The lack of energy transfer from input to output close to the zero crossings of the line voltage worsens crossover distortions and, thus, deteriorates THD. The energy that can be stored in the boost inductor is very low near zero crossings, not enough to charge the total capacitance of $C_{\rm drain}$ up to $V_{\rm out}$. As a result, the boost diode will turn OFF for a number of switching cycles and energy will be confined in the resonant circuit made up of L_b, $C_{\rm in}$, and $C_{\rm drain}$. The $C_{\rm in}$ capacitor will be discharged at a lower rate essentially determined by the losses of the switch and the resonant circuits.

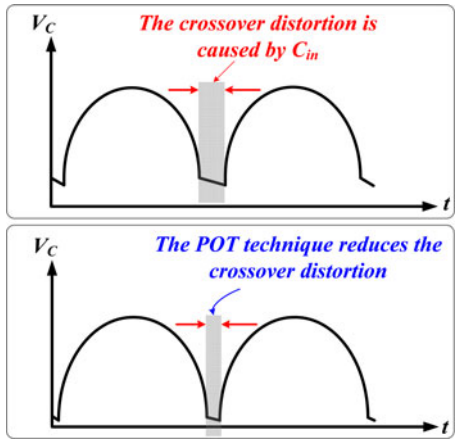

Fig. 5. Improved crossover distortion with the POT technique.

The energy transfer from input to output is lacking as long as the line phase angle is $\Phi_{C\,\rm drain}$ radians away from π fulfills the following inequality shown as follows:

$$\frac{1}{2}L_b\cdot\left(\frac{2}{\sqrt{2}}\cdot\frac{P_{\rm in}}{V_{\rm ac}}\cdot\sin\left(\pi-\Phi_{C\rm drain}\right)\right)^2 \le \frac{1}{2}\cdot C_{\rm drain}\cdot V_{\rm out}^2. \tag{6}$$

This means the input inductor current near the zero crossing voltage does not have enough power to charge the total capacitance. The input energy will be unable to transfer energy because the voltage across the input capacitor will be higher than the input voltage. According to this effect, the input power will stop to supply energy and the input resistance will increase suddenly. These will worsen $\Phi_{C\,\rm in}$ and the THD. Solving this inequality for $\Phi c_{\rm drain}$ yields (7). Fig. 4(b) shows the effect of $C_{\rm drain}$

$$\Phi_{C\rm drain} \approx \sin\Phi_{C\rm drain} \le \frac{V_{\rm out}V_{\rm ac}}{P_{\rm in}}\cdot\sqrt{\frac{C_{\rm drain}}{2L_b}}. \tag{7}$$

It is easy to show that the condition $\Delta\Phi \neq 0$ is true as long as $C_{\rm in}$ fulfills the following inequality:

$$C_{\rm in} \le \frac{V_{\rm out}}{4\pi f_L V_{\rm ac}}\cdot\sqrt{\frac{C_{\rm drain}}{2L_b}}. \tag{8}$$

This will prove that small input capacitor can decrease the zero crossing area and the input capacitor discharge time. The line phase angle is enlarged about $\Delta\Phi$ in Fig. 4(b) under the consideration of $C_{\rm drain}$. According to (8), the $C_{\rm in}$ value should be small enough to decrease the crossover distortion voltage. Thus, the contribution from $C_{\rm drain}$ can be neglected, that is, $\Delta\Phi$ is small enough to be ignored. To further improve the crossover distortion, the POT technique is utilized. The POT technique not only extends the on time automatically to discharge the charge on $C_{\rm in}$ near the zero crossings, but also senses the line voltage information, called the feedforward method, to improve the THD as shown in Fig. 5. Fig. 5 illustrates the decrease in the cross distortion with the POT technique. That is the POT technique can adjust the on-time value according to the variation of the line voltage.

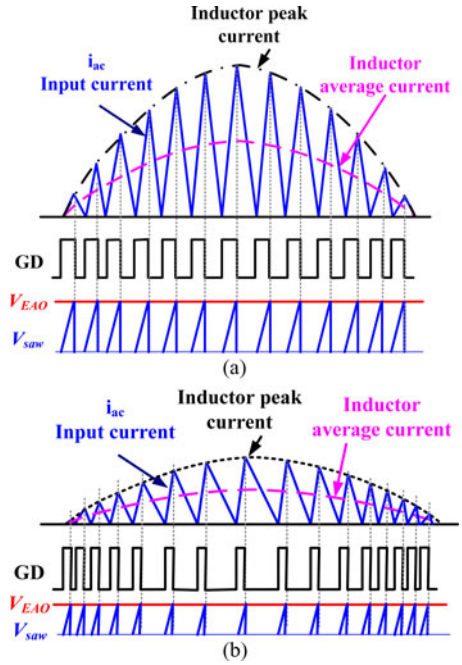

Fig. 6. Conventional PFC input ac current at (a) heavy loads and (b) light loads.

III. Proposed PFC Controller With the POT and the IT Techniques

A. POT Technique

The conventional BCM architecture is as shown in Fig. 1. The expressions of on time $t_{\rm on}$ and off time $t_{\rm off}$ are shown as follows:

$$t_{\rm on} = \frac{V_{\rm EAO}}{V_{\rm saw}} \cdot T_S \text{ and } t_{\rm off} = \frac{V_c}{V_{\rm out} - V_c} \cdot t_{\rm on} \tag{9}$$

where

$$T_S = t_{\rm on} + t_{\rm off}. \tag{10}$$

As shown in Fig. 6(a), the well-regulated dc output voltage ensures the value on time is nearly constant to derive the input resistance seen at the ac source nearly constant for high PF. As mentioned earlier, the THD will deteriorate the PF [11]–[13]. In (11), THD is also commonly defined as the ratio of the sum of the powers of all harmonic components to the power of the fundamental frequency, where I_1 is the fundamental signal of $i_{\rm ac}$ and I_2–I_n indicate the harmonic signals of $i_{\rm ac}$

$$\text{THD} = \frac{\sqrt{I_2^2 + I_3^2 + I_4^2 + I_5^2 + \ldots\ldots + I_n^2}}{I_1}. \tag{11}$$

The THD gradually increases when the output loading decreases as depicted in Fig. 6(b) because the fundamental energy is decreased. Thus, the PF is seriously affected.

Ideally, the PF is equal to the following expression

$$PF = \frac{P_{\rm in}}{P_{\rm line}} = \frac{(1/2\pi) \cdot \int_0^{2\pi} i_{\rm ac}(\theta) \cdot v_{\rm ac}(\theta) \cdot d\theta}{I_{\rm rms} \cdot V_{\rm rms}}. \tag{12}$$

$P_{\rm in}$ is the input power and $P_{\rm line}$ is the line power. $I_{\rm rms}$ and $V_{\rm rms}$ are the rms value of the line current and voltage, respectively.

If the crossover distortion caused by the voltage drop of the diodes and the resonant effect in the bridge is considered, the THD is further deteriorated. The main crossover distortion angle Φ caused by the THD will be proved as follows. That is, the line current can be expressed as (13) if Φ is taken into consideration, where I_m is the peak value of the line current

$$i_{\rm ac}(\theta) = \frac{I_m}{1 - \sin\Phi} \cdot (\sin\theta - \sin\Phi) \text{ and } v_{\rm ac}(\theta) = V_m \sin\theta. \tag{13}$$

As a result, $P_{\rm in}(\theta)$ with the consideration of the THD effect can be derived as (14) after substituting (13) into (12)

$$P_{\rm in}(\theta) = \frac{V_m \cdot I_m}{\pi \cdot (1 - \sin\Phi)} \cdot \left[\frac{\pi}{2} - \Phi - \frac{1}{2}\sin 2\Phi\right]. \tag{14}$$

When the crossover distortion angle is smaller than Φ, the input line current is zero. Hence, the distortion angle is only proved from Φ to $\pi - \Phi$ with $P_{\rm in}$ given by (14). Here, $I_{\rm rms}$ can be derived as follows:

$$I_{\rm rms} = \sqrt{\frac{1}{2\pi} \cdot \int_0^{2\pi} i_{\rm ac}^2(\theta) \cdot d\theta}$$

$$= \sqrt{\frac{I_m^2}{\pi \cdot (1 - \sin\Phi)^2} \cdot \left[\frac{\pi}{2} - \Phi - \frac{3}{2}\sin 2\Phi + (\pi - 2\Phi)\sin^2\Phi\right]}. \tag{15}$$

Therefore, the PF and the THD can be obtained as follows:

$$\text{PF}(\Phi) = \frac{P_i}{V_{\rm rms} \cdot I_{\rm rms}} = \frac{\pi - 2\Phi - \sin 2\Phi}{\sqrt{\pi \cdot [(\pi - 2\Phi)(2 - 2\cos 2\Phi) - (3\sin 2\Phi)]}} \tag{16}$$

$$\text{THD}(\Phi)\% = 100 \cdot \sqrt{\frac{\pi \cdot [(\pi - 2\Phi)(2 - 2\cos 2\Phi) - (3\sin 2\Phi)]}{(\pi - 2\Phi - \sin 2\Phi)^2} - 1}. \tag{17}$$

The THD is seriously affected by the distortion angle Φ. By reducing the value of Φ, the THD can be decreased and thus the PF can be effectively improved. If the value of Φ can be greatly decreased, (16) and (17) can be simplified as follows:

$$\text{PF}(\Phi) = \frac{\pi - 2\Phi}{\sqrt{\pi \cdot (\pi - 2\Phi)}} \tag{18}$$

$$\text{THD}(\Phi)\% = 100 \cdot \sqrt{\frac{\pi}{(\pi - 2\Phi)} - 1}. \tag{19}$$

Fig. 7 illustrates the variations of PF and THD versus the variations of crossover distortion angle effect. The smaller the value of Φ, the better it will correspond to the values of PF and THD. Therefore, if the THD needs to be smaller than 5%, the value of Φ should be smaller than 0.08 rd/s. As a result, it will have a high PF value of 0.999.

Fig. 8 shows the proposed PFC architecture with POT and IT controls for reduced THD and high PF at the same time. The POT technique modifies the conventional fix on-time mechanism through the addition of input current information to

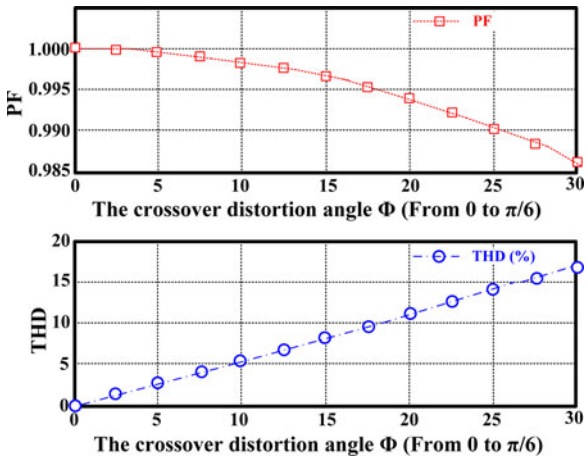

Fig. 7. Relationship of PF and THD versus distortion angle.

modulate on-time behavior according to different load conditions. In other words, the POT technique shapes the on time by the input current and the output voltage loop, rather than simply by the output voltage loop [14]–[17].

Fig. 9 illustrates the functionality of the proposed POT technique to verify the distortion angle Φ is effectively decreased. Input current information through the current sensing signal $V_{\rm CS}$ is injected into the control loop. $V_{\rm CS}$ can also compare with the predefined value $V_{\rm limit}$ to decide whether the overcurrent (OC) situation happens or not. On-time value is drastically increased in case of low input line current to reduce the distortion angle by further discharging $C_{\rm in}$. Simultaneously, efficiency can be raised due to the decreasing switching frequency because switching loss on the charging/discharging of the gate capacitance is greatly reduced. Therefore, the perturbation of on-time value is based on the input ac voltage, which can decrease THD and thus increase PF.

B. IT Control

To further increase the efficiency and reduce the EMI problem, the proposed IT control can set up the minimum off-time value as shown in Fig. 10. The converter contains at least one minimum off time to deliver the energy to the output. Before exceeding the minimum off time, the converter will not trigger the next switching again. In other words, the switching frequency will not be increased infinitely to cause a serious EMI problem. At low input line voltage, the minimum off time is extended. As a result, the resultant reduction in switching frequency can enhance the efficiency [18], [19].

C. System Stability

The stability is simply ensured in the PFC with the BCM control owing to the insertion of the low-frequency dominant pole in the system. For better noise rejection, the bandwidth of the system is designed to filter out the 120-Hz noise caused by the bridge rectifier from $V_{\rm ac}$. Generally, the dominate pole is designed smaller than 20 Hz and expressed as follows:

$$P_1 = \frac{g_{m\_\rm EA}}{2 \cdot \pi \cdot C_C} \tag{20}$$

g_{m_EA} is the transconductance of the EA and C_C is the compensation capacitor at the output of the EA.

IV. Circuit Implementation

A. POT Technique Circuit

As shown in Fig. 11(a), the POT technique circuit contains three blocks, namely, the adjustable saw-tooth generator, the THD improvement, and the max-on-time limiter. Accuracy of the adjustable saw-tooth generator can be improved by the timing adjustment circuit to ensure adequate power delivery. The timing adjustment circuit can adjust the minimum operation frequency higher than 35 kHz. The max-on-time limiter is also used to limit the maximum on-time value for avoiding overloading through the comparison of a higher voltage level $V_{\rm ref2}$ (3 V in this paper), as shown in the timing diagram of POT in Fig. 11(b). The waveform of $V_{\rm saw}$ ramps up from 0.45 V with the addition of the signal $V_{\rm CS}$ to form the signal $V_{\rm add}$. On-time value can be determined by the comparison of $V_{\rm EAO}$ and $V_{\rm add}$.

The adjustment of on-time value can optimize the crossover distortion angle Φ. According to (6) and the POT technique, the derived (21) can demonstrate the improvement contributed by the POT technique, that is, the decrease in Φ can be expressed as $\Phi_{\rm POT}$, which is effectively controlled by the POT technique. Here, $\Phi_{\rm POT}$ is modulated by $t_{\rm on\_POT}$ to perturb $t_{\rm on}$

$$\frac{1}{2}L_b \cdot \left(\frac{V_m}{L_b} \cdot \sin\left(\pi - \Phi_{\rm POT}\right)\right)^2 \cdot \left(t_{\rm on} + t_{\rm on\_POT}\right)^2 \le \frac{1}{2} \cdot C_{\rm drain} \cdot V_{\rm out}^2. \tag{21}$$

Solving this inequality for $\Phi_{\rm POT}$ can be derived as follows:

$$\Phi_{\rm POT} \approx \sin \Phi_{\rm POT} \le \sqrt{L_b \cdot C_{\rm drain}} \cdot \frac{V_{\rm out}}{V_m} \cdot \frac{1}{\left(t_{\rm on} + t_{\rm on\_POT}\right).} \tag{22}$$

The on-time value can be decided by the slope of the input current and the k factor shown as follows:

$$\left(t_{\rm on} + t_{\rm on\_POT}\right) = \frac{V_{\rm EAO}}{S_{\rm saw} + S_{cs}} = \frac{V_{\rm EAO}}{S_{\rm saw} + \left(V_C/L_b\right) \cdot R_{\rm CS}} = \frac{V_{\rm EAO}}{S_{\rm saw} + k \cdot \left(V_C/L_b\right)} \tag{23}$$

where $k = R_{\rm CS}$ and $S_{cs} = k \cdot \frac{V_C}{L_b}$

$S_{\rm saw}$ is proportional to $V_{\rm ref}$ in Fig. 11(a) and indicates the slope of the output voltage from the saw-tooth generator. The on time is determined by the comparison between $V_{\rm EAO}$ and the summation of $S_{\rm saw}$ and $S_{\rm cs}$. The conventional design only uses $S_{\rm saw}$ to decide$t_{\rm on}$ while the insertion of $S_{\rm cs}$ can get the information of the ac line voltage. That is, the THD can be reduced due to $S_{\rm cs}$.

Therefore, adjustment of the k factor can effectively improve THD according to V_C. A too large value of k may affect the

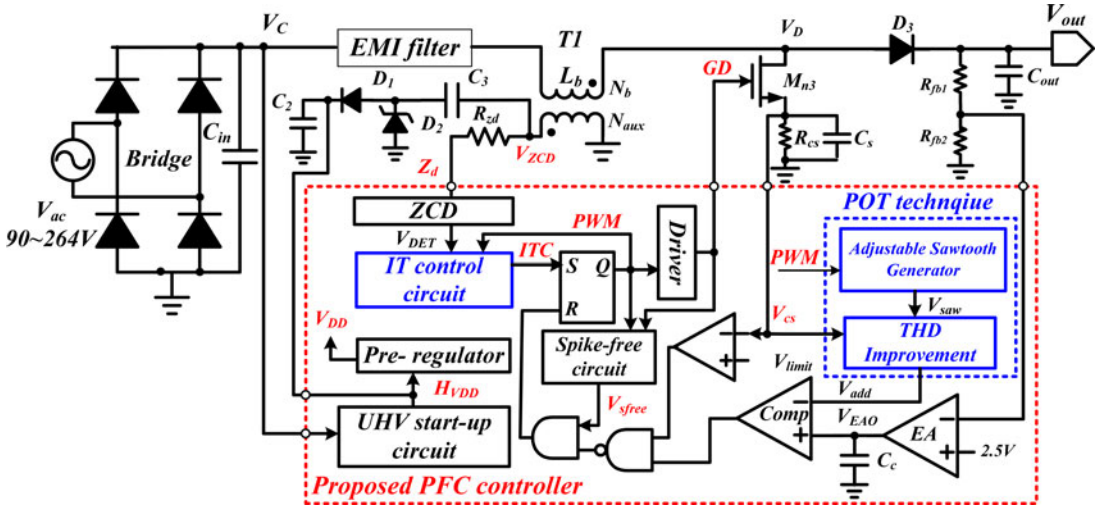

Fig. 8. Proposed PFC architecture with POT and IT controls, NNV-ZCD circuit, and UHV startup mechanism.

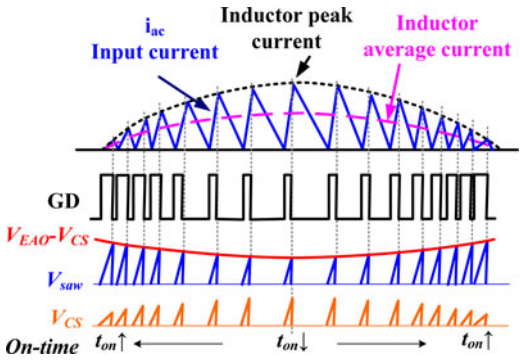

Fig. 9. Control mechanism of the POT technique.

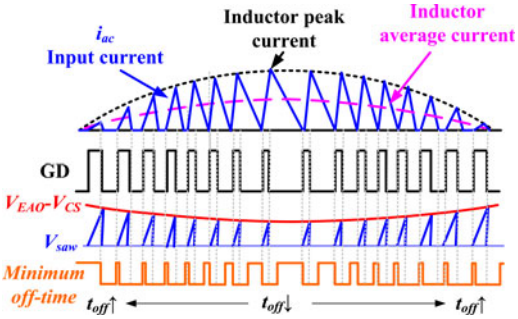

Fig. 10. Control timing diagram of the IT control.

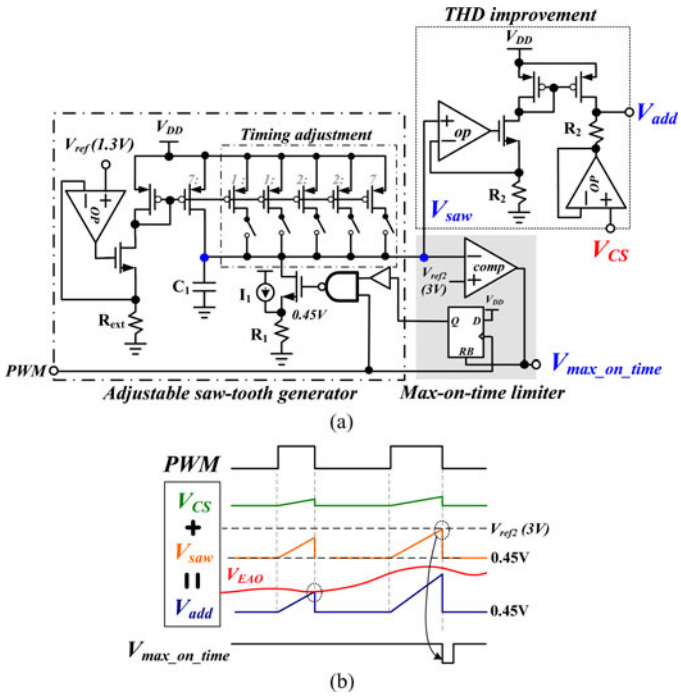

Fig. 11. (a) Schematic of the POT circuit. (b) Timing diagram of the POT technique.

regulated output voltage because the current limiting circuit may be triggered. In this study, $V_{\rm CS}$ is the current sensing signal and is inversely proportional to the value ac input voltage. It results in the increase in on-time value at low ac input voltage but the decrease in on-time value at high ac input voltage. In other words, the inductor current will be charged longer than that of the conventional design at low ac input voltage to reduce the crossover distortion angle Φ. The simulation results will prove the V_C difference with and without the POT technique as shown in Fig. 12. The PF can be increased owing to the reduction in the THD.

B. IT Control Circuit

The IT control circuit in Fig. 13(a) can improve the EMI performance by reducing high switching loss at light loads and around low voltage level of the input line voltage. The IT control circuit adjusts the minimum off-time value according the loading indication signal $V_{\rm EAO}$, which is generated by the EA in Fig. 8. In Fig. 13(a), the voltage across the resistor R_1 defines the current flowing through the transistor M_4. Specifically, lowering the value of $V_{\rm EAO}$ leads to a higher value of the current flowing through the M_4. Consequently, the charging current as expressed in (24) for the capacitor C_1 is drastically decreased

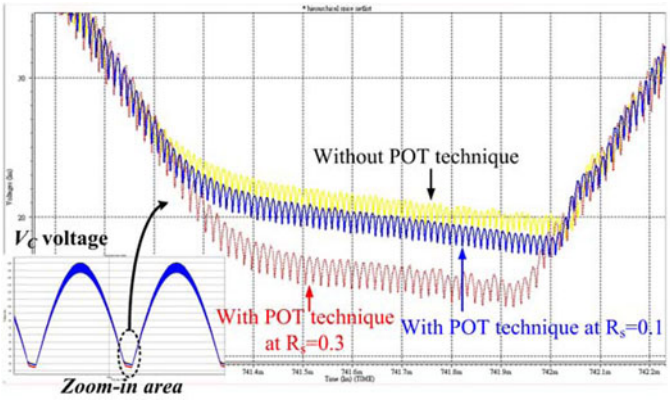

Fig. 12. Waveform of V_C with and without the POT technique.

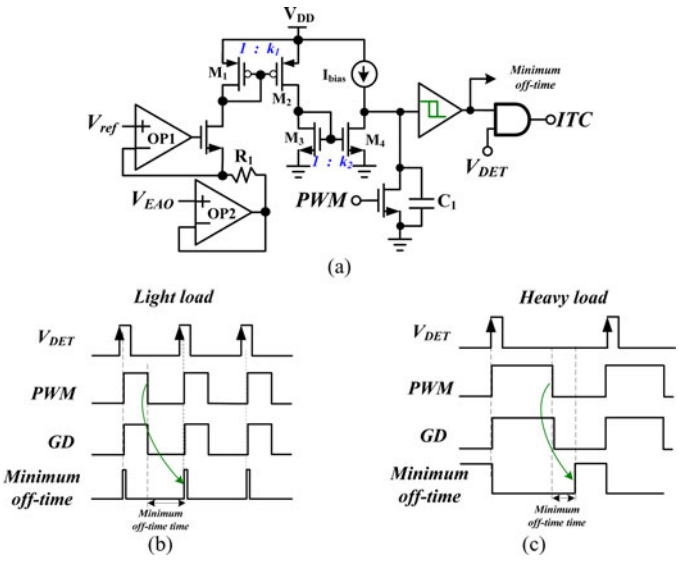

Fig. 13. (a) Schematic of the IT control circuit. The timing diagram of the IT control circuit at (b) light loads and (c) heavy loads.

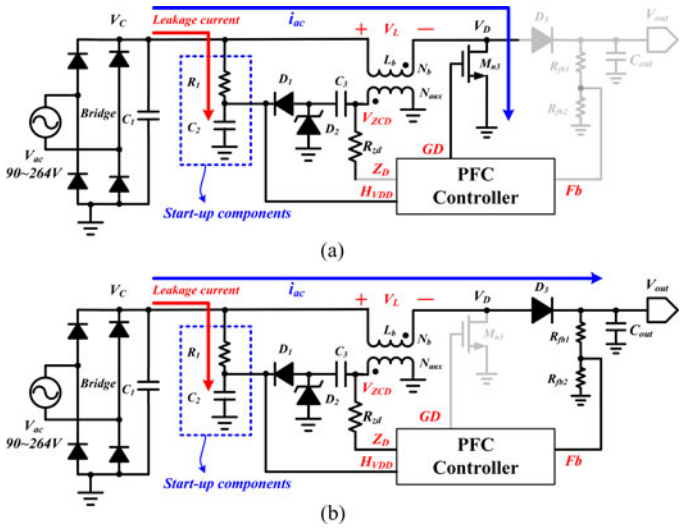

Fig. 14. Operation of the conventional PFC with the BCM control. (a) On-time is determined by the peak current control. (b) Off-time is determined by the ZCD.

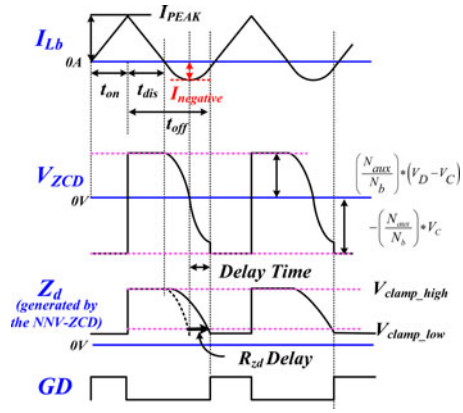

Fig. 15. ZCD waveforms with the proposed nonnegative signal Z_d.

to generate a longer minimum off time

$$I_{C1} = I_{\text{bias}} - k_1 \cdot k_2 \cdot \frac{V_{\text{ref}} - V_{\text{EAO}}}{R_1} \tag{24}$$

where k_1 and k_2 are current mirror ratios.

The timing diagram of the IT control circuit is shown in Fig. 13(b) and (c) at light loads and heavy loads, respectively.

C. Nonnegative-Voltage Zero Current Detector Circuit

The BCM operation is depicted in Fig. 14(a) and (b) to show the inductor charge and discharge path, respectively, for revealing V_{ZCD} potential. The timing diagram of the ZCD operation in BCM control is shown in Fig. 15. The BCM is used in the ZCS technique. As the inductor energy releases to the output, the switch-on point is selected at the next zero-crossing point after t_{dis} because the inductor current is close to zero in the BCM operation. If the inductor current reaches zero, the next switching cycle will be triggered to effectively deliver energy to the output. In the meanwhile, V_{ZCD} decreases toward a negative value equal to $-(N_{\text{aux}}/N_b) \cdot V_C$, that is, the ratio of auxiliary winding to the primary winding determines how negative the value of V_{ZCD} is. However, if the signal of V_{ZCD} as expressed in (25) is injected to the controller chip, it will result in the failure of the chip owing to the latch-up problem, which causes permanent damage

$$-\left(\frac{N_{\text{aux}}}{N_b}\right) \cdot V_C \le V_{\text{ZCD}} \le \left(\frac{N_{\text{aux}}}{N_b}\right) \cdot (V_D - V_C). \tag{25}$$

Therefore, instead of V_{ZCD}, the filtered signal Z_d generated by the proposed nonnegative-voltage zero current detector (NNV-ZCD) circuit in Fig. 16 is clamped between $V_{\text{clamp\_low}}$ and $V_{\text{clamp\_high}}$ to avoid negative voltage and overvoltage, respectively. When the PWM signal switches from high to low, the stored energy of the inductor starts to release to the output. V_{ZCD} will start to decrease because the energy in the inductor dries out. Once the signal Z_d voltage is lower than the threshold voltage V_H, the PWM signal will be set high by the positive triggering signal V_{DET} to start the next switching cycle. The signal V_{DET} will be reset as the Z_d signal is lower than V_L. When Z_d gradually decreases smaller than zero, the transistor M_2 will

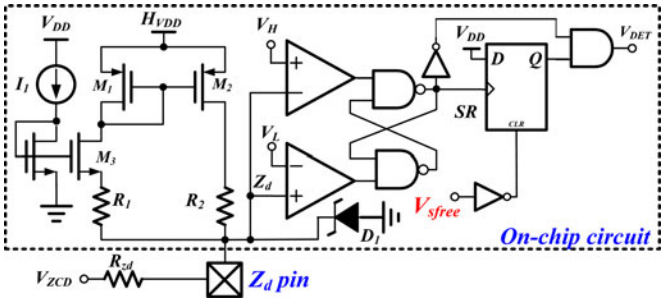

Fig. 16. Schematic of the proposed NNV-ZCD circuit.

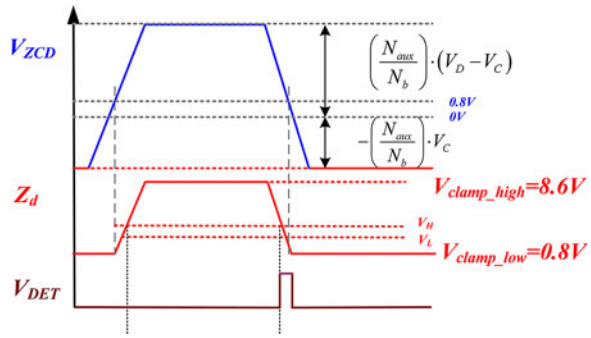

Fig. 17. Timing diagram of the proposed NNV-ZCD circuit.

form a negative feedback to clamp the voltage still higher than 0.8 V. The low clamping voltage $V_{\mathrm{clamp\_low}}$, 0.8 V, is used to detect the high-to-low transition of V_{ZCD} to prevent the chip from seeing the negative voltage. Ideally, the value should be 0 V. However, considering the PVT variations, the value is raised to 0.8 V to have a tolerance margin due to the response time of the sensing circuit. The timing diagram is shown in Fig. 17.

The next switching cycle will start the peak current control after setting the signal gate driver (GD) to high by the PWM signal. Here, to improve the switching noise immunity, the current sensing signal is blocked until the signal V_{sfree} from the spike-free circuit is set to high.

D. UHV Startup Circuit

Before the first stable switching, no power can be delivered to auxiliary winding. Therefore, the PFC control circuit needs the startup circuit to guarantee the initial of the preregulator. After the preregulator obtained the ability to supply the PFC controller to start the BCM operation, the startup circuit will be shut down to save much power loss. In Fig. 1, the conventional startup mechanism contains the external startup resistor and the hold-up capacitor, R_1 and C_2, respectively. R_1 is 470 k and consumes 0.18 W at 220 V_{ac}. The charge pump circuit, composed with D_1, D_2, and C_3, can supply the hold-up voltage for the internal preregulator once the BCM operation starts to work. However, the external startup resistor and capacitor (R_1 and C_2, respectively) will induce a large leakage current even after the startup period because the passive components cannot be shut down. Efficiency is greatly deteriorated by such a simple startup mechanism.

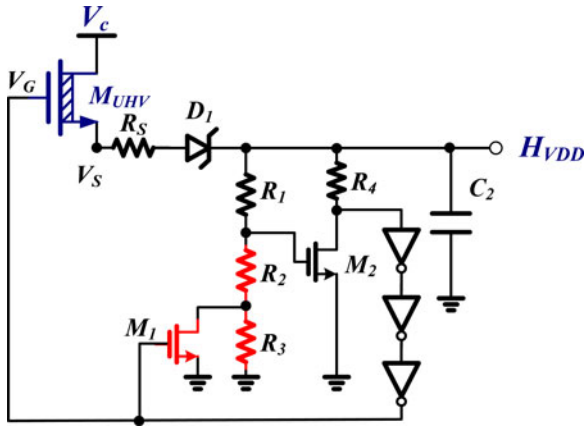

Fig. 18. Schematic of the 800 V UHV startup circuit.

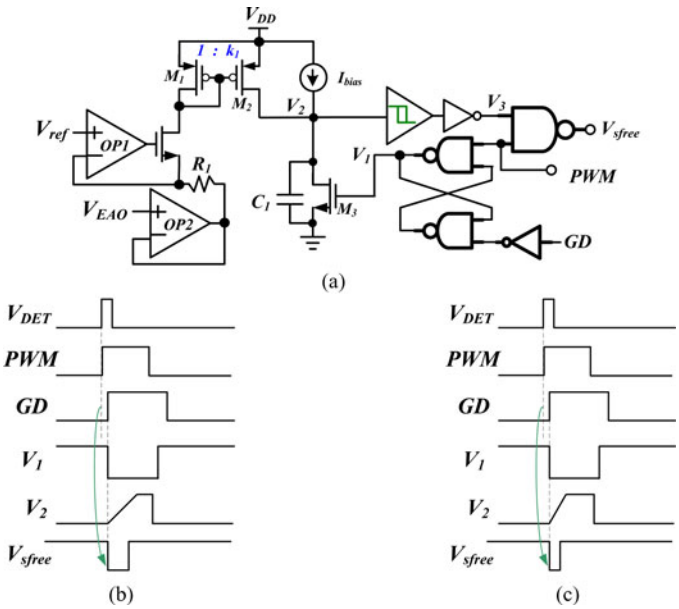

Fig. 19. Schematic of the spike-free circuit at (a) timing diagram at (b) heavy loads and (c) light loads.

In contrast, the proposed UHV startup technique in Fig. 8 can ensure the initial of the preregulator during the power-on period [20], which can be fully shut down for power saving once the auxiliary winding of the transformer can provide enough energy to the hold-up capacitor C_2 to have a regulated H_{VDD}. Moreover, the number of external passive components can be reduced for low cost and compact size.

The 800-V UHV startup circuit is depicted in Fig. 18. The UHV startup function can be implemented using one UHV depletion N-type MOSFET M_{UHV}. The UHV startup circuit has a hysteric window that will be generated by M_1 to reject power noise. The upper bound and lower bound voltages are shown as follows:

$$H_{\mathrm{VDD(upper\_bound)}} = \frac{R_1 + R_2}{R_2} \cdot V_{\mathrm{TH2}} \text{ and } H_{\mathrm{VDD(lower\_bound)}} = \frac{R_1 + R_2 + R_3}{R_2 + R_3} \cdot V_{\mathrm{TH2}}. \quad (26)$$

TABLE I
DESIGN SPECIFICATIONS

Technology	TSMC 0.5 μm UHV LDMOS
PFC die area (with test pads)	1200 μm × 800 μm
UHV start-up area	650 μm × 500 μm
Ac input voltage range V_{rms}	90–264V_{ac}
Output voltage (V_{out})	400V
Minimum Switching frequency (f_{SW})	>35 KHz
Output power	90 W
L_b	400μH
N_b	60T
N_{aux}	8T
Output capacitor (C_{out})	68μF/450V
C_C	1μF
ΔV_{out}	9.6V
Power consumption	88 mW

TABLE II
COMPARISONS ARE BETWEEN THE PROPOSED METHOD AND THE PRIOR ARTS

	This work	[2]	[3]	[7]	[21]	[22]
Input inductor (μH)	400	600	N/A	80/180	1240	70
Output Capacitor	68 μF	100 μF	N/A	220 μF	220 μF	220 μF
Input line voltage	90-264 V_{ac}	265 V_{ac}	85-267 V_{ac}	90-264 V_{ac}	85-265 V_{ac}	230 V_{ac}
Output voltage	400 V	400 V	390 V	400 V	392.5 V	400 V
Switching frequency	> 35 kHz	N/A	60 kHz	100 kHz	50 kHz	65 kHz
Circuit Integrated	Fully integrated	System level	Fully integrated	System level	System level	System level
Control mechanism	POT technique	Variable on-time	DCM/BCM	Proposed variable-duty-cycle control	CCM-DCM control	Digital controller
THD (minimum) (%)	6	6.1	N/A	N/A	3.59	14.6
Power factor	0.998	N/A	~0.98	~0.999	0.985	0.964
Efficiency	95.4%	N/A	N/A	N/A	99.17%	N/A
FOM	0.164	N/A	N/A	N/A	0.994	0.233

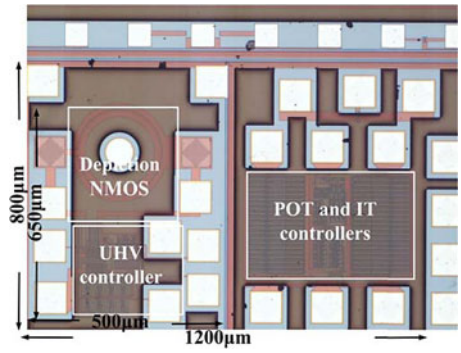

Fig. 20. Micrograph of the PFC circuit with the POT technique, the IT control circuit, and the UHV startup mechanism.

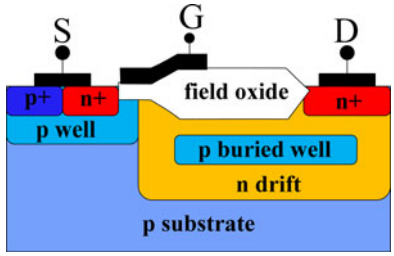

Fig. 21. Cross sections in UHV lateral power LDMOS with triple RESURF structure.

During the power-on sequence, the UHV transistor will be turned OFF by M_2 when $H_{\rm VDD}$ is higher than the upper bound voltage. Due to the shutdown of the UHV transistor, the leakage current can be minimized. If the voltage at the output capacitor C_2 is lower than the lower bound voltage, the UHV startup circuit is triggered again.

E. Spike-Free Circuit

Owing to high current flowing through the power MOSFET M_{n3} in Fig. 8, the spike-free circuit is used to evade the spike noise and avoid an abnormal decision of the duty cycle. The spike-free circuit is shown in Fig. 19(a) can avoid the high switching noise issue when the power MOSFET is turned ON. Simultaneously, the current limiting mechanism will be disabled during the spike-free operation in order not to shut down the overall operation. The spike-free circuit eliminates the switching noise issue spike without needing an external low pass filter.

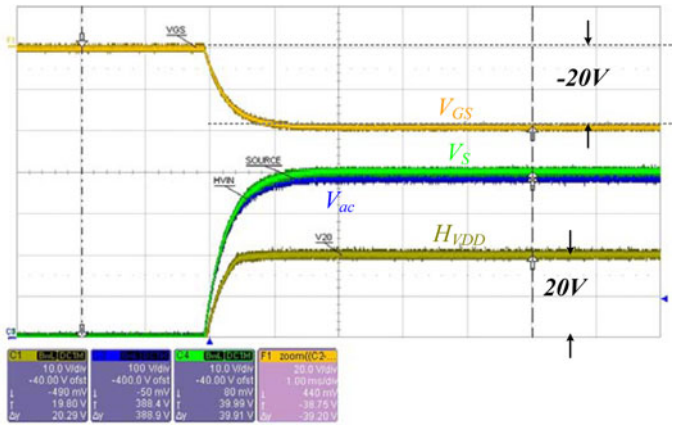

Fig. 22. Power-on waveforms of the UHV startup mechanism.

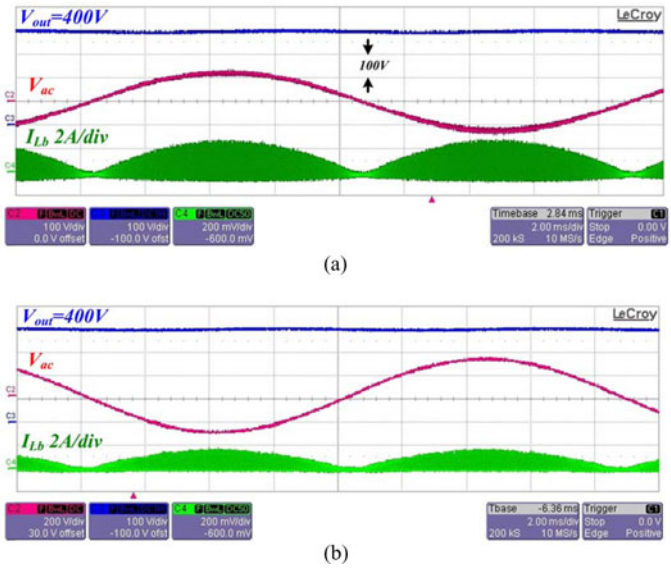

Fig. 23. Measured input and output voltages and output current with the load of 90 W at (a) $V_{\rm in} = 90\ V_{\rm ac}$ and (b) $V_{\rm in} = 220\ V_{\rm ac}$.

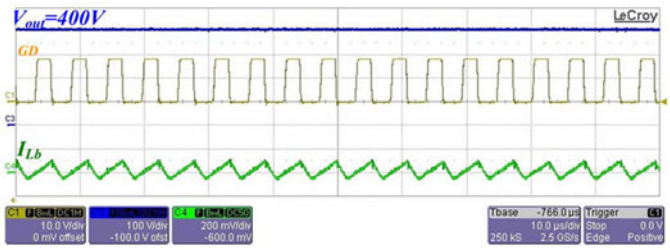

Fig. 24. Measured inductor current waveform under the POT technique and the IT control.

The spike-free circuit adjusts the spike-free time according to the loading condition, as indicated by the signal $V_{\rm EAO}$ in Fig. 8.

In Fig. 19(a), the voltage across the resistor R_1 defines the current flowing through the transistor M_3. Lowering the value of $V_{\rm EAO}$ leads to a higher value of the current flowing through M_3. As a result, the charging current is expressed as follows:

$$I_{C1} = I_{\rm bias} + k_1 \cdot \frac{V_{\rm ref} - V_{\rm EAO}}{R_1}. \qquad (27)$$

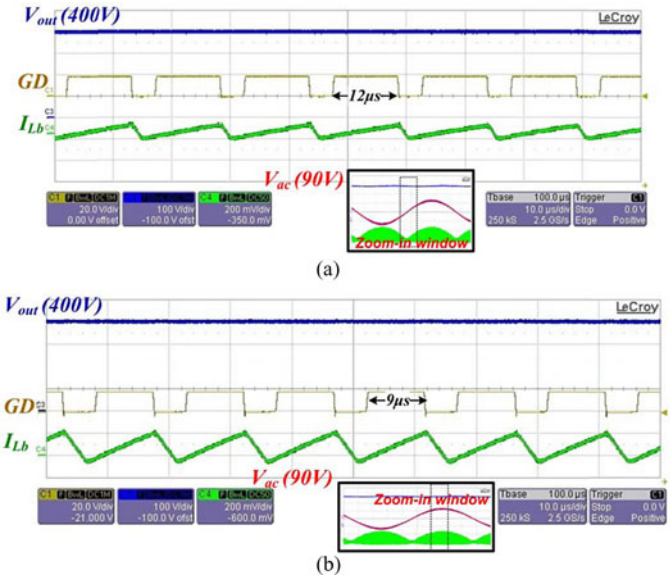

Fig. 25. POT function can extend the on time value according to the load current at $V_{\rm in} = 90\ V_{\rm ac}$. (a) Zoom-in waveforms at low ac input voltage. (b) Zoom-in waveforms at high ac input voltage.

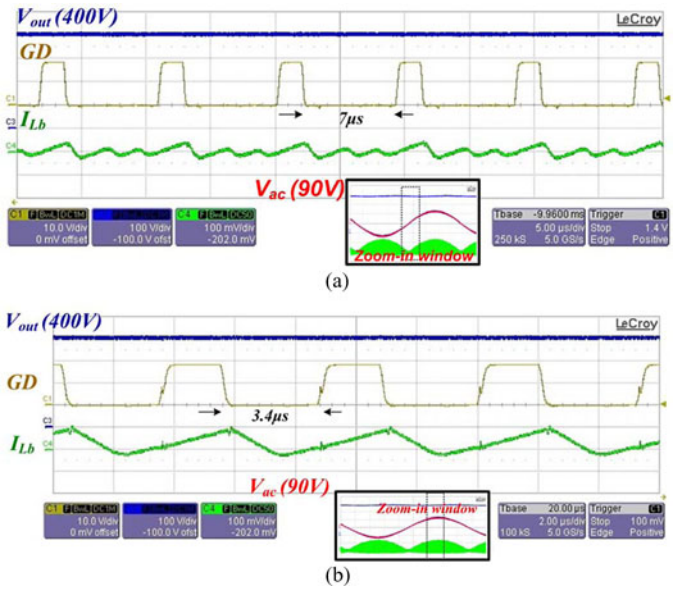

Fig. 26. Under ac input voltage = 90 $V_{\rm ac}$ and output power is 15.5 W. (a) Off-time is extended at low AC input voltage. (b) Off-time is slightly extended at high AC input voltage.

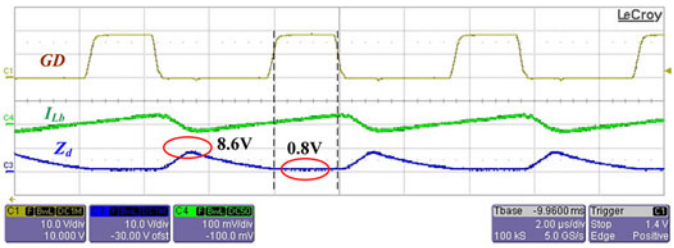

Fig. 27. Measured waveforms of the NNV–ZCD circuit.

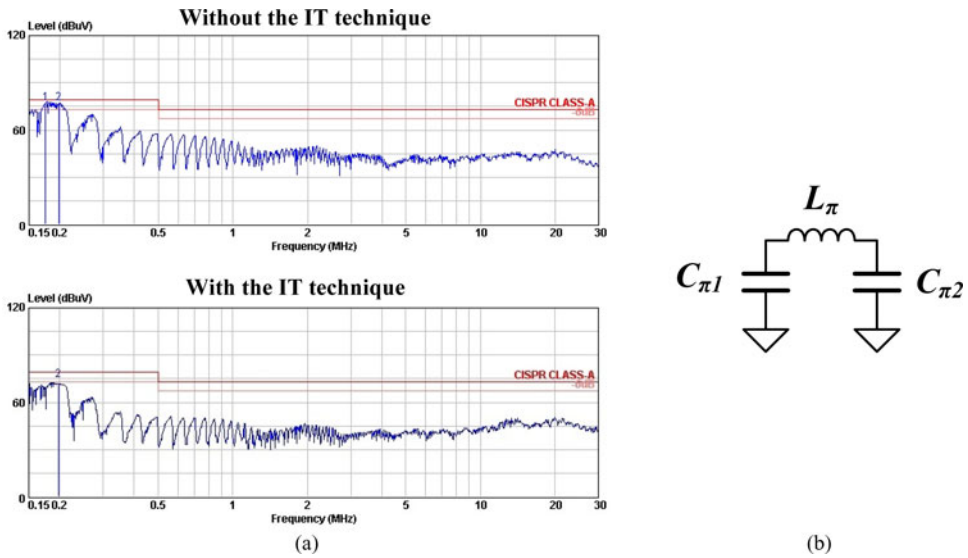

Fig. 28. (a) Measured EMI results of the PFC controller without the IT technique and with the IT technique under the same EMI filter. (b) EMI filter used in this paper.

The timing diagram of the spike-free circuit is shown in Fig. 19(b) and (c) at heavy and light loads, respectively. The value of the spike-free period is extended at heavy loads due to the large switching noise caused by a large inductor current.

V. Experiment Results

The PFC controller with the POT technique and the IT control circuit, the NNV-ZCD circuit, and the UHV startup mechanism was fabricated in the TSMC 0.5 μm 800-V UHV LDMOS process. The specifications of the PFC controller are listed in Table I and the comparison with the prior arts is also shown in Table II. The figure of merit (FOM) shown in (28) can compare the performance among different implementations

$$\mathrm{FOM} = \frac{L_b \cdot C_{\mathrm{out}} \cdot \mathrm{THD}}{\mathrm{PF}}. \tag{28}$$

The proposed technique can have the minimum FOM compared to the others. That is, the system can have a small volume and improved performance compared to the others.

The external devices of the primary-side inductor and the output capacitor are 400 and 68 μF, respectively. Considering the preregulator as the internal power supply, the upper-bound startup voltage is 16 V. Output voltage of the PFC controller is 400 V for the next-stage PWM converter.

The chip micrograph is shown in Fig. 20 with an active area of 1200 μm $\times$ 800 μm. A conventional cross section of the UHV triple reduce surface field (RESURF) lateral MOSFET (LDMOS) is shown in Fig. 21. The contact of n-drift and p-well can resist high voltage. Furthermore, the structure with floating p buried well inserted into n drift region to provide dual conduction paths that can provide a significant reduction in on-state resistance [23]. The power-on sequence of the UHV startup mechanism is shown in Fig. 22. The output voltage H_{VDD} is 20 V and the final V_{GS} of the UHV device is -20 V. That is, the depletion NMOSFET is completely turned OFF for low leakage current.

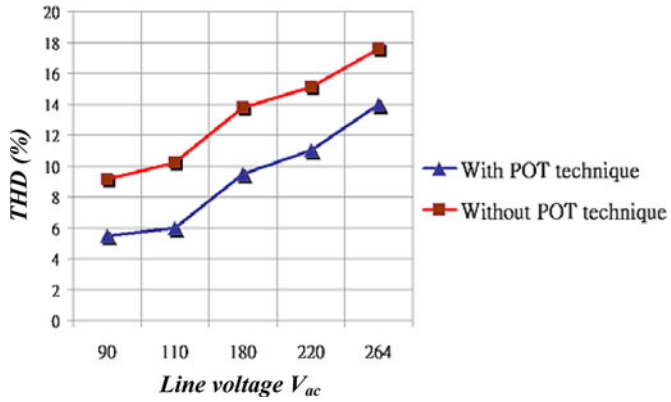

Fig. 29. Measured THD performance with and without the POT technique at full load condition.

Fig. 23 shows the measured waveforms at full load at 90 V_{ac} and 220 V_{ac} input voltages, respectively. V_{out} is regulated at 400 V with the load of 90 W. The PF is 0.998 and 0.985, respectively. The measured inductor current shows the POT and IT operations in Fig. 24. Fig. 25(a) shows the function of the POT circuit to extend the on-time value at low ac input voltage. The on-time value will be extended at zero current condition to improve THD value automatically. Fig. 25(b) shows the POT on time at high ac input voltage. Thus, the PF is 0.998 contributed by the POT technique. Fig. 26(a) shows the function of the IT controller to reduce switching loss at the low ac input voltage. The zero current is detected, but the next PWM signal is triggered when the inhibit off time is over. Fig. 26(b) shows the IT is smaller than the off-time value. Thus, the zero current determines the beginning of the next PWM signal. The estimated efficiency is 95% due to the POT and IT controls.

Fig. 27 shows the measured waveforms of the NNV-ZCD circuit. When the power N-type MOSFET is turned ON, the maximum input signal Z_d is clamped to 8.6 V, not the calculated

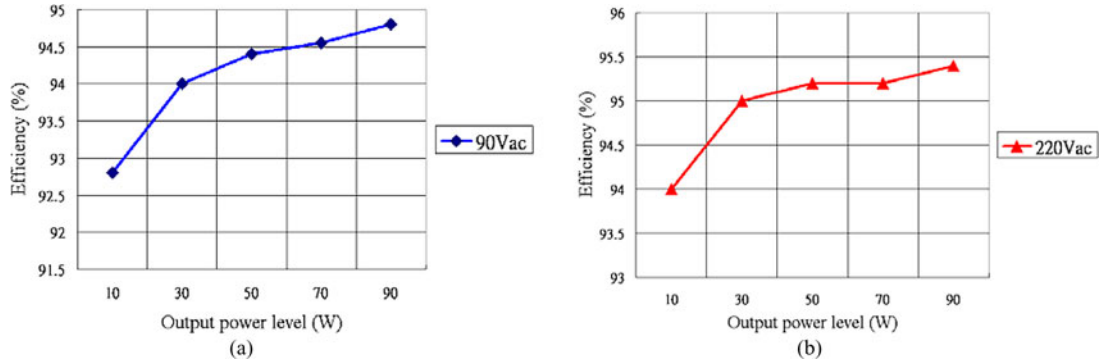

Fig. 30. Measured efficiency results of the PFC controller. (a) 90 V_{ac}. (b) 220 V_{ac}.

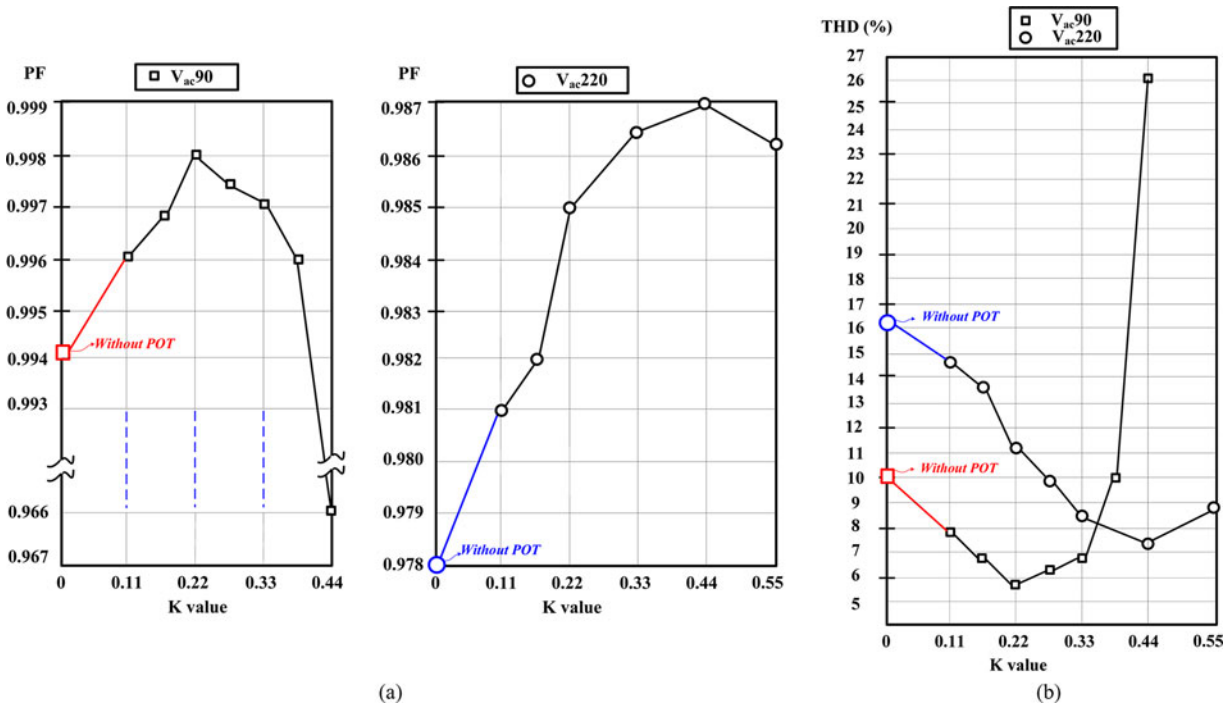

Fig. 31. Measured results improved by the POT technique. (a) PF value. (b) THD value.

value of 53.3 V. On the other hand, the minimum input signal Z_d is clamped to 0.8 V, not the calculated value of −49.77 V. $V_{\text{clamp\_high}}$ was locked by the zener diode and $V_{\text{clamp\_low}}$ was reached almost 0.8 V by negative feedback technique in the NNV circuit. The nonnegative Z_d can prevent the integrated chip from being damaged by the large negative voltage. Fig. 28(a) shows the experimental EMI in the two cases: with and without IT enabled. The EMI can be effectively improved by the proposed technique with the same EMI filter in Fig. 28(b). Besides, under the requirement of EN61000−3−2, the proposed method can reduce the EMI filter ($C_{\pi 1}$, L_{π}, and $C_{\pi 2}$) from the conventional design (0.47, 350, and 0.47 μF) to the new value (0.33, 280, and 0.33 μF).

Fig. 29 shows the measured THD performance comparison between the conventional fix-on time and the proposed POT technique. The proposed technique has improved the THD 4% toward fulfilling the requirement of high PF value. Fig. 30 shows the measured efficiency of the PFC controller.

Fig. 31 shows the measured PF and THD, which include the bridge diode forward-voltage and parasitic capacitors. After the POT technique implementation, the distortion angle can be alleviated. The improved PF and THD can approach the ideal values compared to the calculated PF and THD under different selections of k factor. Once the value of k is larger than 0.22, the current limiting circuit will be triggered to cause the decrease in the PF and the increase in the THD as the ac line voltage is 90 V_{ac}. On the other hand, if the ac line voltage is 220 V_{ac}, the increasing value in the k factor will continuously improve the PF and the THD until k is large than 0.44.

VI. Conclusion

A high efficiency of 95% can be ensured at the output power of 90 W through the proposed POT and IT controls. The PFC controller can have low THD of 6% and high PF of 0.998 at 90 $V_{ac,}$ and high PF of 0.985 at 220 V_{ac} because the on-time

value is perturbed by the input voltage information for reducing the distortion angle. The adaptive minimum off-time adjustment by the IT controller can also reduce the switching power loss to guarantee high efficiency. In addition, due to the UHV device, the startup mechanism can minimize the current leakage at the ac input and remove the need of external startup components. Thus, the performance can be further enhanced under the improved noise immunity by the spike-free circuit. The test circuit fabricated in the TSMC 800-V UHV process can show high performance and a highly integrated PFC controller.

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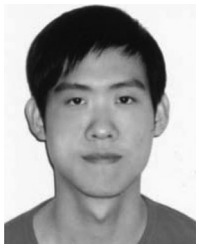

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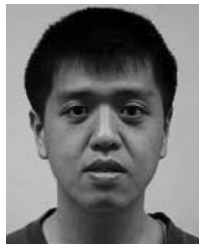

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