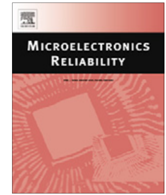
Microelectronics Reliability 53 (2013) 2–6

Contents lists available at SciVerse ScienceDirect

Microelectronics Reliability

journal homepage: www.elsevier.com/locate/microrel



Transition from flip chip solder joint to 3D IC microbump: Its effect on microstructure anisotropy

K.N. Tu [a,*], Hsiang-Yao Hsiao [b], Chih Chen [b]

[a] Department of Materials Science and Engineering, University of California at Los Angeles, Los Angeles, CA 90095-1595, USA
[b] Department of Materials Science and Engineering, National Chiao Tung University, Hsinchu, Taiwan, ROC

ARTICLE INFO

Article history:
Received 23 April 2012
Received in revised form 23 July 2012
Accepted 24 July 2012
Available online 1 September 2012

ABSTRACT

As microelectronic industry develops 3D IC on the basis of through-Si-vias (TSV) technology, the processing and reliability of microbumps, which are used to interconnect the stacking chips, is being actively investigated. Due to the reduction in size of microbumps, the diameter is about one order of magnitude smaller than that of flip chip solder joints, and the volume is 1000 times smaller. Its microstructure and in turn its properties will be anisotropic because the number of grains in a microbump becomes very small. Its statistical failure will have a wide distribution because of anisotropy, including early failure. This review addresses this issue and the remedy.

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1. Introduction

As the trend of miniaturization of large-scale-integration of circuits on Si chip technology is approaching the limit of Moore's law, microelectronic industry has been looking for ways to overcome or to extend the limit. One of the ways is to turn to 3D IC by combining chip technology and packaging technology. This is because the Moore's law for packaging technology, assuming there is one, has not reached its limit yet. If we just consider the diameter of solder joints, in today's flip chip technology, the diameter is about 100 μm, and the diameter of microbumps in 3D IC is now about 20 μm. It is possible that the solder joint diameter can be reduced to 1 μm, thus there is ample room in the near future for the packaging technology to advance.

In packaging technology, whether we have systems in packaging (SIP) or systems on chip (SOC), they are 3-dimensional structures. To stack Si chips, the industry is seriously developing the through-Si-via (TSV) technology and microbump technology [1,2]. The latter is used to join the vias between two TSV chips in stacking. Owing to the change in dimension and in geometry, the reliability issues in 3D IC packaging will be different from those in flip chip. The change in dimension is because the diameter of via is about 10 μm, so does the diameter of microbumps, and the change in geometer is because of 3D integration. Before we address the new reliability challenges, we consider the following five general questions regarding the transition from flip chip to 3D IC.

The first is that 3D IC by using wire bonding technology is much cheaper than that by using TSV plus microbumps, so why should we develop the latter? This question has been asked before when microelectronic industry was trying to develop flip chip technology since at that time wire bonding was widely used and was much cheaper. The answer is because of the number of I/O on the chip; in wire bonding the number is proportional to the linear dimension of the peripheral of the chip, which is $4l$ if l is the length of the edge of a chip. Typically, it is limited to about 400 wires or 400 I/O. On the other hand, in flip chip, the number of solder bumps will be proportional to the area of chip, l^2, so the number of I/O can be up to 10,000. The same argument applies to 3D IC; if a low number of I/O can serve the purpose, we use wire bonding. But if the device needs a large number of I/O, we have to use TSV and microbumps.

The second question is about joule heating; it will be very serious, so how to reduce it or conduct it away [3–6]? Upto now, there is no proven solution to this fundamental problem. While Cu TSV is used for electrical interconnect between stacking chips in 3D IC, some of them can be used for heat conduction since Cu is a good electrical and thermal conductor. Thus, we can have two kinds of TSV; one kind is electrical TSV and the other kind is thermal TSV. The latter will require thermal contacts. Since thermal conduction depends on temperature gradient, thermomigration can occur and it will become important in the reliability of thermal contacts as well as in thermal interfacial materials (TIM). It is worth mentioning that a temperature difference of only 1 °C across a thickness of 10 μm results in a temperature gradient of 1000 °C/cm, which is known to have caused thermomigration in Pb-free solders at the operation temperature of 100 °C [7–10]. On the other hand, a practical approach to deal with the heat problem is to begin with a stacking of only two to three Si chips so that the problem will not be too serious. We need to learn to overcome it step by step before we jump to the stacking of a large number of chips.

* Corresponding author.
E-mail address: kntu@ucla.edu (K.N. Tu).

0026-2714/$ - see front matter © 2012 Elsevier Ltd. All rights reserved.
http://dx.doi.org/10.1016/j.microrel.2012.07.029

The third question is while the size of microbump is reduced, the temperature and time of processing is not, for example, the temperature and time of reflow will be more or less the same as that used in processing flip chip solder joints. Then, what will be the consequence? The consequence is that the relative amount of intermetallic compound (IMC) formed between solder and under-bump-metallization (UBM) will be greatly increased [11–13]. Also this is because while we reduce the thickness of solder, we do not reduce the UBM thickness in proportion. The entire solder joint may transform completely to intermetallic. In the literature, this issue has been addressed [14,15]. Since the physical and reliability problems of IMC is not well known, more research and data on IMC will be needed in the near future.

The fourth question is about chip-packaging interaction. Whether or not it will be more serious in 3D IC than that in flip chip packaging? Chip-packaging interaction is due to different thermal expansion coefficients between the Si chip and the polymer-based packaging substrate. The flip chip solder joints join the two. The cyclic thermal stresses in device operation will be transmitted to the on-chip multi-layered interconnects through the solder joints, especially those joints at the corners of the chip. When SiO_2 was the dielectric layer on multi-layered Al interconnects and when the solder was eutectic SnPb, the soft solder joints will absorb most of the stresses. Since SiO_2 is rather hard and strong, the reduced thermal stress did not cause cracking or dilamination of the dielectric. However, when low *k* dielectric was introduced to form the Cu/low *k* multi-layered interconnect systems and when a harder Pb-free solder replaces the soft SnPb eutectic, most of the thermal stresses are transmitted to the multi-layered interconnect and has caused cracking of the low *k* dielectric and breakdown of the Cu/low *k* interconnects [16,17]. Because of this reliability problem, microelectronic packaging industry has developed the so-called 2.5D IC technology, in which a passive TSV interposer is inserted between the active Si chip and the substrate [12]. The thermal stress between the active Si chip and the interposer is much reduced because both are Si. Thus, we expect that the chip-packaging interaction in 3D IC is similarly reduced. However, since joule heating is more serious in 3D IC, thermal stress remains a key concern.

The fifth question concerns the anisotropic properties of small solder joints. When the diameter is reduced by 10 times, from 100 μm to 10 μm, the volume is reduced by 1000 times. Thus, if we consider an extreme case in which the grain size is assumed to be 10 μm, the microbump may have only one grain, but the flip chip solder joint will have 1000 grains. In the latter case, we can assume the properties of the solder joint to be isotropic because of the large number of grains, but in the former case, we cannot.

Since Sn has a body-centered tetragonal crystal structure, it has anisotropic properties, for example, its conductivity is anisotropic. In transforming Sn to Cu–Sn or Ni–Sn intermetallic compound (IMC), the IMC has anisotropic crystal structure too [18,19]. This is a concern because it means that among a large number of microbumps on a TSV chip, the properties of each of the microbumps can be different. From the point of view of reliability, it could mean a wide distribution in failure statistics, so some microbumps could have early failure. Thus, it is important to control the microstructure or the grains of every microbump on a TSV chip in order to have a uniform microstructure in all of them. However, there are hundreds or even thousands of microbumps on a TSV chip, how to do so is challenging.

In this review, we shall concentrate on the issue of IMC in microbumps and how to control their formation in order to have an oriented growth and in turn a uniform microstructure in all the microbumps.

2. Effect of size reduction of microbumps on Sn whisker formation

Fig. 1a is a schematic diagram of the cross-sectional view of half a microbump, consisting of a 10 μm thick layer of Sn–Ag on a thick Cu UBM. To form a microbump, we shall flip one of them up-side down and join it to another one. Before joining, we reflow the solder to form a cap on the Cu. Fig. 1b is an SEM image of the solder cap after reflow and after storage at room temperature for a while. Whiskers of Sn formed on the cap surface. Since the spacing between microbumps is small, one of the whiskers is shown to have bridged two neighboring microbumps and it could become an electrical short.

It is known in lead-frame technology that the plating of a layer of Sn or SnCu as surface finish on lead-frames of Cu has often shown Sn whisker growth [20,21]. When the layer thickness of Sn or SnCu is about 10 μm, it is about the optimal thickness for Sn whisker growth. The driving force of spontaneous Sn whisker

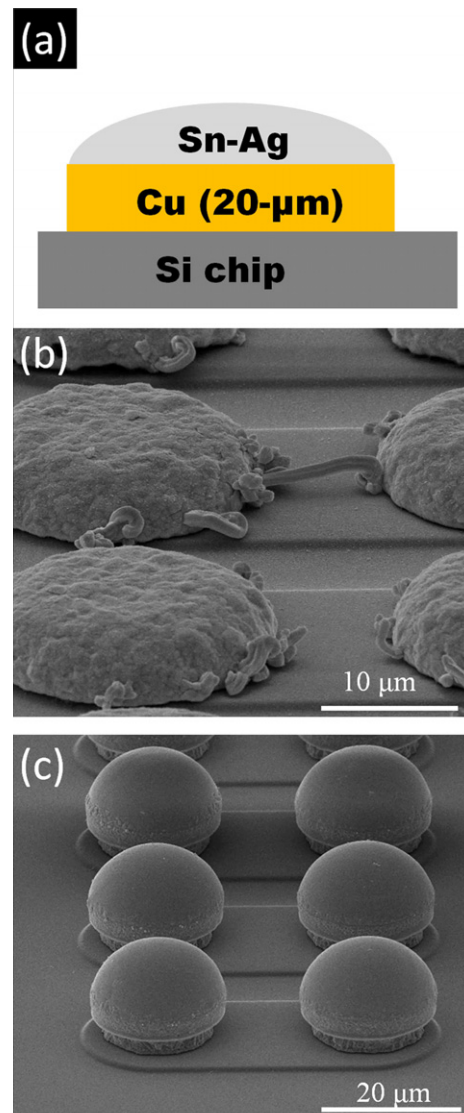


Fig. 1. (a) A schematic diagram of the cross-sectional view of half a microbump, consisting of a 10 μm thick layer of Sn–Ag on a thick Cu UBM. (b) SEM image of the solder cap after reflow and after storage at room temperature for a while. Whiskers of Sn formed on the cap surface. (c) SEM image of a very smooth surface after reflow and no whisker growth was found.

growth is due to room temperature reaction between Sn and Cu to form Cu_6Sn_5 IMC in Sn, the compressive stress induced by IMC formation is relaxed by the diffusion of Sn to grow a stress-free whisker on the finish surface. The compressive stress gradient in a Sn layer of about 10 μm thick is most effective for the stress migration in Sn whisker growth. On the other hand, in Pb-free flip chip solder joints of 100 μm on Cu UBM, very few Sn whiskers have been observed.

To prevent Sn whisker growth on microbumps, a diffusion barrier layer of Ni is plated between the Cu and the Pb-free to prevent the Cu–Sn reaction. Fig. 1c shows the SEM image of a very smooth surface after reflow and no whisker growth was found. While the intermediate layer of Ni has prevented Cu_6Sn_5 formation and Sn whisker growth, it nevertheless has made the microbump more brittle.

3. Effect of size reduction of microbumps on IMC formation and transformation

Fig. 2a is a schematic diagram of the cross-sectional view of forming a microbump by joining the upper half and the lower half of the half-structure depicted in Fig. 1a. On IMC formation in such a microbump, we shall consider two issues which are not found in flip chip solder joints. Since the physical spacing between the upper and lower UBMs across a microbump is small or the physical spacing between the two solder/UBM interfaces is just about 10 μm, the first question we ask is that how long does it take to allow the IMC scallops growing from the upper side and from the lower side to touch each other. In other words, how long will it take to grow the average scallops to 5 μm in radius? This question is important in the sense that when scallops touch each other, the vertical dimension of the microbump is fixed. Subsequently, if any force tends to change the dimension, stress will be induced. In addition, when the scallops of Cu_6Sn_5 stop growing, the growth of Cu_3Sn between Cu_6Sn_5 and Cu will become fast. Since the growth of Cu_3Sn will lead to Kirkendall void formation [22], this is a reliability concern, especially when the supply of Cu is plenty.

The second question we ask is what will be the chemical interaction between the two interfaces? Due to the small spacing between them, atomic diffusion takes very little time to go from one side of the solder/UBM interface to the other side in the molten state as well as in the solid state. The two interfaces in a microbump can communicate with each other much faster than those in flip chip solder joints.

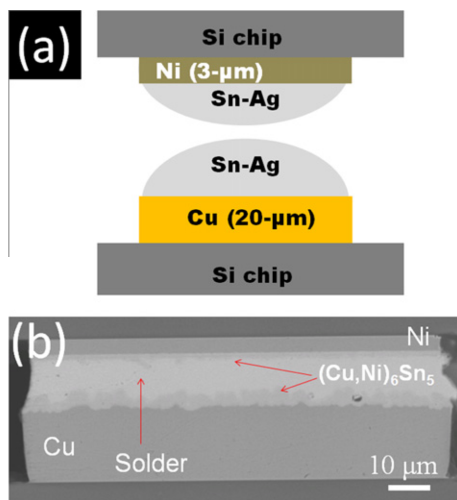


Fig. 2. (a) Is a schematic diagram of the cross-sectional view of forming a microbump by joining the upper half and the lower half of the half structure depicted in Fig. 1a. (b) Cross-sectional SEM image of a microbump which has had Cu UBM on one side and Ni UBM on the other side. After reflow, ternary SnNiCu IMC formed on both sides.

To answer the first question, we recall that the growth rate of Cu_6Sn_5 scallops in the reaction between eutectic SnPb and Cu at temperature around 200 °C has been measured [23], and it will take about 30 min to grow hemispherical scallops of 5 μm in radius. If we assume this rate for microbumps, a longer annealing will lead to fast growth of the Cu_3Sn phase.

To answer the second question on the interaction between the two interfaces across the microbump, it can be seen clearly if we have Ni UBM on one side and Cu UBM on the other side. When Ni diffuses to the other side and vice versa, we can detect the interaction directly due to the formation of ternary IMC. What will happen in IMC formation is that the ternary SnCuNi compound is more stable than the binary IMC of SnCu or SnNi, so we expect ternary IMC to form on both interfaces. Furthermore, $(Ni, Cu)_3Sn_4$ is less stable than $(Cu, Ni)_6Sn_5$, so the latter will be the dominant ternary IMC to form in microbumps, provided that both Cu and Ni are available. Thus even if $(Ni, Cu)_3Sn_4$ forms first on the Ni UBM side, it will transform to $(Cu, Ni)_6Sn_5$ later. Fig. 2b is a cross-sectional SEM image of a microbump which has had Ni UBM on one side and Cu UBM on the other side. Upper reflow, we found $(Cu, Ni)_6Sn_5$ on both sides, and it indicates the interaction between the two sides of the microbump.

The interaction is affected by the asymmetry of the microstructure across the microbump. However, even if the design of the microstructure is symmetrical, it becomes asymmetrical when the device is powered because the electric current flow across the microbump is not symmetrical due to the anode and the cathode. Electromigration induced phase change will be asymmetrical; it is different between the anode and the cathode of the solder joint. Actually, electromigration will accelerate the IMC formation at the anode. The effect of electromigration on IMC formation in microbumps will not be covered in this review.

4. The control formation of oriented IMC in microbumps

The number of grains in the Pb-free microbump before IMC formation as well as grains in the IMC after formation will be small, may be just a few grains, so we expect anisotropic behaviors. It is known that the diffusion of Cu and Ni in Sn is anisotropic, the diffusivity along the *c*-axis is about two to three orders of magnitude faster than that along the *a*- and *b*-axis [24,25]. Thus the formation of IMC on a c-axis oriented Sn grain will be much faster than that on *a*-axis or *b*-axis oriented Sn grain [26]. Due to such anisotropic behavior, the grain orientation and the distribution of grain orientation in all the microbumps on a TSV chip are of concern. We ask whether or not we can control the orientation of the small number of Sn grains as well as the IMC grains in microbumps. The answer is yes and it can be done; we start from the control of grains in Cu UBM by forming (1 1 1) oriented nano-twins in the Cu.

The crystal structure of a face-centered-cubic metal such as Cu can be represented by a stacking of (1 1 1) planes in the sequence of ABCABC. When an error of stacking occurs and changes the stacking to ABCACBA, where the middle plane of A is a mirror of atomic planes on both sides, a twin is formed. The stacking error increases the internal energy of the crystal only slightly because each atom in the twin plane still has 12 closely packed nearest neighbors, thus twin is considered as a coherent planar defect of low energy. The energy increase is of the order of a stacking fault. Copper has a low stacking fault energy and twin energy, so even an ordinary piece of bulk Cu tends to have micro-twins, meaning the twin plane spacing is of the order of microns.

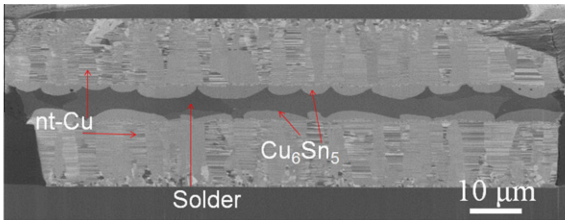


Fig. 3. SEM cross-sectional view of a microbump formed with the oriented nano-twin Cu as the top and the bottom UBMs.

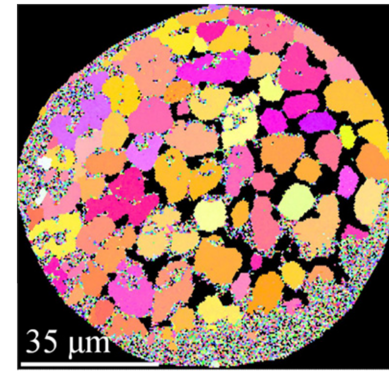
Recently, a high density of nano-twins has been produced in bulk size Cu by pulsed electroplating [18]. However, to form a high density of them having nano spacing between twin planes will require a certain amount of formation energy to be compensated. It has been proposed that the strain energy stored in Cu during electroplating is traded to form the nano-twins [27,28]. We recall that in thin film deposition, it is known that even when a thin film is deposited and kept at room temperature, intrinsic stress or strain is found. Experimentally, it was found that at a high plating rate of deposition at a low temperature, most of the deposited atoms are jammed into non-equilibrium position. If there is not enough time and thermal energy for them to relax to the lowest equilibrium position, stress builds up. Indeed, by using first principle calculation, it was found that nano-twins can be formed with just a reasonable amount of strain energy in Cu. On the other hand, it is very unlikely to have nano-twins in Al since its twin energy is very high, so the amount of strain energy needed will be too high in order to compensate for nano-twin formation.

Since the twin plane is (1 1 1) plane of Cu and if we can have this plane to be parallel to the substrate surface during electroplating, we have a uni-directional growth of (1 1 1) oriented Cu film or a highly textured (1 1 1) Cu film. We might say that it is the second best to a bulk single crystal of (1 1 1) oriented Cu. Indeed, the (1 1 1) oriented nano-twin Cu thin films have been obtained by sputtering [29]. In electroplating, we can also do so by using a seeding layer to enhance the nucleation of ⟨1 1 1⟩ oriented Cu nuclei on a given substrate, for example on a Si wafer, then the oriented growth of ⟨1 1 1⟩ nano twins can be enhanced by a high rate of rotation of the Si wafer or the electrolyte during plating [30]. The axis of rotation is the normal of the wafer as well as the normal of the ⟨1 1 1⟩ twin plane.

The beneficial effect of the rotation is that it cools the wafer and keeps the surface temperature of the wafer constant. In addition, since it produces a shear force between the wafer and the plating solution, the shear force not only will remove any gas or bubble formation on the film surface, but also will create instability of Cu adatoms on the film surface, the (1 1 1) plane, so that the probability of stacking error for twin nucleation is enhanced.

We recall that when (1 0 0) and (1 1 1) oriented single crystal Cu was used as substrate to study IMC formation with molten solder, the oriented Cu_6Sn_5 with roof-top shape or prism-type was observed on both (1 0 0) and (1 1 1) Cu [31,32]. On (1 0 0) oriented single crystal Cu, the oriented Cu_6Sn_5 grains are elongated along two perpendicular directions. On (1 1 1) oriented single crystal Cu, the oriented Cu_6Sn_5 grains are elongated along three preferential directions with 120° separation. The orientation relationship between Cu_6Sn_5 and (1 0 0) Cu and (1 1 1) Cu were determined and published. They will not be repeated here. When solder was reflowed on the (1 1 1) oriented nano-twinned Cu, we found similarly oriented growth of Cu_6Sn_5.

Fig. 3 shows the cross-sectional view of a microbump formed with the oriented nano-twin Cu as UBM. The layered microstructure in both the upper and the lower UBM are the oriented nano-twins. The scallops are the Cu_6Sn_5 IMC. When the scallops from the upper and the lower UBM touched each other, they joined to form columnar grains and surprisingly that there does not seem to have a grain boundary between the upper and the lower Cu_6Sn_5 grains. It is possible that ripening has occurred between them. This observation has also been reported in the literature [33]. Between the Cu_6Sn_5 scallops and the nano-twins, there is a layer of Cu_3Sn. Whether the formation of Cu3Sn will affect the orientation of Cu_6Sn_5 is an interesting question. The effect is small. This is because during the wetting of molten solder on Cu, the first phase to form is Cu_6Sn_5, thus the orientation of Cu_6Sn_5 scallops is affected directly by the Cu UBM. The subsequent formation of Cu3Sn between the Cu and Cu6Sn5 may tilt or rotate the latter a little bit.



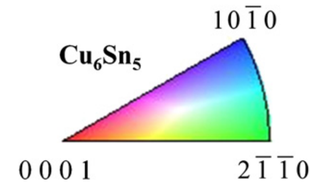


Fig. 4. Top view of the scallops taken from a cross-section of a microbump parallel to the substrate, and we obtained a view of all the scallops formed within a the microbump of diameter of 20 μm.

Fig. 4 is top view of the scallops taken from a cross-section of a microbump parallel to the substrate, and we obtained a view of all the scallops formed within the microbump of diameter of 20 μm. By using EBSD, we can determine that all the Cu_6Sn_5 grains have nearly the same orientation. In other words, their normal has nearly the same axis.

What is of interest in Fig. 3 is to compare the microstructure of Cu_6Sn_5 to that of Cu_3Sn. While the latter is thinner and has a large number of small grains, its polycrystalline microstructure is very clear. On the other hand, the Cu_6Sn_5 has much larger grains, and each scallop seems to be a single grain. In particular, their microstructure looks the same, at least from their appearance they look alike. In addition, when the upper Cu_6Sn_5 joined the lower Cu_6Sn_5, they seem to have merged into one grain; there does not seem to have a grain boundary between them, which is a phase change needs to be carefully studied.

5. Summary

In summary, due to a small number of grains in the microbump, microstructure anisotropy is expected to be a reliability issue. It will lead to a wide distribution of statistical failure, especially the early failure, of the large number of microbumps used in the TSV technology. The issue of anisotropy can be overcome by introducing the controlled growth of oriented nano-twins in Cu UBM. The oriented nano-twins will enable the uni-directional growth

of Cu_6Sn_5 IMC in the microbumps. A uniform microstructure of all the microbumps can be achieved.

Acknowledgment

The author would like to thank Miss Tian Tian at UCLA and Dr. Taihong Chen at ITRI, Taiwan for Fig. 1b and c.

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