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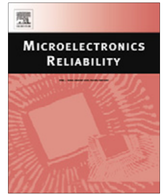

# Reliability of key technologies in 3D integration

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A B S T R A C T

3D IC packaging offers miniaturization, high performance, low power dissipation, high density and heterogeneous integration. Through-silicon via (TSV) and bonding technologies are the key technologies of 3D IC, and the corresponding reliability has to be well evaluated and qualified before real production applications. This paper reviews the emerging 3D interconnection technologies in worldwide 3D integration platforms with the latest reliability assessment results, including the reliability demonstration of Cu and oxide hybrid bonding in Ziptronix's platform, micro-bump and adhesive hybrid bonding in ITRI's platform, adhesive bonding followed by TSV formation in WOW alliance's platform, wide I/O interface TSV interposer in Xilinx's platform, and the active and passive TSV interposer in Samsung, TSMC and ASE's platforms. With low temperature bonding and TSV processes, optimized design and material selection to lower the induced stress and warpage, these platforms are successfully developed with enhanced reliability. The reliability of key technologies in 3D integration with these representative platforms are summarized in the paper to address the feasibility of 3D IC in mass production, which could be the guidelines for future development and applications of 3D integration technology.

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## 1. Introduction

Three-dimensional integrated circuits (3D ICs) has emerged as a promising solution beyond Moore's law to achieve system level integration with high function density, high performance, small form factor, and low power consumption. Various 3D integration platforms have been developed to realize with TSV and chip/wafer stacked bonding technologies [1–9]. Although each integration platform has innovations and benefits, cost and reliability are always the major concerns for considering as the real product applications. For instance, bonding interfaces are susceptible to failure due to structure and process induced stress. Crack or fatigue failure could be resulted from the CTE (Coefficient of Thermal Expansion) mismatch between Si and TSV. In addition, the thermal issue in 3D stacking structure, and the electro-migration issue in the ultra-fine electrical path are both the tough reliability problems in 3D IC. In this paper, the emerging 3D interconnection technologies in worldwide 3D integration platforms are studied with the reliability assessment demonstration, including the reliability of Cu and oxide hybrid bonding in Ziptronix's platform [10–14], micro-bump and adhesive hybrid bonding in ITRI's platform [15–17], adhesive bonding followed by TSV formation in WOW (Wafer-on-Wafer) alliance's platform [18–22], wide I/O interface TSV interposer in Xilinx's platform [23–26], and the active and passive TSV interposer in Samsung Electronics [27–29], TSMC [24,30] and ASE's [30–32] platforms. These 3D integration platforms could be the guidelines for future development and applications of 3D integration technology.

## 2. Reliability of Cu and oxide hybrid bonding

Ziptronix reported the copper and silicon oxide DBI (Direct Bonding Interconnect) hybrid bonding technology [10–14]. It utilizes the standard damascene processes to build the hybrid surface with exposed copper CMP (Chemical Mechanical Polishing) planar or dished topography about 2 nm below silicon oxide layer. TiW diffusion barrier liner is included in via and trench for reliability enhancement. Fig. 1 shows the process flow of DBI bonding technology [12]. By activating and terminating the CMP planarized oxide surface, the bonds can be formed at significantly low temperature, which enables the room-temperature direct oxide bonding with preserved alignment accuracy since no external heat and pressure applied. After bonding, 300–350 °C annealing is employed to improve the inter-wafer bond strength and the Cu–Cu contact quality. The fully functional serial daisy chains with 72500 and 463000 3D copper DBI interconnects on a 25 μm pitch with 125 °C heat treatment and 10 μm pitch with a 350 °C heat treatment were achieved, respectively [12]. Fig. 2 demonstrates the 10 μm pitch bonded structure using 4 μm size Cu DBI plugs and a TiW barrier liner [12]. The corresponding DBI contact resistance was about 50 mΩ and resistivity was achieved less than 0.45 Ω $\mu m^2$, respectively [12]. These parts passed the JEDEC

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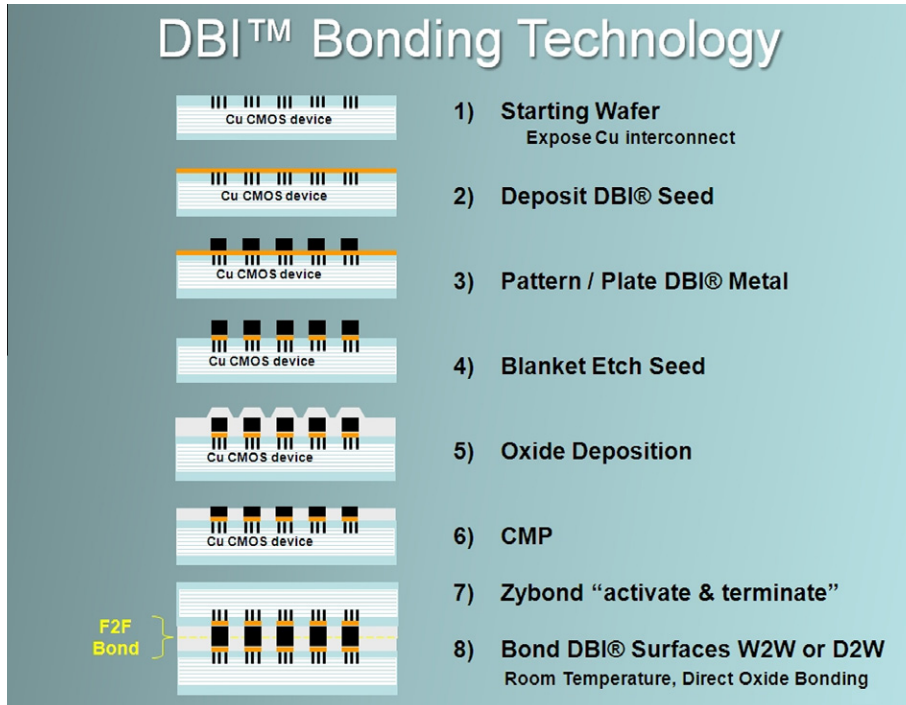


**Fig. 1.** The process flow of DBI bonding technology [12].

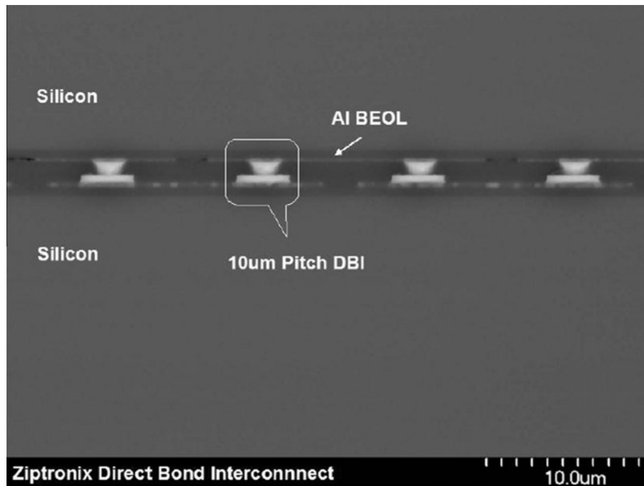


**Fig. 2.** 10 μm pitch direct bond interconnects from Ziptronix DBI technology [12].

**Table 1**
Ziptronix DBI interconnect reliability data [13].

| Test part | 50 μm pitch | 25 μm pitch | 10 μm pitch |
|---|---|---|---|
| Test part | 9,950 Serial connections | 72,500 Serial connections | 460,000 Serial connections |
| Typical resistivity | <20 mΩ (<1.5 Ω/μm$^2$) | <50 mΩ (<0.5 Ω/μm$^2$) | <50 mΩ (<0.5 Ω/μm$^2$) |
| Thermal cycling −65 °C to 175 °C | 1000 cycles, 18/18 pass 10,000 cycles, 9/9 pass | 1000 cycles, 5/5 pass 10,000 cycles, 4/4 pass | 1000 cycles, 10/10 pass |
| Hast (130 °C, 85% RH, 333 psi) | 96 h, 12/12 pass | 288 h, 6/6 pass | |

temperature cycling (−65 °C to 175 °C, 1000 cycles) and HAST (Highly Accelerated Stress Test) (130 °C, 85% RH, 333 psi) reliability assessment as Table 1 presents [13]. No failures were found as defined by a significant change in resistance of the daisy chain. With increasing the temperature cycling by 10 times to 10,000 cycles and HAST by 3 times to 288 h, no failures were detected. In addition, the electro-migration resistance of DBI connections was evaluated with a daisy chain (1 mm of total length and 8 μm of width) at a current density of $3 \times 10^6$ A/cm$^2$ for 100 h, showing no failures or significant change in resistance [13].

## 3. Reliability of micro-bump and adhesive hybrid bonding

ITRI has developed various micro-bump and assembly technologies for 3D IC applications [33–37], including Cu/Ni/Sn2.5Ag by conventional reflow process, Cu/Ni/Sn2.5Ag by thermo-compressive bonding (TCB), and Cu/Sn by solid liquid interdiffusion (SLID) bonding. Fig. 3a shows one example of the bonding schemes for investigation, and the micro-joint interconnects were subjected to reliability test for assessment and comparison [33]. Fig. 3b shows the Weibull analysis results of the three kinds of micro-joints for thermal cycle test [37]. The ranking of characteristic life (the intersection with the dotted line located on 63.2% in the Fig. 3b) is Cu/Ni/Sn2.5Ag (TCB) with 4980 cycles > Cu/Sn (SLID) with 3262 cycles > Cu/Ni/Sn2.5Ag (Reflow) with less than 1000 cycles. The micro-joint bonded by conventional reflow is not reliable enough due to the short lifetime. Although the average lifetime of the Cu/Sn intermetallic micro-joint is inferior to that of Cu/Ni/Sn2.5Ag micro-joint by TCB, the first failure of the former occurred when 1000 cycles passed. Compared to that of the latter of 200 cycles, Cu/Sn SLID bonding seems to be more beneficial to lead in the mass production to prevent the early failure of products [33,37]. The failure of Cu/Sn SLID bonding micro-joint was induced by the volume change resulted from the phase transformation as the Fig. 4 presents [37]. The intermetallic micro-joints formed by SLID bonding has a characteristic life of more than 3000 cycles under TCT because of a slight volume contraction (0.59%) elicited by the reaction $2Cu_3Sn + 3Sn \rightarrow Cu_6Sn_5$.

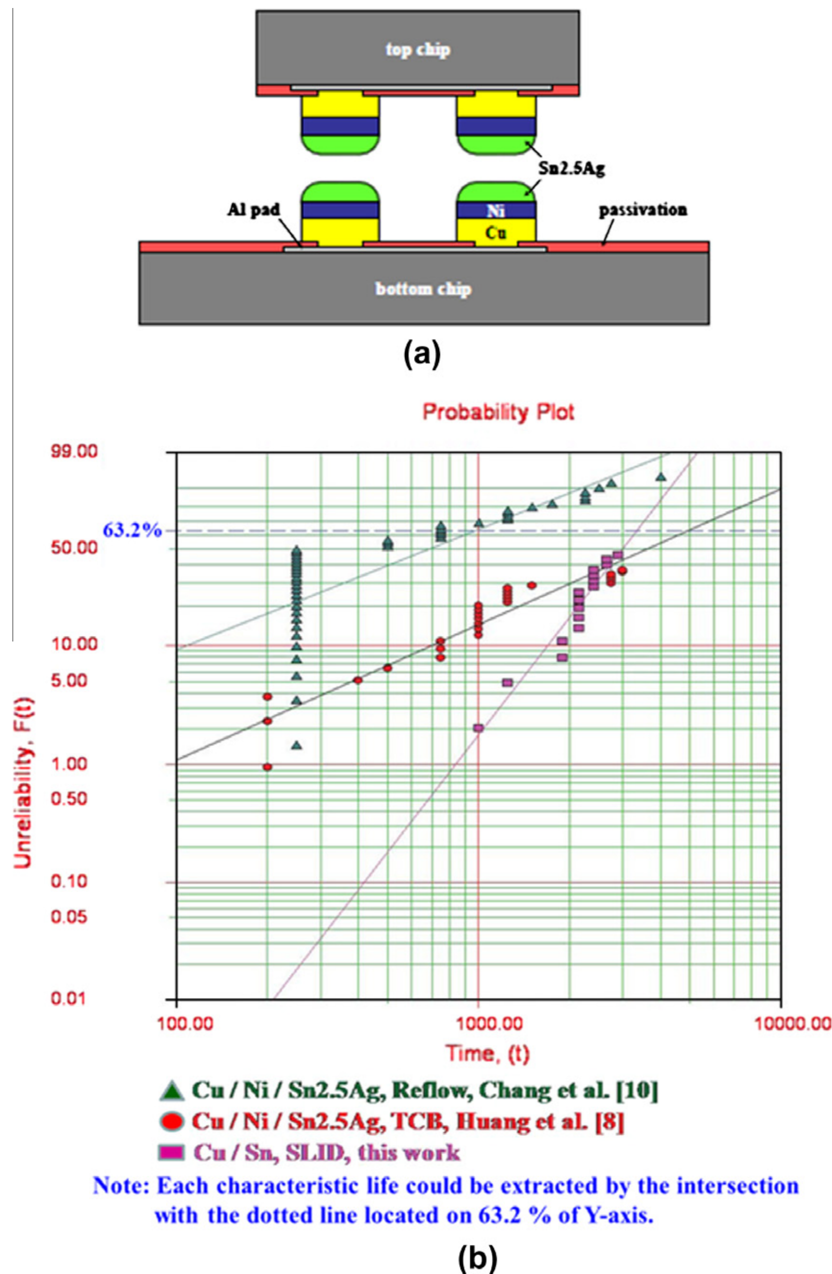


**Fig. 3.** (a) One example of the micro-bump bonding scheme for investigation, and (b) the Weibull analysis results of the three kinds of micro-joints conducted to TC test [33,37].

ITRI and NCTU reported a wafer-level carrier-less 3D integration platform using high reliable Cu/Sn micro-bump and Benezocyclobutene (BCB) adhesive hybrid bonding technology [15–17]. Fig. 5 shows the structure design and schematic process flow [16]. Cu/Sn micro-bumps are fabricated on bottom wafer and Cu TSVs of top wafer, respectively. Photo-definable BCB is subsequently spin-coated and lithographed to form the hybrid scheme before hybrid bonding at 250 °C. Cu/Sn micro-bump and BCB adhesive are adopted for low temperature hybrid bonding to achieve metallic interconnection with adhesive sealing around to enhance the reliability of the micro-joints, and serving reinforcement of the mechanical stability to stand the severe wafer thinning and backside processes. There is no carrier and thin wafer handling technique required in the 3D integration platform. Therefore, it is beneficial to simplify the process flow, decrease the production cost, and enhance the reliability of the stacked devices. Fig. 6 demonstrates the completed 3D integration scheme with Cu/Sn and BCB excellent hybrid bonding integrity. Herein 5 μm TSVs and 10 μm micro-bumps in 20 μm pitch were applied for 3D interconnection. The scheme was investigated after multiple current stressing and humidity test for reliability assessment [16].

Fig. 7 shows the characteristics of voltage and current on single 5 μm Cu TSV and 10 μm Cu/Sn micro-joint under multiple current stressing [16]. There is no apparent change between the characteristic curves, which implies the integration scheme has excellent electrical performance and stability even after 1000 cycles current stressing. The via chain samples were subjected to 1000 cycles of current stressing and humidity test under 45 °C, 100% humidity and 2 h conditions, and the results show excellent stability as well and passed both tests. The micro-joints are well protected from atmosphere with BCB perfect sealing performance. The assessment results indicate the 3D integration scheme possesses excellent

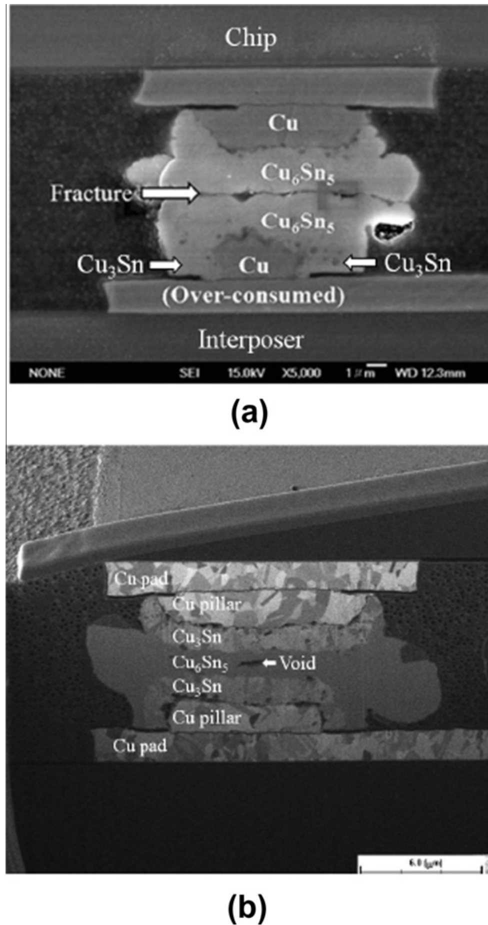


**Fig. 4.** (a) Cross-sectional image of the failed Cu/Sn SLID micro-joint, and (b) FIB analysis of the SLID micro-joint after TCT for 2650 cycles [37].

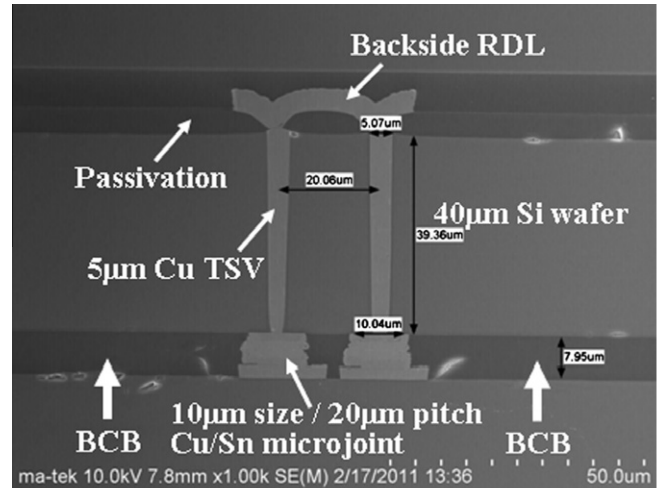


**Fig. 6.** The demonstration of the completed 3D integration scheme with Cu/Sn and BCB excellent hybrid bonding integrity [16].

reliability and electrical stability, and is potentially to be applied for the 3D IC applications [16].

## 4. Reliability of adhesive bonding with TSV formation

WOW (Wafer-on-Wafer) alliance reported using BCB adhesive bonding followed by low temperature TSV fabrication approach for 3D integration [18–22]. Fig. 8 shows the process flow of WOW stacking method [19]. The secondary wafer (Si 2) with transistors and interconnect metallization is temporarily bonded with support glass before thinning down to less than 20 μm. This wafer is then permanently bonded to the primary wafer (Si 1) with BCB adhesive. After removing the support glass from the wafer stack, TSV and RDL are subsequently fabricated by Cu dual-damascene

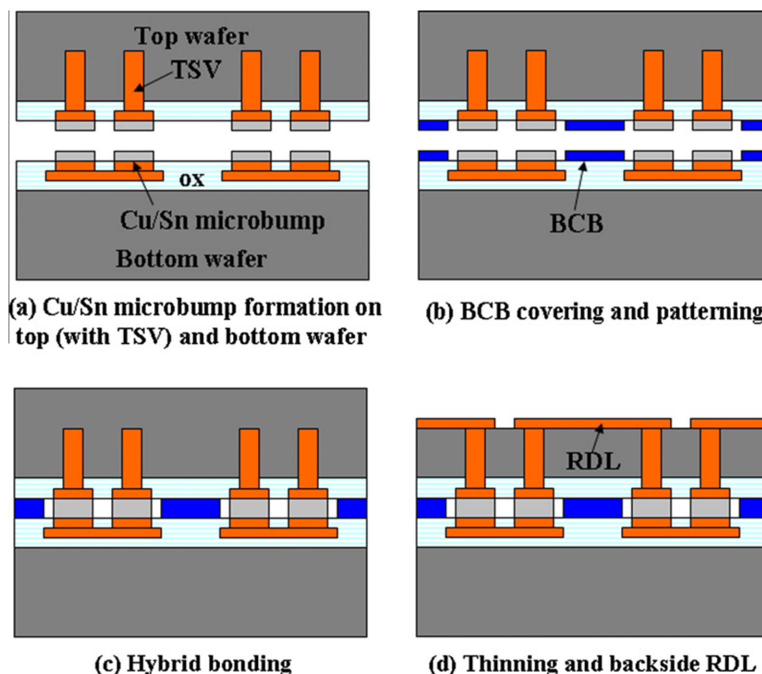


**Fig. 5.** The structure design and schematic process flow of ITRI's 3D integration platform [16].

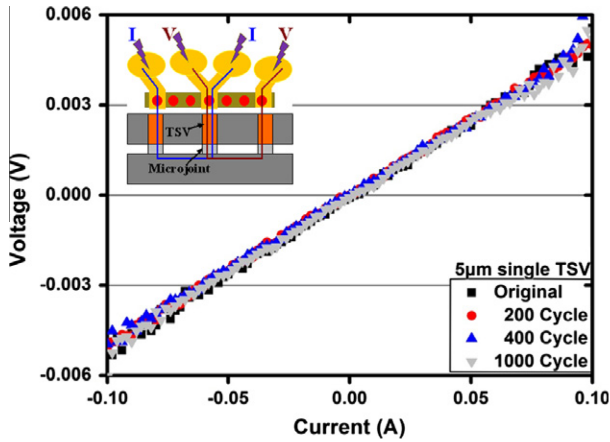


**Fig. 7.** The characteristics of voltage and current on single 5 μm Cu TSV and 10 μm Cu/Sn micro-joint under multiple current stressing [16].

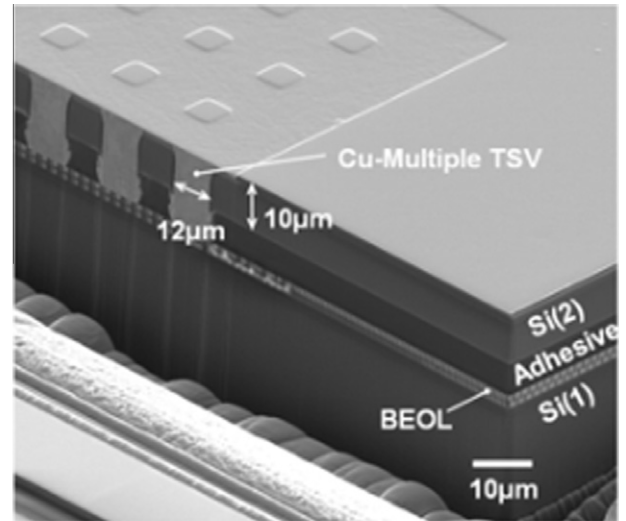


**Fig. 9.** The FIB–SEM image of stacked wafers and multiple TSV on BEOL device [21].

processes [19]. Fig. 9 shows the FIB–SEM (Focused Ion Beam Scanning Electron Microscope) image of stacked wafers and multiple TSV on BEOL device [21]. Herein 150 °C low temperature TSV process was applied to reduce the pumping stress on Cu TSV for reliability enhancement.

Fig. 10 shows the calculation results of the pumping height in TSV with varied thermal stress [21]. The pumping stress induced by CTE mismatch at the dielectric film in TSV decreases with reduced via size and process temperature. Cu diffusion profile in the dielectric layers was analyzed by BS-SIMS after annealing at 400 °C, 10 h for thermal aging [21]. As the results shown in Fig. 11 [20], Cu diffusion increased with decreasing deposition temperature, but the SiON film deposited by PECVD at the low temperature of 150 °C was sufficient to be a barrier layer against Cu diffusion in TSV. Cu diffusion rate is evaluated as a function of film density relative to the value of bulk $Si_3N_4$ and $SiO_2$ calculated using Cu depth profiles. The rate becomes higher in lower density film formed at lower deposition temperature. In case of density below 50%, the dielectric layer thicker than 1000 nm is recommended to suppress the Cu diffusion into Si substrate [20]. Thermal stress test evaluation using Cu TSV and BEOL chain contact was carried out with −55 °C to 125 °C temperature cycling. As the results shown in Table 2 [21], there was no open failure and significant resistance change in the Cu interconnects with TSV process after 1000 cycles of TC testing by using 150 °C LT-PECVD (Low-Temperature Plasma Enhanced Chemical Vapor Deposition) dielectric film. The LT-TSV (Low Temperature Through-Silicon via) process can lower the overall process temperature and induced stress, and is suitable to be applied for high reliable TSV structure for the wafer-level 3D stacking [21].

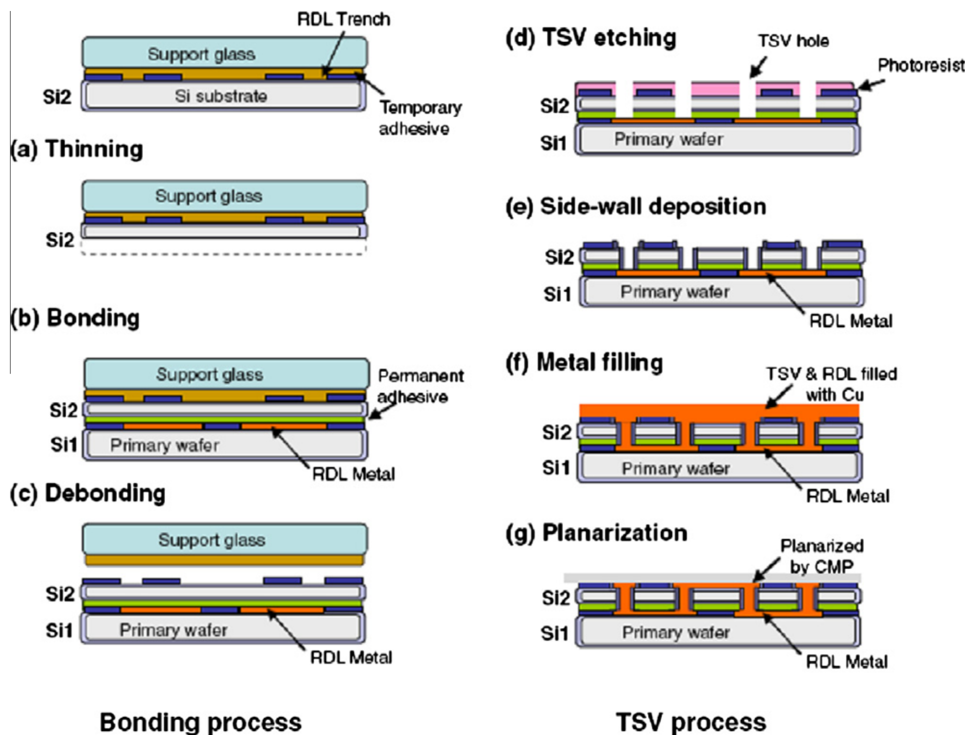


**Fig. 8.** The process flow of WOW stacking method [19].

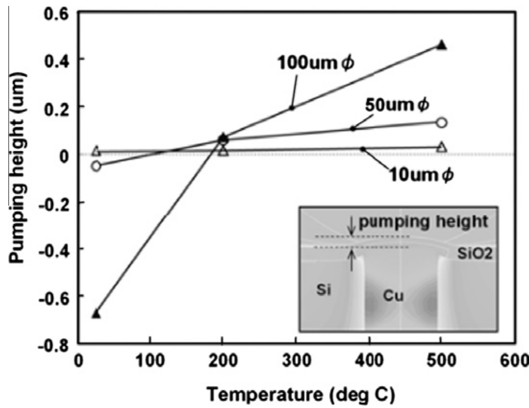


**Fig. 10.** The pumping height in TSV with varied process temperature [21].

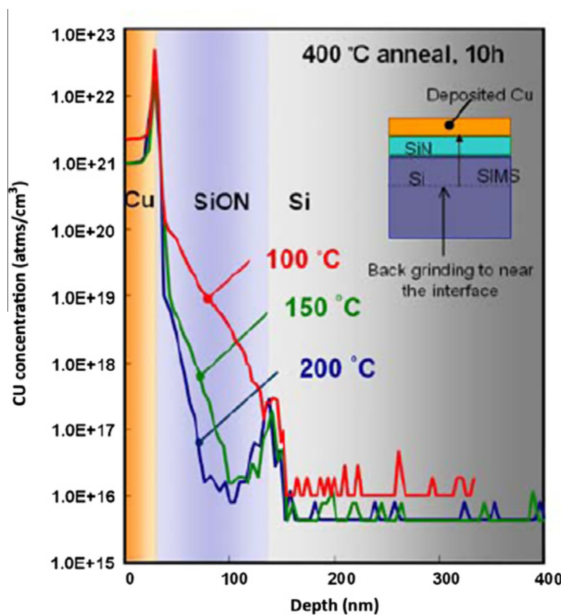


**Fig. 11.** SIMS depth profile of Cu diffusion in SiON barrier layer of TSV [20].

**Table 2**
Resistance change of Cu-TSV and BEOL interconnects after TC testing [21].

| | Before TSV process | After TSV process | After TC 1000 cycle |
|---|---|---|---|
| 0.4 μm dense chain (Ω) | 1.04E + 05 | 1.00E + 05 | 1.01E + 05 |
| 3 μm single line (Ω) | 10.02 | 10.04 | 9.97 |

## 5. Reliability of TSV interposer

The conventional flip chip packaging with the organic IC substrate is facing great challenge in ultra fine pitch wiring fabrication as the interconnect density becomes higher and higher. TSV interposer has emerged as a promising solution to provide high wiring density interconnects, improve electrical performance, and minimize CTE mismatch between the Cu/low-k die and the TSV interposer for reliability enhancement. Xilinx has reported the development of wide I/O interface TSV interposer technology for a 4-slice high performance 28 nm FPGA (Field Programmable Gate Array) dies mounted on a large TSV interposer (manufactured by TSMC) [23–26]. Fig. 12a and b shows respectively the schematic package configurations and completed overall assembly SEM images [25,26]. To maximize the yield and reliability, several DOEs have been performed to optimize design and material selection with 3D thermal–mechanical modeling and simulation analysis. The μ-bump and C4 solder reliability were evaluated with simulated strains, inelastic energy and fatigue. The results indicate that μ-bump and C4 solder undergo acceptable reliable solder inelastic strain and fatigue as Table 3 summarizes [25]. One detailed local model was built to study TSV stress in detail. The results shown in Table 4 indicates that the overall stresses in Si, $SiO_2$ and Cu via are below fracture toughness of these materials with no delamination or fracture risk for the TSV interposer [25]. The samples with adequate underfill, improved gap height, and plasma cleaning, were subjected to temperature cycling from −55 °C to 125 °C. There was no delamination observed either in level 5 preconditioning or after 264 h of HAST at 110 °C. All the samples passed 1000 cycles of TCB without Cu protrusion of TSV, as one SEM image shown in Fig. 13. It is suggested that this developed TSV interposer is a desirable 3D path to have a reliable package for high density interconnection, and has been proven in high-volume production [25].

The worldwide leading manufacturers, such as Samsung Electronics [27–29], TSMC [24,30] and ASE [30–32], have worked in the development of TSV interposer technology. Table 5 summarizes and compares their technology platforms. Samsung focuses on the field of wide I/O memory and wide I/O DRAM application, therefore the active interposer is fabricated by forming TSVs on CPU or Logic devices. Lots of reliability issues are concerned as forming TSVs on active devices, because TSV stress (due to CTE mismatch between Cu (∼17 ppm) and Si (∼3 ppm)) and Cu contamination (due to Cu diffusion) may damage the CMOS layer, and TSV stress induced Cu extrusion may cause the low-k IMD (Inter-Metal Dielectric) crack or interface delamination happened [27,29]. Samsung has reported the less stress induced by the smaller TSV size. As the results shown in Fig. 14, TC 1000 cycles could be passed without IMD crack or interface delamination as the Cu extrusion height was controlled less than 0.2 μm [29]. Table 6 shows the TSV proximity impacts on 45 nm CMOS devices [27]. Impact on TSV was observed in less than 2 μm distance only, and the amount of changes caused by TSV is very small (2% in maximum). Long channel looks more sensitive than short channel, and NMOS looks more sensitive than PMOS. In addition, no significant impact was found in thin_short_NFET and off-current. Regardless of the TSV positions, $I_{dsat}$ is decreased for NFET and increased for PFET by TSV.

TSMC and ASE have developed 2.5D and 3D IC technologies with passive interposer, which eliminates above issues because TSVs are formed on passive device. TSMC has developed 2.5D interposer for Xilinx for wide I/O interface application [24]. As aforementioned, the developed TSV interposer shows excellent reliability. In March 2012, Altera and TSMC announced to develop the world's first heterogeneous 3D IC test vehicle using TSMC's Chip-on-Wafer-on-Substrate (CoWoS) integration process [30], an integrated technology that attaches devices to a wafer through the chip on wafer (CoW) bonding process, following by attaching CoW chip to the substrate to form the final component. By attaching the device to the original thick wafer before the fabrication process, manufacturing-induced warpage could be avoided. TSMC plans to offer CoWoS as a turnkey manufacturing service. ASE developed TSV structure with polymer isolation for 2.5D silicon interposer, which shows the features of low temperature fabrication process, low warpage, and low leakage with minimized TSV parasitic parameters [30–32]. Fig. 15 presents the 2.5D Si interposer assembly process flow and package prototype [32]. Herein the simplified direct reflow flip chip assembly process is adopted to minimize the cost. The interposer

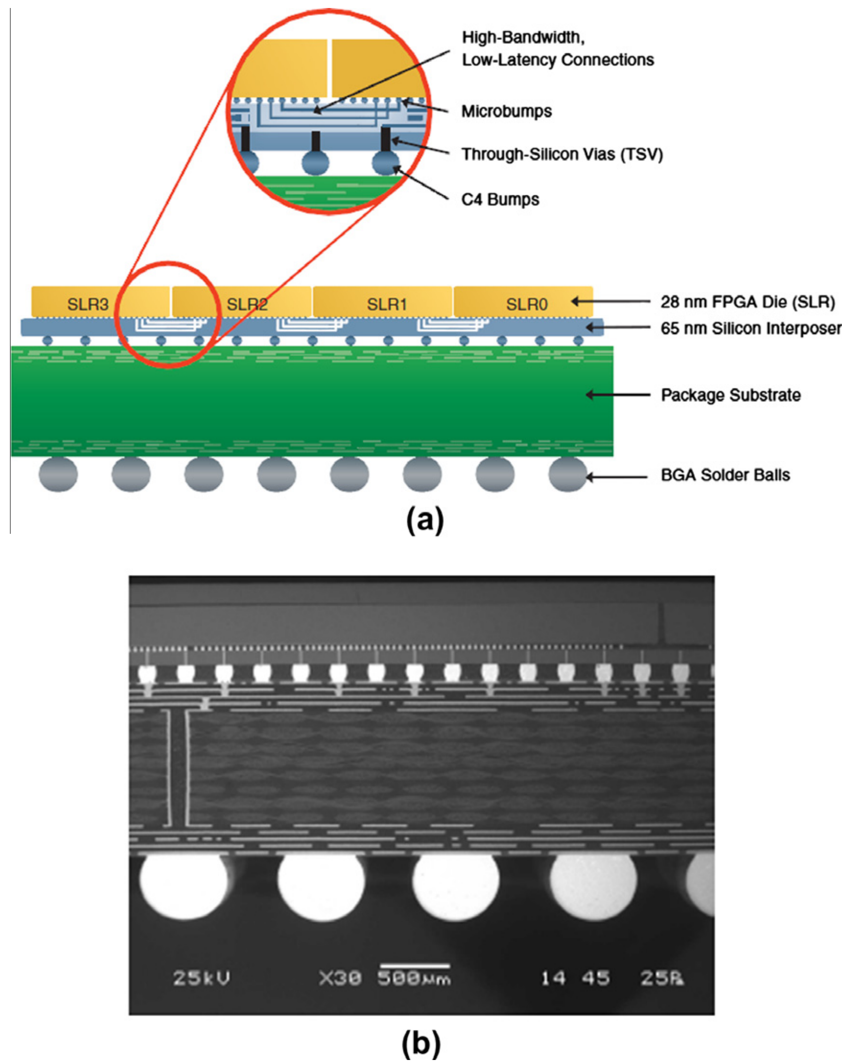


**Fig. 12.** (a) The schematic package configuration, and (b) the overall assembly SEM image of TSV interposer [25,26].

**Table 3**
Summary of solder fatigue study in Xilinx TSV interposer [25].

| | After *x* cycles @ 125 °C | After *x* cycles @ −55 °C |
|---|---|---|
| μbump solder inelastic strains | 0.12 | 0.38 |
| μbump solder inelastic energy | 2.52 | 2.93 |
| C4 solder inelastic strains | 0.08 | 0.17 |

**Table 4**
TSV stresses in silicon interposer during −55 °C to 125 °C cycling [25].

| | Max in-plane stress (MPa) | Max shear stress (MPa) | Max out-of-plane stress (MPa) |
|---|---|---|---|
| Si | 127.5 | 4.28 | 82.10 |
| $SiO_2$ | 120.3 | 16.47 | 77.06 |
| Cu-TSV | 146.3 | 21.75 | 111.3 |

has been assessed and passed MSL3/260 °C precondition, followed by TCT condition-B 3000 cycles and HAST 504 h without failures.

## 6. Conclusions

The emerging 3D interconnection technologies in various 3D integration platforms are reviewed in the paper with the latest reliability assessment results, including the reliability demonstration of Cu and oxide hybrid bonding in Ziptronix's platform, micro-bump and adhesive hybrid bonding in ITRI's platform, adhesive bonding followed by TSV formation in WOW alliance's platform, wide I/O interface TSV interposer in Xilinx's platform, and the active and passive TSV interposer in Samsung, TSMC and ASE's platforms. Ziptronix activates the CMP planarized oxide surface to perform bonding at room-temperature and followed by annealing to improve the bond strength and Cu–Cu contact quality, and this scheme passes the TCT, HAST and electro-migration reliability test. ITRI adopts high reliable Cu/Sn SLID and BCB hybrid bonding at low temperature to perform carrier-less 3D integration platform, and this scheme passes multiple current stressing and humidity test assessment. WOW alliance develops 150 °C LT-TSV process with qualified LT-PECVD dielectric film to reduce the pumping stress on Cu TSV, which enhances the reliability. Xilinx develops wide I/O interface TSV interposer with several DOEs performed to optimize design and material selection for yield and reliability enhancement, and this scheme passes the HAST and TCB tests. The interposer technologies developed by Samsung, TSMC and

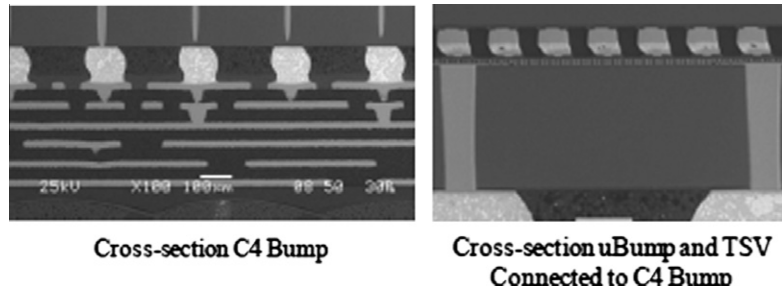


**Fig. 13.** Cross-sectional image of one sample after subjecting to 1000 TCB cycles [25].

**Table 5**
The comparison of TSV interposer technologies between Samsung, TSMC, and ASE.

| | Samsung [27-29] | TSMC [24, 30] | ASE [30-32] |
|---|---|---|---|
| Interposer type | Active | Passive | Passive |
| Application | • Wide I/O memory<br>• Wide I/O DRAM | • Wide I/O interface | • Wide I/O interface |
| Feature | • Wide bandwidth and low power memory on CPU/Logic or SoC with TSVs<br>• DRAM stacking with TSVs on Logic with TSVs | • Moore's law chips on a passive interposer with TSVs | • Moore's law chips on a passive interposer with TSVs |
| Scheme | Wide I/O Memory<br>1st die(LogicAP)<br>TSV<br>Set PCB | | |
| Announcement for commercialization | 2012 | 2H 2011<br>(2.5D interposer mass production already for Xilinx) | 2012-2013 |

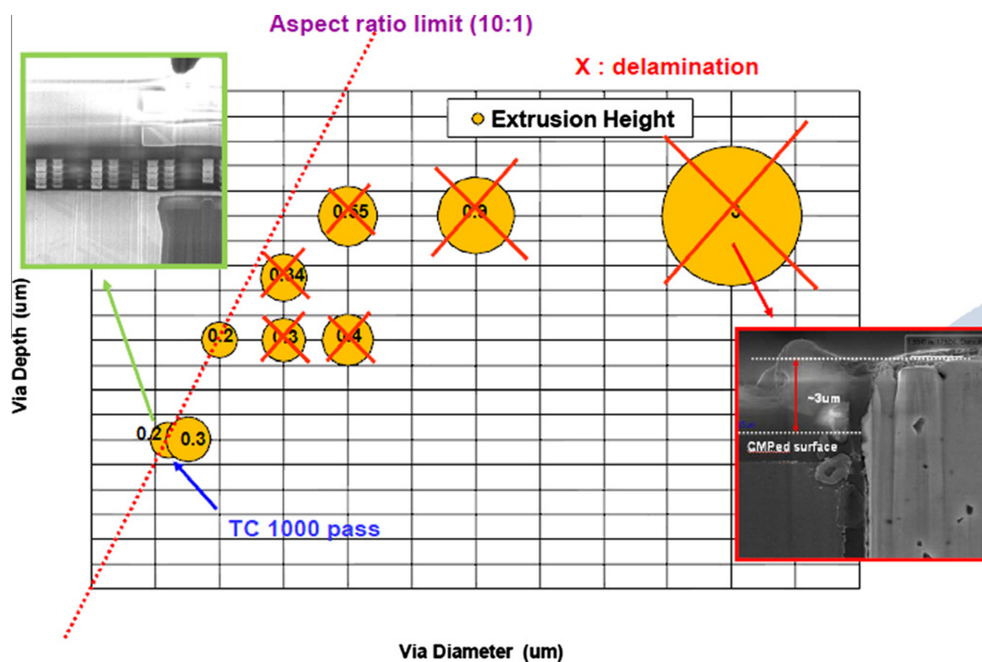


**Fig. 14.** The effects of via dimension on Cu extrusion height and interface delamination [29].

**Table 6**
The TSV proximity impacts on 45 nm CMOS devices [27].

| TSV position | Gate oxide | Channel | Impace/impacted distance | | | | | |
|---|---|---|---|---|---|---|---|---|
| | | | NMOS | | | PMOS | | |
| | | | $V_{th}$ | $I_{dsat}$ | $I_{doff}$ | $V_{th}$ | $I_{dsat}$ | $I_{doff}$ |
| Horizon | Thin | Short | X | X | X | X | X | X |
| | | Long | X | −/2 μm | X | X | +/2 μm | X |
| | Thick | Short | X | −/2 μm | X | X | X | X |
| | | Long | +/2 μm | −/2 μm | X | X | +/2 μm | X |
| Diagonal | Thin | Short | X | X | X | X | X | X |
| | | Long | X | −/1 μm | X | X | +/1 μm | X |
| | Thick | Short | X | −/2 μm | X | X | X | X |
| | | Long | +/1 μm | −/1 μm | X | X | X | X |
| Vertical | Thin | Short | X | X | X | X | X | X |
| | | Long | X | X | X | X | +/2 μm | X |
| | Thick | Short | X | −/2 μm | X | X | X | X |
| | | Long | +/2 μm | −/2 μm | X | X | X | X |

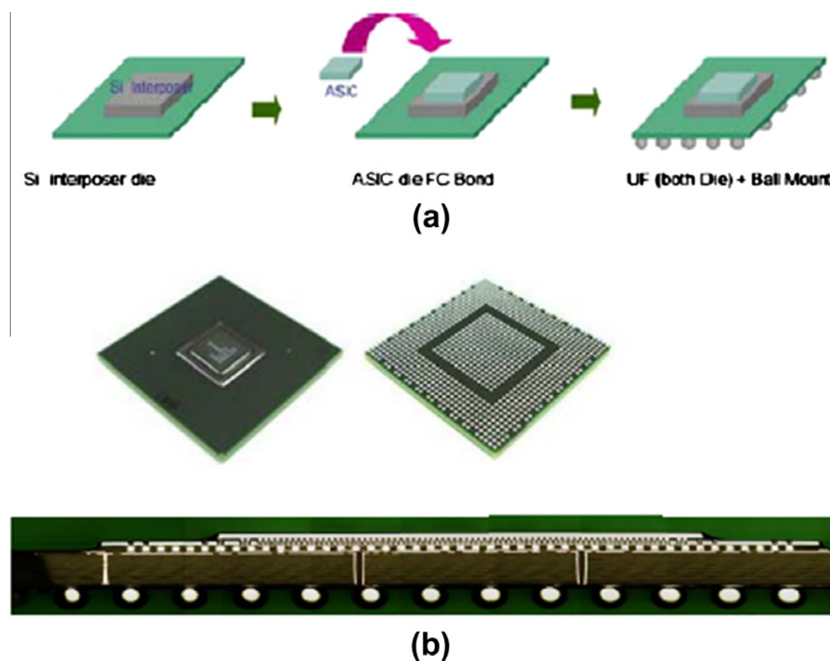


**Fig. 15.** ASE 2.5D Si interposer (a) assembly process flow and (b) package prototype [32].

ASE were introduced and compared as well. Samsung studies the impact influence of TSV induced stress and successfully develops the active interposer with well design of TSV size and position. TSMC and ASE develop 2.5D and 3D IC technologies with passive interposer with simplified process flow and low warpage to reduce cost and enhance reliability. The assessment results indicate that all of these emerging 3D interconnection technologies possess excellent reliability, and show the potential to be applied for 3D integration in real product applications. These 3D integration platforms could be the guidelines for future development and applications of 3D integration technology.

## References

[1] Jourdain A et al. Simultaneous Cu–Cu and compliant dielectric bonding for 3D stacking of ICs. In: Proceedings of IITC conference; June 4–6, 2007.
[2] Peter Ramm. European activities in 3D system integration – the e-Cubes project. In: 12th Annual Pan Pacific Maui; February 1, 2007.
[3] McMahon JJ, Chan E, Lee SH, Gutmann RJ, Lu J-Q. Bonding interfaces in wafer-level metal/adhesive bonded 3D integration. In: Electronic components and technology conference (ECTC); May 2008. p. 871–78.
[4] Garrou P. Handbook of 3D integration: technology and applications of 3D integrated circuits, vol. 2. Wiley-VCH; 2008.
[5] Liu F, Yu RR, Young AM, Doyle JP, Wang X, Shi L, et al. A 300-mm wafer-level three-dimensional integration scheme using tungsten through-silicon via and hybrid Cu-adhesive bonding. In: Proceedings of IEDM; 2008. p. 1–4.
[6] Jourdain A, Soussan P, Swinnen B, Beyne E. Electrically yielding collective hybrid bonding for 3D stacking of ICs. In: Electronic components and technology conference (ECTC); May 2009. p. 11–13.
[7] Taibi R, Cioccio LD, Chappaz C, Chapelon LL, Gueguen P, Dechamp J, Fortunier R, Clavelier L. Full characterization of Cu/Cu direct bonding for 3D integration. In: Electronic components and technology conference (ECTC), proc; 2010.
[8] Aoki M, Hozawa K, Takeda K. Wafer-level hybrid bonding technology with copper/polymer co-planarization. In: International 3D system integration conference (3DIC); 2010.
[9] Vos DJ, Jourdain A, Erismis MA, Zhang W, Munck DK, Manna LA, Tezcan DS, Soussan P. High density 20 μm pitch CuSn microbump process for high-end 3D applications. In: Electronic components and technology conference (ECTC), Lake Buena Vista, FL; May 2011. p. 27–31.
[10] Peters L. Ziptronix, raytheon prove 3-D integration of 0.5 μm CMOS device. Semiconductor international; April 6, 2007.
[11] Ye Z. Sensor/ROIC integration using oxide bonding. In: Proc. int. linear collider workshop (LCWS08 and ILC08); 2008.
[12] http://www.i-micronews.com/lectureArticle.asp?id=2009.
[13] Enquist P, Fountain G, Petteway C, Hollingsworth A, Grady H. Low cost of ownership scalable copper direct bond interconnect 3D IC technology for three dimensional integrated circuit applications. In: 3D system, integration (3DIC); 2009.
[14] Enquist P. Scalable direct bond technology and applications driving adoption. In: 3D system, integration (3DIC); 2011.

[15] Ko CT, Hsiao ZC, Fu HC, Chen KN, Lo WC, Chen YH. Wafer-to-wafer hybrid bonding technology for 3D IC. In: Electronic system-integration technology conference (ESTC); 2010.
[16] Ko CT et al. Wafer-level 3D integration with Cu TSV and micro-bump/adhesive hybrid bonding technologies. In: 3D system, integration (3DIC); 2011.
[17] Ko CT, Hsiao ZC, Chang YJ, Chen PS, Huang YJ, Fu HC, et al. A wafer-level 3D integration scheme with Cu TSVs based on micro-bump/adhesive hybrid bonding for 3D memory application. IEEE Trans Dev Mater Reliab 2012.
[18] Suzuki K, Maeda N, Kitada H, Fujimoto K, Nakamura T, Ohba T. TSV (through silicon via) interconnection on wafer-on-a-wafer (WOW) with MEMS technology. In: Proc. 15th symp. On microjoining and assembly technol. in, electronics; 2009. p. 283–5.
[19] Tominaga S, Abe D, Enomoto T, Kondo S, Kitada H, Ohba T. Hybrid electrochemical mechanical planarization process for Cu dual-damascene through-silicon via using noncontact electrode pad. Jpn J Appl Phys 2010;49(5):05FG01–5.
[20] Fujimoto K et al. Development of multi-stack process on wafer-on-wafer (WOW). In: The IEEE CPMT symposium Japan; 2010.
[21] Kitada H, Maeda N, Fujimoto K, Mizushima Y, Nakata Y, Nakamura T et al. Stress and diffusion resistance of low temperature CVD dielectrics for multi-TSVs on bumpless wafer-on-wafer (WOW) technology. In: Advanced metallization conference; 2010.
[22] Maeda N, Kim YS, Hikosaka Y, Eshita T, Kitada H, Fujimoto K, Mizushima Y, Suzuki K, Nakamura T, Kawai A, Arai K, Ohba T. Development of ultra-thinning technology for logic and memory heterogeneous stack applications. In: 3D system, integration (3DIC); 2011.
[23] Handel H. Technical viability of stacked silicon interconnect technology. Publication; 2010.
[24] Santarini M. Stacked & loaded: Xilinx SSI, 28-Gbps I/O yield amazing FPGAs. Xcell Journal; 2011.
[25] Banijamali B, Ramalingam S, Nagarajan K, Chaware R. Advanced reliability study of TSV interposers and interconnects for the 28 nm technology FPGA. In: Electronic components and technology conference (ECTC), proc; 2011.
[26] Saban K. Xilinx stacked silicon interconnect technology delivers breakthrough FPGA capacity, bandwidth, and power efficiency. White paper; 2011.
[27] Cho S et al. Impact of TSV proximity on 45 nm CMOS devices in wafer level. In: Proc. IEEE Int. Interconnect technology conf. and 2011 materials for advanced metallization (IITC/MAM); 2011. p. 1–3.
[28] http://www.eetimes.com/electronics-products/memory-products/4218905/Samsung-samples-30nm–32GB-DDR3-RDIMMs.
[29] Cho S. Technical challenges in TSV integration to Si. SEMATECH Symposium Korea; 2011.
[30] Industry review. 3D Packaging; May 2012.
[31] Chen B. 3D Ecosystem; March 2011.
[32] Wang MJ, Hung CY, Kao CL, Lee PN, Chen CH, Hung CP, Tong HM. TSV technology for 2.5D IC solution. In: Proceedings of international conference on electronic packaging; 2012. p. 284–8.
[33] Zhan CJ, Chuang CC, Juang JY, Lu ST, Chang TC. Assembly and reliability characterization of 3D chip stacking with 30 μm pitch lead-free solder micro bump interconnection. In: Electronic components and technology conference (ECTC), proc; 2010.
[34] Chang TC et al. Reliability characterization of 20 μm pitch microjoints assembled by a conventional reflow technique. In: Proceedings of international conference on electronic packaging; 2011. p. 221–6.
[35] Huang SY et al. Failure mechanism of 20 μm pitch microjoint within a chip stacking architecture. In: Proceedings of electronic components technology conference (ECTC); 2011. p. 886–92.
[36] Chang TC et al. Reliable microjoints for chip stacking formed by solid–liquid interdiffusion (SLID) bonding. IMPACT, Taipei, Taiwan; Oct. 2011. p. 476–9.
[37] Chang JY, Cheng RS, Kao KS, Chang TC, Chuang TH. Reliable microjoints formed by solid–liquid interdiffusion (SLID) bonding within a chip-stacking architecture. IEEE Trans Comp, Pack Manuf 2012;2(6):979–84.