Design of a CMOS T/R Switch With High Power Capability: Using Asymmetric Transistors

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***Abstract*—A single-pole double-throw transmit/receive (T/R) switch has been realized by using both conventional and asymmetric MOSFETs in a standard 0.18 μm CMOS technology. At 2.4 and 5.8 GHz, the asymmetric-transistor based T/R switch shows 2.7 dBm and 2.3 dBm improvements in measured 1 dB compression points ($P_{1\ \mathrm{dB}}$s) than the conventional circuit of the same circuitry and layout, respectively. This switch also has good insertion losses of 0.62/0.7 and 0.94/1.2 dB for transmit-end/receive-end modes at 2.4 and 5.8 GHz, respectively.**

***Index Terms*—BV_{dss}, insertion loss, isolation, power-handling capability.**

I. Introduction

TRADITIONAL silicon technologies have inherent drawbacks of low breakdown voltage and high substrate loss, resulting in strict challenges for designing high power circuits, such as power amplifiers (PAs) and T/R switches. While CMOS PAs have been successfully implemented in recent researches [1], [2], the demand for high power-handling capability CMOS T/R switches also becomes more imperative.

The critical design considerations of T/R switches include high isolation, low insertion loss and high power-handling capability. Unfortunately, these performances generally are trade-offs with each other. In the commonly used series/shunt topology, the shunt branch typically is used for increasing the off-state isolation, but the insertion loss and the power-handling capability of a series/shunt T/R switch also degrade due to the increased RC losses, the junction diode current and the low breakdown voltage of the shunt transistor. While the parasitic RC and diode effects can be significantly suppressed by using the body-floating technique [3] or the body-switch [4], the signal linearity is still limited by the off-state drain-source breakdown voltage (BV_{dss}) of the shunt transistor, especially for the transmitting path from TX to antenna (ANT). Although the CMOS T/R switch incorporating the LC-resonator can substantially improve the power-handling capability [5], this technique also consumes large chip area. For the inductor-less designs, the solution for low breakdown voltage of the shunt transistor is either using multi-stacked topology [4], [6] or increasing the transistor gate-length. Generally speaking, these methods are based on increasing the device area in exchange for higher voltage endurance, while the research that focuses on enhancing the transistor performances itself is still rare. Recently, a SPDT T/R switch was implemented in 0.25 μm LDMOS technology with a high breakdown voltage of 25 V [7]. One advantage of this design is that the LDMOS T/R switch can be implemented with conventional CMOS circuit blocks on the same silicon wafer. However, the fabrication cost of such hybrid process is still higher than using single CMOS technology of the same gate-pitch. Besides, the applicable level of the LDMOS T/R switch is relatively limited due to a high operation voltage of 15 V.

The asymmetric MOSFET that removes the drain-extension has a similar f_t and a significantly higher BV_{dss} than conventional MOSFETs [8]. More importantly, the fabrication of the asymmetric transistor can be achieved in a standard CMOS technology without any process modification. In this letter, a SPDT T/R switch using both conventional and asymmetric MOSFETs is implemented in a foundry 0.18-μm CMOS technology. Compare with the identical circuitry that only uses conventional devices, the $P_{1\ \mathrm{dB}}$ improvements of 2.7 dBm and 2.3 dBm are measured at 2.4 and 5.8 GHz, respectively, indicating that the performance of the existing circuit topologies can be further promoted by proper incorporating the asymmetric devices into a T/R switch design.

II. Transistor Characteristics and Circuit Design

Fig. 1 shows the cross-section of the conventional and the asymmetric NMOSFETs in a triple-well CMOS process. The only difference between these two devices is that the drain-extension is removed in the asymmetric MOSFET. Fig. 2(a) compares the BV_{dss}s of the conventional and the asymmetric transistors, where an off-state current density of 10^{-7} A/μm is used for the drain-source breakdown criterion. The measured BV_{dss}s of the conventional and the asymmetric transistors are 4 V and 6.9 V, respectively. The increased breakdown voltage of the asymmetric device is attributed to lacking of the drain-extension, resulting in wider surface-depletion region and decreased electric field at the drain-side. In the fabrication process, the mask for PMOSFETs can be used as the drain-side blocking mask of the asymmetric devices; therefore the additional mask or the customized process flow is unnecessary. Fig. 2(b) shows the I_D-V_D characteristics of the conventional and the asymmetric NMOSFETs. This figure reveals two properties of the asymmetric transistors which are critical to the following T/R switch design: First, the asymmetric MOSFET has the higher on-resistance (R_{on}) at the triode region than the conventional

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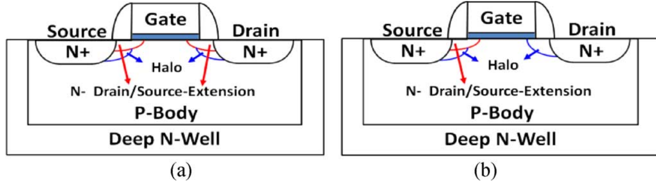
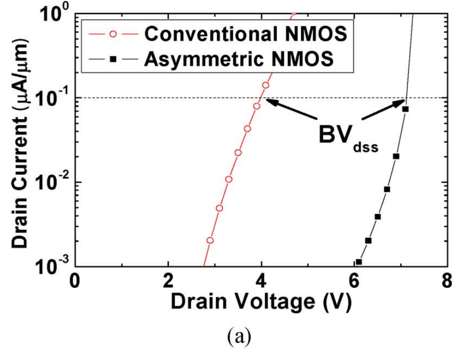


Fig. 1. Cross section of (a) the conventional and (b) the asymmetric NMOSFETs in a triple-well CMOS process.



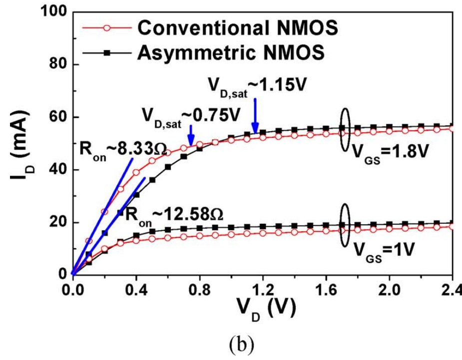


Fig. 2. (a) BV_{dss}s of the conventional and the asymmetric transistors. (b) The I_D-V_D characteristics of the conventional and the asymmetric transistors.

MOSFET. Second, the asymmetric transistor exhibits the higher saturation voltage ($V_{D,sat}$) than conventional device. The first property implies that the asymmetric MOSFET is unsuitable to be used for the switching device on the main signal path due to the higher resistive loss. In the shunt arm design, however, the high BV_{dss} and the smaller gate-to-drain overlapping capacitance ($C_{gd,ov}$) of the asymmetric transistor are beneficial to insertion loss and power-handling capability, in particular to the high-power signal path from TX to ANT. While the T/R switch operates at the TX-mode, the shunt transistor at RX may temporarily be forced into the high-impedance saturation region due to the strong signal coupling from TX, therefore losing the function of improving the port-to-port isolation. Hence, the higher $V_{D,sat}$ indicates that the asymmetric MOSFET is suitable for the shunt transistor at RX, since a transistor has high $V_{D,sat}$ is difficult to enter the saturation region.

Based on the above observations, we designed a SPDT T/R switch which used the hybrid of the conventional and the asymmetric transistors to demonstrate the improvement of power-handling capability. This circuit was implemented in a triple-well 0.18-μm 1P6M CMOS technology. The circuit schematic is shown in Fig. 3(a), where transistors M_1 and M_2 are the main switching devices on the signal paths from ANT to RX and from TX to ANT, respectively. The shunt transistors, $M_3 \sim M_7$, are used to improve the isolation while the corresponding signal

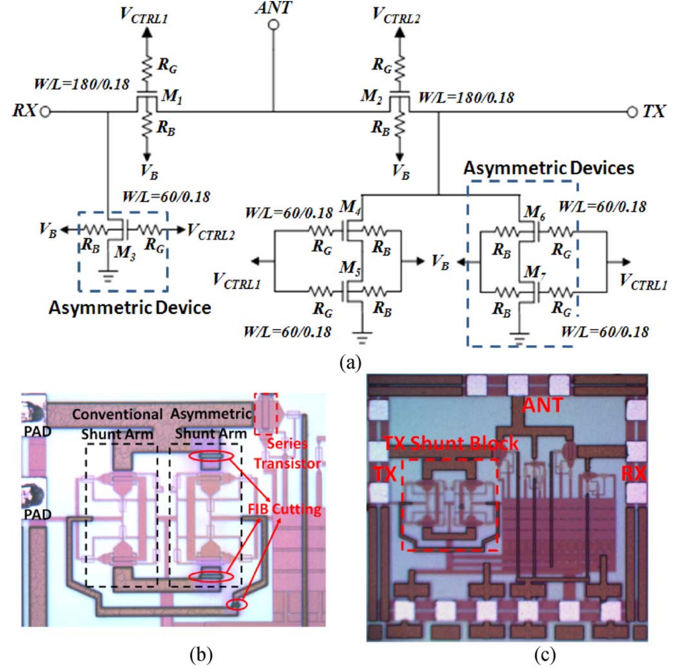


Fig. 3. Designed SPDT T/R switch: (a) The circuit schematic, (b) the local image of the shunt branch at TX and (c) the chip photograph.

path is switched off. The control voltages (V_{ctrl1}, V_{ctrl2}) of this design are 1.8/0 V while the corresponding signal path turns on/off, respectively. The body bias (V_B) is 0 V while the shunt transistors turns off and is 0.2 V while the shunt transistors turn on. R_G and R_B are 10 kΩ resistors used to suppress the capacitive loss and to eliminate the parasitic diode current interior transistors [5]. The shunt arm at RX is a single asymmetric device (M_3), while the shunt branch at TX adopts two stacked transistors to increase the breakdown voltage. This is because the transmitting path from TX to ANT typically is for large signal. To fairly compare the power-handling capability of using the conventional and the asymmetric shunt devices, in this circuit, the shunt arm at TX is designed as the two identical sub-branches. One is composed of the conventional devices (M_4 and M_5), the other is using the asymmetric devices (M_6 and M_7). Fig. 3(b) shows the layout image of the shunt branch at TX, where the two parallel sub-branches are fully symmetric; therefore, the variations caused by layout difference between the two conditions can be minimized in this design. While measuring the circuit performance of one sub-branch, the other sub-branch is cut by focused ion beam (FIB), and vice versa. Fig. 3(c) shows the micro-photograph of the proposed SPDT T/R switch. The whole chip size is $0.67 \times 0.64\ \mathrm{mm}^2$ including the pad frames and the dummy patterns for satisfying density rules. The actual circuit area is only about $0.25 \times 0.5\ \mathrm{mm}^2$.

III. Measurement Results

Fig. 4 shows the measured isolations of the designed T/R switch. While operating at 2.4 GHz, the RX-mode isolation is 33 dB, and the TX-mode isolations of both conditions are better than 35 dB. At 5.8 GHz operation frequency, the RX-mode isolation is 23.7 dB, and the TX-mode isolations are better than 25 dB. The RX-mode return losses are -27.1 dB and -23.7 dB at 2.4 and 5.8 GHz, respectively. The TX-mode return loss of using the asymmetric and conventional shunt

TABLE I
PERFORMANCE COMPARISON OF THE REPORTED CMOS T/R SWITCHES

Refs.	Tech.			Freq. (GHz)	Isolation (dB)	Insertion Loss (dB)	P_{1dB} (dBm)
[3]	0.18 μm CMOS			2.4/5.8	35/27	0.7/1.1	21.3/20
[4]	0.18 μm CMOS			1.9	>20(TX)/>30(RX)	1.5(TX)/1.8(RX)	31.5
[5]	0.18 μm CMOS *			5.2	37.5(TX)/18.24(RX)	1.62(TX)/1.45(RX)	>30(TX)/11(RX)
[6]	0.13 μm CMOS			2.4	>24	0.8(TX)/1.2(RX)	28(TX)
[7]	0.25 μm LDMOS			0.9	25	0.82	18
This Work	**0.18 μm**	**Asymmetric Shunt Arm**		**2.4/5.8**	**>35(TX)/33(RX) (2.4 GHz)**	**0.62(TX)/0.7(RX) (2.4 GHz) 0.94(TX)/1.2(RX) (5.8 GHz)**	**29.2(TX)/23.2(RX) (2.4 GHz) 25.6(TX)/21.1(RX) (5.8 GHz)**
		Conventional Shunt Arm			**>25(TX)/23.7(RX) (5.8 GHz)**	**0.68(TX)/0.7(RX) (2.4 GHz) 1.11(TX)/1.2(RX) (5.8 GHz)**	**26.5(TX)/23.2(RX) (2.4 GHz) 23.3(TX)/21.1(RX) (5.8 GHz)**

* Using LC-resonator

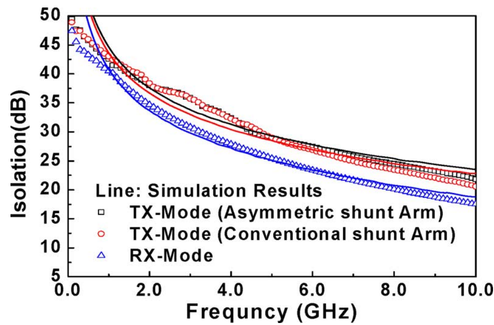


Fig. 4. Measured isolation of the designed T/R switch.

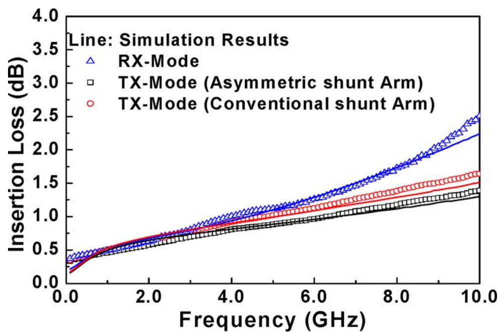


Fig. 5. Measured insertion loss of the designed T/R switch.

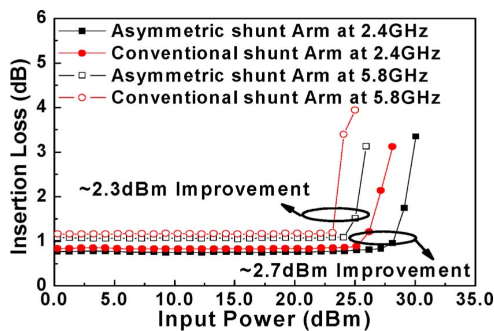


Fig. 6. Measured TX-mode power-handling capabiltiy.

arms at 2.4 GHz are at -30.2 dB and -29.3 dB, respectively, while the TX-mode return losses at 5.8 GHz of these two shunt branches are -27.1 dB and -26.3 dB, respectively.

Fig. 5 shows the measured insertion losses of the proposed T/R switch. The RX-mode exhibits insertion losses of 0.7 dB and 1.2 dB at 2.4 and 5.8 GHz, respectively. The TX-mode insertion losses of using the conventional shunt arm are 0.68 dB and 1.11 dB at 2.4 and 5.8 GHz, and the TX-mode insertion losses of using the asymmetric shunt arm are 0.62 and 0.94 dB at 2.4 and 5.8 GHz, respectively. The insertion loss difference between the two conditions gradually increases with increasing frequency, which can be attributed to the smaller $C_{gd,ov}$ of the asymmetric device, which reveals the advantage of the asymmetric device in high-frequency designs. Fig. 6 exhibits the measured TX-mode power-handling capability, where the asymmetric shunt branch provides 2.7 dBm and 2.3 dBm improvements than using the conventional shunt transistors at 2.4 and 5.8 GHz, respectively. Table I summarizes the reported CMOS T/R switches at the similar frequency bands. The proposed hybrid T/R switch achieves good balance between insertion loss and power-handling capability, based on a simple inductor-less SPDT architecture with a small size. These performances can mainly be attributed to the high BV_{dss} and the small $C_{gd,ov}$ of the asymmetric shunt transistors.

IV. CONCLUSION

A SPDT T/R switch incorporating the conventional series switching devices and the asymmetric shunt transistors have been designed and implemented. The measurement results show 2.7 dBm and 2.3 dBm improvements in TX-mode $P_{1\text{ dB}}$ at 2.4 and 5.8 GHz, respectively, while low TX-mode insertion losses of 0.62 and 0.94 dB are obtained at 2.4 and 5.8 GHz, respectively. These performances indicate that the asymmetric transistor is a potential solution for high-power circuit designs in a low cost CMOS technology.

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