Ultra-low voltage implicit multiplexed differential flip-flop with enhanced noise immunity

W.-H. Sung, M.-C. Lee, C.-C. Chung and C.-Y. Lee

An ultra-low voltage 22T implicit multiplexed differential (IMD) flip-flop (FF) is proposed. An implicit multiplexer is designed to simplify the differential FF complexity, while its control data path is able to enhance the FF noise immunity as well. So, the fully static IMD-FF with modified differential topology provides a sufficient noise margin under voltage scaling. On the other hand, the IMD-FF operation avoids considerable DC current dissipation to save active power and suppresses the idle leakage by stacked transistors. The post-layout simulation in 90 nm CMOS process with 400 mV supply voltage shows that the IMD-FF achieves 56% active power and 42.2% leakage power reduction. The tolerable noise energy is enhanced by 18.9% on average. Finally, this work provides 93% function yield rate under the effect of process-voltage-temperature variations and 40 pJ input noise energy.

Introduction: The flip-flop (FF) is the most critical circuit in low energy VLSI systems. This is because FFs not only consume a large portion of system power and leakage, but also remain as the bottleneck in voltage scaling due to higher complexity than other logics. As supply voltage drops to near the sub-threshold region, the ratio between the conductance current I_{ON} and cutoff current I_{OFF} is degraded in an exponential order. I_{ON} is more difficult to charge and discharge internal nodes against I_{OFF} towards the correct state. Such degradation is even worse when considering the effect of process-voltage-temperature (PVT) variations, resulting in a poor static noise margin (SNM) [1]. That is, FFs become quite sensitive to input noise induced from coupling crosstalk or supply ripple [2].

To enhance the SNM for low voltage operation, FFs must maintain sufficient driving I_{ON} and noise immunity at the same time. The former can be achieved by removing dynamic logics or current contention nodes, e.g. 2-INV positive feedback latch, from FF designs, while the latter normally depends on circuit topologies. The master-slave (MS) based FF is a well-known power and area efficient topology. Especially, the clocked CMOS (C^2MOS) FF [3] and transmission-gate (TG) FF [4] are PVT insensitive owing to their static and complementary design without a current contention node. However, MS-based FFs suffer weak immunity to noise appearing on the clock input since any induced noise pulse with merely short duration, i.e. a transmission-gate delay, might easily turn on the master/slave latch incorrectly. In contrast, the static differential FF [5] requires higher noise energy to drive the storage latch and related control signals, implying better noise immunity. Unfortunately, this structure occupies considerable transistor counts and consumes more power. Note that, except [5], most of differential FFs are unable to operate at low voltage because the commonly adopted NMOS shorting device (providing a ground path to avoid floating) fails to generate correct control signals with degraded current. Accordingly, an ultra-low voltage 22T implicit multiplexed differential (IMD) FF is proposed for low energy operation. An implicit multiplexer (I-MUX) is designed to simplify the differential FF complexity, while its control data path is able to enhance noise immunity. The fully static IMD-FF with modified topology provides sufficient SNM under voltage scaling. In addition, the IMD-FF operation avoids DC current dissipation to save active power, and its leakage current is reduced by stacked transistors.

Proposed design: Differential FFs contain the precharge unit and SR-latch. The precharge unit is applied to precharge and evaluate control signals S/SB (set) and R/RB (reset). The SR-latch determines output Q/QB according to S/SB and R/RB. For SB = '0' and RB = '1', Q will be set to high. For SB = '1' and RB = '0', Q will be reset to low. If SB and RB are both high, output Q will remain the same logic. To solve the high complexity issue in [5] for power and area reduction, the proposed IMD-FF utilises an implicit multiplexer (I-MUX) to complete SR logics. Fig. 1*a* shows the I-MUX design concept. From a truth table, the SR-latch function is realised by an equivalent 4-to-1 MUX simply. Then, the 4-to-1 MUX can be further translated to I-MUX, including an internal data latch constructed by INV1 and INV2. The differential N-MOS pass gates MN5 and MN6 are in charge of dual discharge path selection. For SB = '0' and RB = '1', MN6 is turned on to discharge QB; for SB = '1' and RB = '0', MN5 is turned on to discharge QQ and Q. When SB = '1' and RB = '1', MN5 and MN6 are turned off for latch storage. Based on the operation of the I-MUX, the proposed IMD-FF circuit diagram is shown in Fig. 1*b*. When CLK is low, SB/RB are precharged to high, and then S/R are discharged to low. I-MUX (MN5 and MN6) is turned off to hold the data (QQ and QB) stored in MP1, MN1, MP2 and MN2, where SB/RB and S/R act as virtual VDD and virtual GND, respectively. When CLK is triggered to high, D (DB) will discharge SB (RB) to low through MN8 (MN7), and S (R) is charged to high (low). Then, the I-MUX performs data path selection as indicated in Fig. 1*a*. That is, when D = '1' (DB = '1'), MN6 (MN5) is turned on to discharge QB (QQ), while QQ (QB) is charged by MP1 and MP3 (MP2 and MP4).

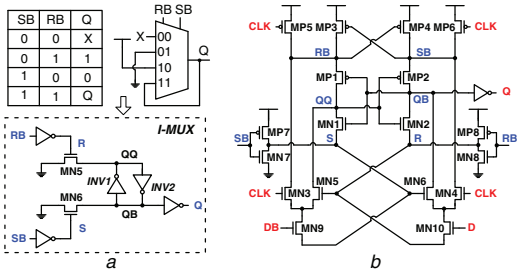

Fig. 1 *Proposed IMD-FF design*

a I-MUX design concept
b IMD-FF circuit diagram

Conventional differential FFs require an extra retention latch holding the '0' logic of SB/RB in the evaluation phase to avoid floating until the next precharge of SB/RB, resulting in increased transistor counts. Instead, IMD-FF connects SB (RB) with data latch output QB (QQ) through MN4 and MN6 (MN3 and MN5) since QB (QQ) exists as a discharge path to MN7 (MN8) as CLK = '1'. Fig. 2 shows the implementation of the SR-latch applied in a differential FF [5] and an IMD-FF, excluding the precharge unit for simplicity. The IMD-FF occupies 14T to implement the SR-latch, while [5] contains 14T and 8T in the data latch and the retention latch. Considering the precharge unit, the IMD-FF totally saves 14T. Besides, the operation of the IMD-FF prevents current contention to eliminate DC current dissipation because all charge and discharge paths of the SR-latch output QQ (QB) are controlled by MP3 and MN7 (MP4 and MN8) according to SB (RB). The I-MUX will not discharge QQ (QB) until SB (RB) turns off MP3 (MP4). On the other hand, as the I-MUX begins to discharge QQ (QB), QB (QQ) is being charged concurrently and its discharge path MN8 (MN7) has already been turned off by RB (SB). Moreover, most of the IMD-FF internal nodes are designed as a stacked structure to minimise V_{DS} for leakage suppression. For instance, RB, QQ, and S (SB, QB, and R) are inserted between cascode transistors MP1, MN1, MN3, MN5, and MN9 (MP2, MN2, MN4, MN6, and MN10) since these nodes have the same logic value in the evaluation phase.

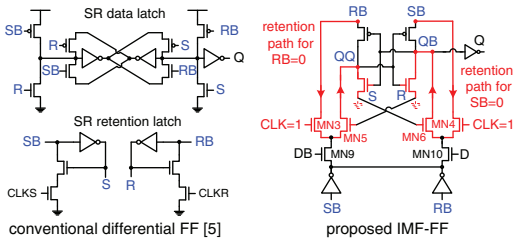

Fig. 2 *SR-latch implementation in [5] and IMD-FF*

In the precharge phase, differential FFs provide better noise immunity than MS-based FFs since the noise pulse must retain sufficiently long duration to turn on the SR logics and lead the SR-latch to error state. However, differential FFs remain unstable in the evaluation phase since the noise pulse might easily enable the single gate delay precharge unit to erase the SR signals. Alternatively, to force IMD-FF function failure, the noise is required to turn on the precharge unit, SB/RB inverter and the I-MUX successively, indicating the robustness of the IMD-FF for all conditions. Moreover, after noise pulse duration, the

I-MUX retention path is able to recover the SB/RB signal correctly to avoid an unknown state of SB/RB.

Experimental results: The IMD-FF and related designs are implemented in 90 nm CMOS process, where the FF sizing is determined by choosing minimal energy for a fixed D-to-Q delay. The post-layout simulation in Fig. 3 shows the FF reliability analysis with 400 mV supply voltage and ±10% variation. Fig. 3*a* is the noise immunity curve [2] which indicates the maximum tolerable noise without function failure in terms of noise amplitude V_N and pulse width T_N. When D-to-Q delay equals 0.7 ns, the IMD-FF improves 40.6% tolerable T_N for $V_N = 0.2$ V. Fig. 3*b* shows the FF function yield rate under PVT and noise effects. Each point indicates the correctness probability from 20000 times of Monte-Carlo simulation with varied process, temperature (0–100°C) and V_T mismatch. The X-axis represents input noise energy. The IMD-FF achieves 93% yield rate for 40 pJ input noise energy, but related designs decrease to below 80%. Table 1 lists the performance comparisons. Compared to [5], this work achieves 56% active power and 42.2% leakage power reduction. Besides, the index average noise threshold energy (ANTE) [2] is enhanced by 18.9%, where the ANTE represents the average tolerable noise energy of each curve in Fig. 3*a*, i.e. E($V_N^2 \times T_N$), to benchmark noise immunity.

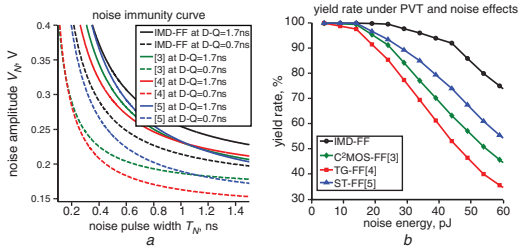

Fig. 3 *Reliability analysis under PVT and noise effects*

a Noise immunity curve
b FF function yield rate

Table 1: Performance comparisons

	Proposed	[5]	[3]	[4]
Transistor counts	22T	36T	26T	24T
Topology	Diff.	Diff.	MS	MS
Setup time (ns)	−0.08	−0.4	0.26	0.27
Hold time (ns)	0.14	0.5	−0.18	−0.14
Active power* (nW)	24.4	55.4	32.3	28.7
Leakage (nW)	15.2	26.3	18.2	18.6
ANTE (pJ)	74.5	60.4	48.7	44.3

*Switching activity = 50%, voltage = 400 mV, D-Q delay = 1.7 ns, output load = $16C_{min}$

Conclusion: A 22T IMD-FF is presented for low voltage operation. By applying I-MUX, the IMD-FF can be realised in minimal transistor counts. Hence, the fully static IMD-FF with modified differential topology provides reliable tolerance against PVT and noise effects for voltage scaling. Besides, this work also reduces considerable active power and idle leakage, giving an adequate solution for low energy applications.

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