A Low Glitch 10-bit 75-MHz CMOS Video D/A Converter

Tien-Yu Wu, Ching-Tsing Jih, Jueh-Chi Chen, and Chung-Yu Wu

Abstract—A low glitch 10-bit 75-MHz CMOS current-output video digital-to-analog converter (DAC) for high-definition television (HDTV) applications is described. In order to achieve monotonicity and low glitch, a special segmented antisymmetric switching sequence and an innovative asymmetrical switching buffer have been used. The video DAC has been fabricated by using 0.8 μm single-poly double-metal CMOS technology. Experimental results indicated that the conversion rate is above 75 MHz, and nearly 50% of samples have differential and integral linearity errors less than 0.24 LSB and 0.6 LSB, respectively. The glitch has been reduced to be less than 3.9 pV·s and the settling time within $\pm$ 0.1% of the final value is less than 13 ns. The video DAC is operated by a single 5 V power supply and dissipates 170 mW at 75 MHz conversion rate (140 mW in the DAC portion). The chip size of video DAC is 1.75 mm $\times$ 1.2 mm (1.75 mm $\times$ 0.7 mm for the DAC portion).

I. INTRODUCTION

HIGH-SPEED and high-resolution CMOS video DAC's are required to enhance the performance of many video systems. For example, video DAC's which are faster than 70 MHz and have more than 10-bit resolution are needed in HDTV applications. In these applications, the CMOS video DAC has the advantages of low power, low cost, and I/O compatibility with both TTL and external CMOS circuitry. Furthermore, it can be integrated with memory and digital signal processing IC's for various video applications [1]. However, glitches or output spikes in these CMOS video DAC's should be as small as possible, especially in high-resolution video applications. Glitches in DAC's generally occur at major **carries** over certain points (1/4, 1/2, 3/4, and 1 of full-scale) and appear as intensity variation on a television screen. A parameter called the glitch area is a measure of the product of the amplitude and the duration of the spike.

Among several CMOS DAC's proposed so far [2]–[4], some have a low conversion rate [2], [3] while another has a large glitch area [4]. This paper describes a 10-bit 75 MHz CMOS video DAC with only 3.9 pV·s glitch area. It was fabricated in 0.8 μm single-ploy double-metal standard digital CMOS process. This video DAC is based on the current cell matrix design [5] and can drive a load resistor without an output buffer. The key innovation here is a special "segmented antisymmetric switching" sequence, which
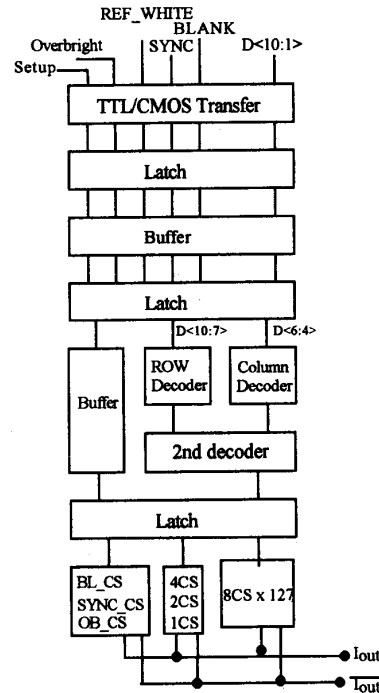
Fig. 1. Video DAC block diagram.

suppresses graded errors, symmetrical errors, and random errors distributed throughout the output of the current cells. Furthermore, a new deglitching circuit is proposed in the current cell configuration. As a result, the conversion rate of the converter is higher than 75 MHz and the glitch area is only 3.9 pV · s.

II. BASIC CONFIGURATION

Fig. 1 shows the architecture of the video DAC. This is a 10-bit multifunction video DAC designed specifically for color graphics and conventional D/A conversion applications. Available control inputs include sync, blank, reference white, and 10% overbright. An additional feature is a setup pin to specify one of the three available setups in the analog output. The video DAC can generate RS-343A and RS-170 compatible video signals output on a resistor load without external buffering.

Fig. 2 shows the basic configuration of the D/A converter. It consists of 127 eight-LSB (8CS) current sources for the upper 7 MSB's and 3 binary weighted current sources (1CS,
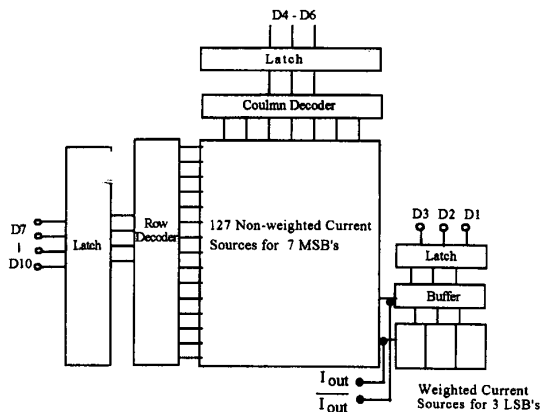
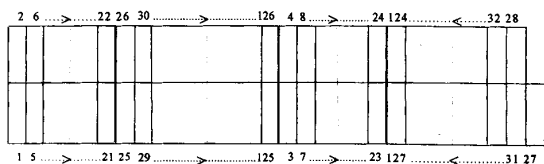Fig. 2. Basic configuration of the current matrix D/A converter.

Fig. 3. Segmented antisymmetric switching sequence.

2CS, 4CS) for the remaining 3 LSB's. The outputs of current sources are summed directly to a resistor load. Since the unit current generated by the largest cell is 8 LSBs, a mismatch of ± 6.125% in unit currents is allowable to keep the differential linearity error within ± 0.5 LSB. On the other hand, the integral linearity error is sensitive to the gradient of transconductance across the matrix due to the variations of threshold voltage and process lithography.

III. SEGMENTED ANTISYMMETRIC SWITCHING

Fig. 3 shows a 2-D current source matrix and a segmented antisymmetric switching sequence. One–hundred twenty–seven nonweighted eight-LSB current sources are placed in two rows. These current sources are nonuniform for various reasons, such as layout mismatch, thermal distribution, and process deviation. First, the voltage drop on a long power line can cause a graded error [5]. Second, the thermal distribution inside the chip can generate a symmetrical error [4]. Moreover, the threshold voltage of an enhancement-mode MOSFET is highly process dependent. The equation of the threshold voltage V_{TE} can be written as

$$V_{TE} = V_{FB} - \frac{Q_{SS}}{C_{ox}} + V_s + 2|\Phi_P| + \frac{|Q_d|}{C_{ox}} \qquad (1)$$

where V_{FB} is the flat-band voltage, Q_{SS} is the surface charge per unit area, C_{ox} is the gate oxide capacitance per unit area, V_s is the substrate bias, $2|\Phi_P|$ is the voltage required for strong inversion, and Q_d is the depletion charge per unit area in
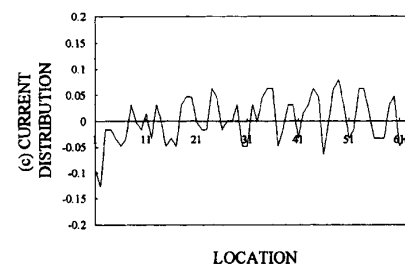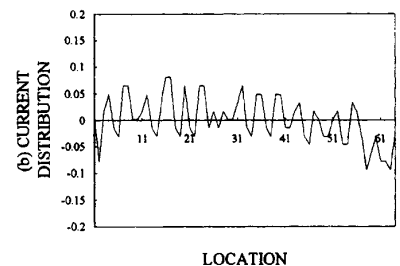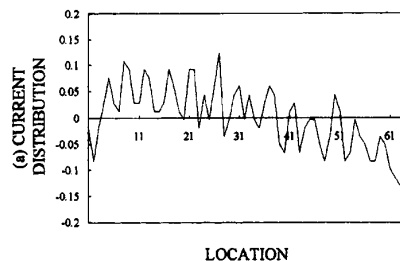

Fig. 4. Current distribution of experimental result. (a) Random asymmetrical and right side down. (b) Random symmetrical. (c) Random asymmetrical and left side down.

the depletion region. All of the terms except V_s are process dependent. Hence, there exists random error due to process variations. However, the random error is anisotropic from chip to chip and wafer to wafer. Therefore, the final error distribution in the current source matrix can not be simply given by linearly superposing these error components. The worst graded error can be easily reduced to only 0.04 LSB by widening the power line. Because the voltage drop $(\Delta V_{\max})$ along the power line from the origin point to the last eight-LSB current source is about 3 mV $(\Delta V_{\max} \approx \sum_{x=0}^{63} 294\mu A \times [64 - X] \times 0.0048\ \Omega)$. The symmetrical error is not significant, either, because power dissipation is only 140 mW. After taking several measurements from different chips, wafers, and process technologies (1.2 μm double-metal single-poly CMOS technology and 0.8 μm double-metal single-poly CMOS technology), the final error distribution of the current cell matrix can be grouped into three categories, as shown in Fig. 4.
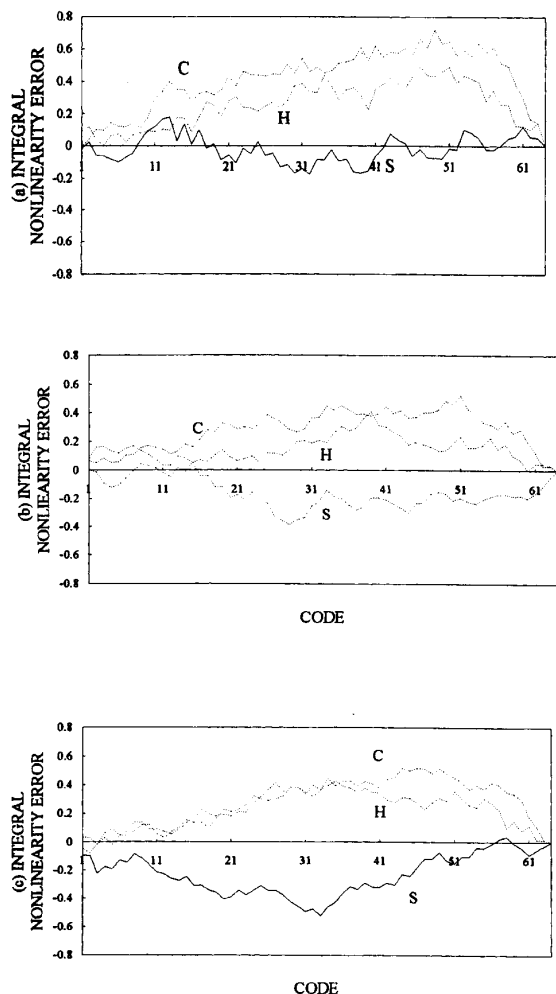
Fig. 5. Integral linearity error of conventional symmetrical switching (curve C), hierarchial symmetrical switching (curve H), and segmented antisymmetrical switching (curve S). (a) Random asymmetrical and right side down. (b) Random symmetrical. (c) Random asymmetrical and left side down.

Fig. 6. Current source with asymmetrical switching buffer.

The conventional symmetrical switching sequence can compensate for graded errors of current source [5]. On the other hand, hierarchical symmetrical switching [4] has the advantage of compensating the linear superposition of graded error and symmetrical error. But when current distribution is dominated by random error as shown in Fig. 4, another switching sequence should be developed to alleviate the increase of integral nonlinearity error. From the current distribution shown in Fig. 4, we can separate 127 eight-LSB current sources into four segmentations and each has positive or negative average, respectively. After the MATLAB program and computer simulation, it can be proved that "segmented antisymmetric switching" sequence is the best solution to reduce random error.

According to our experiment and simulation, a "segmented antisymmetric switching" sequence has been developed. Fig. 3
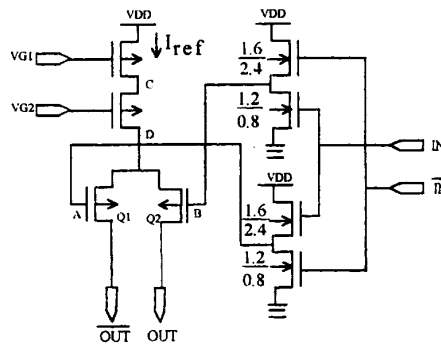
shows the segmented antisymmetric switching, which is the optimum switching to suppress the superposition of graded error, symmetrical error, and especially random error. Fig. 5(a) shows that the segmented antisymmetric switching significantly improves the integral nonlinearity (INL) error due to random asymmetrical and right side down current distribution. It also has a better INL than conventional symmetrical switching, as well as hierarchical symmetrical switching for random symmetrical current distribution, as shown in Fig. 5(b). Although it is not superior to the hierarchical symmetrical switching, it is still better than the conventional symmetrical switching for random asymmetrical and left side down current distribution, as shown in Fig. 5(c). Measurement results have shown that the segmented antisymmetric sequence can get significant improvement on the DAC's differential nonlinearity (DNL) error and integral nonlinearity (INL) error. Its INL values are from 0.4 LSB to 0.9 LSB, whereas the DNL values are from 0.24 LSB to 0.45 LSB.

IV. CURRENT CELL CONFIGURATION

A key aspect of the performance of a video DAC is its glitch or output spike. The maximum value usually occurs at the half-scale transition, where the MSB is turned on (or off) and all the other bits are turned off (or on). The glitch is mainly due to the following effects:

1) imperfect synchronization of inputs
2) channel length modulation of current sources due to voltage fluctuation at ground line and output resistor load
3) charge and discharge of parasitic capacitances associated with current sources
4) feedthrough of digital input data to the output of current source and
5) the time that the switching transistors are simultaneously in the off state.

Fig. 6 shows the high-speed, low-glitch current cell. A sequential decoder with one stage latch [5] for current cells has been used to prohibit simultaneously connecting one current source while disconnecting the other, which minimizes output spike. A cascade current source is used to minimize voltage fluctuation at the node C. This configuration provides high output resistance with short channel length, which in turn
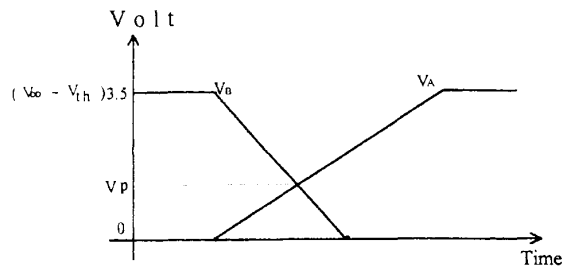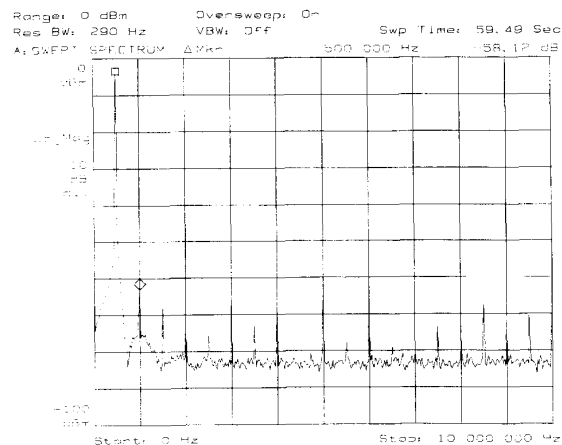
Fig. 7. Buffer output waveform.

Fig. 8. Output spectrum of 500 kHz input signal at 75 MHz conversion rate.

Fig. 9. Glitch occurs at the major code transitions (rising edge).

reduces the stray capacitance at the common source node D. This helps to reduce the recovery time of voltage at this node during the switching transition.

A key aspect of the current source is the asymmetrical switching buffer. The principle of asymmetrical switch control in differential switches is to avoid simultaneously turning off the differential switching transistors ($Q1$ and $Q2$ in Fig. 6) completely, but allow simultaneous turn-on for a short period of time. If both switching transistors are turned off, the output node of the current source will rapidly discharge and the current source will turn off. To recover from this condition, the current source must progress through the linear region and back into saturation. Hence, turning off the current source not only slows down speed but increases output spike (glitch). On the other hand, simultaneously turning on the switching transistors only degrades the speed a little. It helps to make I_{ref} constant during the switching transition and reduces glitch substantially. Hence, the voltage output of the asymmetrical buffer has shorter fall time (T_f) and longer rise time (T_r) as shown in Fig. 7. The voltage swings are limited to 0 and V_{DD}-V_{th} (about 3.5 V), and consequently, the feedthrough of digital input data to the output of current source is reduced. The crossing point voltage (V_p) is set at
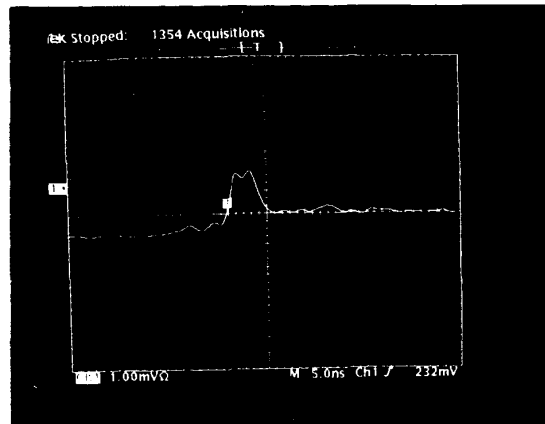
the optimum low level to ensure both $Q1$ and $Q2$ do not turn off simultaneously even if skew happens. Thus the voltage fluctuation at the node D can be minimized at the same time. There will be trade-offs in the decision of rise time, fall time, settling time, and glitch. The final optimum decision will depend on iterative computer simulations. Parameter deviations (ΔV_{th}, $\Delta L \cdots$) as well as temperature and supply voltage voltage variations should be considered in computer simulation to get the final optimum decision of fall time (T_f) and rise time (T_r). The experimental results have shown that a 10-bit video DAC with this kind of current cell can reduce the glitch energy to less than 3.9 pV · s and retain the settling time (to ± 0.1%) to less than 13 ns at the same time.

V. EXPERIMENTAL RESULTS

Figs. 8 and 9 show the performance of the fabricated DAC measured with a 50 Ω and 30 pF load. Fig. 8 shows the output spectrum of the D/A converter with 500 kHz digital sinusoidal input clocked at frequency of 75 MHz and full scale current of 18.8 mA. The overall signal-to-noise ratio, including distortion, is dominated by the second harmonic distortion located at 1 MHz, which is 58.12 dB below the signal level. For a 4 MHz digital sinusoidal input clocked at frequency of 75 MHz, the overall signal-to-noise ratio, including distortion, is still dominated by the second harmonic located at 8 MHz, which is 49 dB below the signal level.

Fig. 9 shows the glitch that occurs when the most significant bit is turned on while other bits are turned off. The glitch is the time integral of the transient waveforms. The maximum glitch is 3.9 pV · s. The power consumption for the whole video DAC is 170 mW, but only 140 mW is for the DAC portion.

VI. CONCLUSION

A low glitch 10-bit 75-MHz video D/A converter based on the current cell matrix has been developed. A special seg-mented antisymmetric switching sequence is introduced. This

switching sequence suppresses the superposition of graded error, symmetrical error, and random error distributed among the outputs of current cells. A current source cell with asymmetrical switching buffer has been used to reduce the glitch and achieve high speed performance at the same time. The video D/A converter has been fabricated by using a 0.8 μm standard CMOS digital technology. The settling time to $\pm$ 0.1% is less than 13 ns and the glitch energy is less than 3.9 pV $\cdot$ s. This video D/A converter can be operated at single power supply of 5 V. It dissipates 170 mW (18.8 mA is in the load, 10 mA is for the video signal, 1 mA is for the bias circuit; another 4 mA is for the digital circuit) at 75 MHz clock rate. P-channel transistors are used for current source so that it can directly drive a load resistor without an output buffer. Only one external current source is needed in VGA graphics card and HDTV applications.

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