A Programmable Implantable Microstimulator SoC With Wireless Telemetry: Application in Closed-Loop Endocardial Stimulation for Cardiac Pacemaker

Shuenn-Yuh Lee, *Member, IEEE*, Mario YuCheng Su, *Student Member, IEEE*, Ming-Chun Liang, You-Yin Chen, Cheng-Han Hsieh, Chung-Min Yang, Hsin-Yi Lai, Jou-Wei Lin, and Qiang Fang, *Member, IEEE*

***Abstract*—A low-power, wireless, and implantable microstimulator system on chip with smart powering management, immediate neural signal acquisition, and wireless rechargeable system is proposed. A system controller with parity checking handles the adjustable stimulus parameters for the stimulated objective. In the current paper, the rat's intra-cardiac electrogram is employed as the stimulated model in the animal study, and it is sensed by a low-voltage and low-power monitoring analog front end. The power management unit, which includes a rectifier, battery charging and detection, and a regulator, is used for the power control of the internal circuits. The stimulation data and required clock are extracted by a phase-locked-loop-based phase shift keying demodulator from an inductive AC signal. The full chip, which consumes 48 μW only, is fabricated in a TSMC 0.35 μm 2P4M standard CMOS process to perform the monitoring and pacing functions with inductively powered communication in the *in vivo* study.**

***Index Terms*—Endocardial stimulation, pacemaker, power management, programmable implantable stimulator, wireless telemetry.**

I. Introduction

THE human body is a complex closed-loop regulation system. In patients with dysfunctional control mechanisms, the general open-loop device is not safe or effective when interacting with the circulatory system. Therefore, the use of closed-loop implantable telemetry devices [1], [2] is popular, as recent clinical studies have shown their efficiency and usefulness in detecting and treating various cardiac arrhythmias. In the present study, a closed-loop implantable microstimulator system on chip (IMSoC), which possesses the sensing of a physiological signal, microstimulation, and wireless data/command transmission, is developed to cure arrhythmia. Power transfer to the implanted devices is required, which employs radio frequency (RF) coupling with no fear of infection caused by the battery replacement. However, providing sufficient and stable energy to power the biomedical implant system inside a freely moving subject is challenging. RF-coupling and loading variations, due to the deviation of stimulated point caused by the moving, may result in the decrease in induced supply voltage/current because of insufficient transmitted power, thereby causing improper device operation or shutdown.

To avoid the influence caused by the RF-coupling and loading variations, the RF signal from the coupling and combined with battery control, can be utilized to charge a rechargeable device [3], thus offering a more stable voltage for proper device operation. An improvement of the powering system, which is used in biomedical implants, can also be adopted to eliminate the demand of periodic surgery for battery replacement and to improve the life quality of the patient.

In the present work, the proposed IMSoC is designed as a cardiac defibrillator for the remote delivery of power through coupled coils, which supply power to a bio-implanted rechargeable battery. The IMSoC consists of a smart control circuit for power management and an RF-coupling power system for battery charging [3]. Moreover, two off-chip ultra-small rechargeable batteries are used as the power supply. The microstimulator circuit embedded in the IMSoC is externally powered and controlled by a single encoded RF carrier. Stimulus parameters, such as pulse width, amplitude, and frequency, can be programmable [4] from the remote controller.

Using an implantable system on chip with a closed-loop function, stimulation can be dynamically adjusted according to the real-time heart rate (HR). To acquire intracardiac electrograms (EGMs) continuously, a monitoring analog front end (MAFE) is implemented to sense and detect the peak value of EGMs and to achieve the close-loop control of HR. To verify a prototype of the IMSoC *in vivo*, the current study presents an example of an implantable RF power converter used to regulate endocardial pacing with the closed-loop physiological feedback from the conscious rodent model. Compared with the previous work [5], the present study adopts a power management system to

Manuscript received May 19, 2011; revised September 02, 2011; accepted November 16, 2011. Date of publication December 12, 2011; date of current version December 29, 2011. This work was supported by the Chip Implementation Center (CIC), the National Science Council, Taiwan, under Grant 100-EC-17-A-01-S1-040, NSC100–2220–E–194–002, NSC100–2220–E–194–003, NSC100-2628-E-194-003, and the Australian Research Council, Australia. This paper was recommended by Associate Editor D. Ham.

S.-Y. Lee, M. Y. Su, M.-C. Liang, C.-H. Hsieh, and C.-M. Yang are with the Electrical Engineering Department, National Chung Cheng University, Min-Hsiung Chia-Yi 62102, Taiwan (e-mail: ieesyl@ccu.edu.tw).

Y.-Y. Chen is with the Biomedical Engineering Department, National Yang Ming University, Taipei 112, Taiwan (e-mail: youyin.chen@ym.edu.tw).

H.-Y. Lai is with the Electrical Engineering Department, National Chiao Tung University, Hsinchu 300, Taiwan.

J.-W. Lin is with the Cardiovascular Center, National Taiwan University Hospital Yun-Lin Branch, Yun-Lin, Taiwan (e-mail: jouweilin@yahoo.com).

Q. Fang is with the Electrical and Computer Engineering Department, Royal Melbourne Institute of Technology, Melbourne, Victoria 3001, Australia (e-mail: john.fang@rmit.edu.au).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TBCAS.2011.2177661

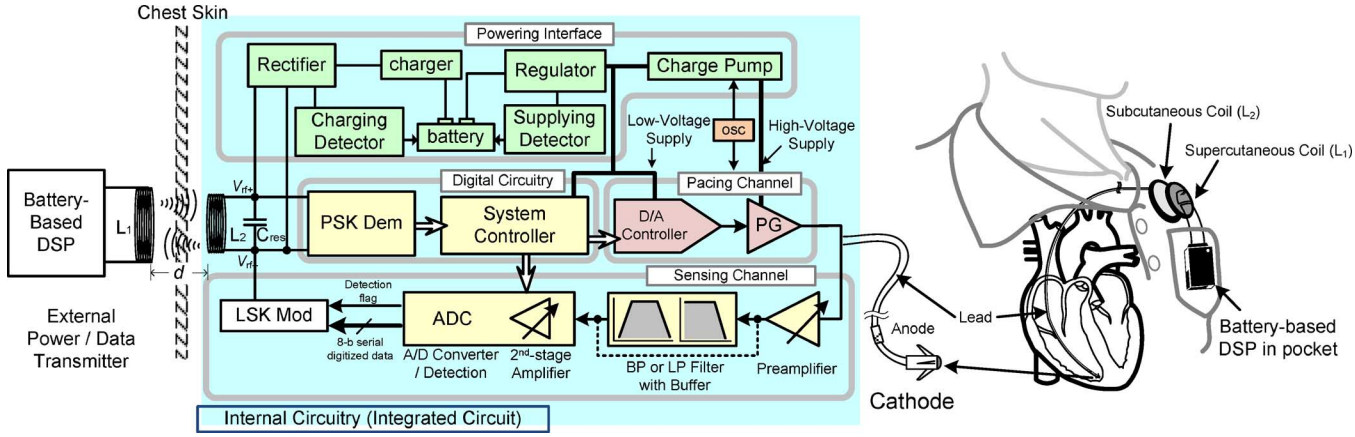


Fig. 1. Block diagram of the proposed close-loop microstimulator system with an external device.

provide a more stable power supply than the pure RF-coupling supply. A phase-locked-loop (PLL)-based phase shift keying (PSK) demodulator and the multi-mode filter of sensing channel are developed as well to increase the reliability of the whole system and to provide the functions of heart-rate detection and heart-signal monitor. Moreover, a prototype of a bidirectional data transmission sharing a set of coil is considered in the proposed system to upgrade the interactivity between the patient and the physician. The *in vivo* experiment is also presented to demonstrate the behavior of the closed-loop system.

Section II presents the microstimulator system architecture. Section III reports the powering interface and pacing channel. In Section IV, the digital circuits, including a PLL-based PSK demodulator and the system controller, in charge of clock-and-data recovery (CDR) and the stimulation functions are explained in detail. Section V discusses the implementation of the sensing channel. The *in vivo* experiment adopting Sprague-Dawley (SD) rats are presented in Section VI to demonstrate the closed-loop system. Section VII briefly concludes the present paper.

II. System Architecture

The block diagram of the close-loop stimulation system with an external device is presented in Fig. 1. The external device, including a battery-based digital signal processor (DSP) in the pocket, transmits encoded data and charging energy to the in-body circuit through a set of coils. The modulated digital data acquired from the sensing channel are transmitted out of the body through the same coils to save on coil area. Four sub-blocks, namely, powering interface, digital circuitry, pacing channel, and sensing channel, are integrated in the proposed IMSoC to carry out the wireless bidirectional communication. The powering interface with charging ability is implemented to reduce the required charge capacity of the battery and further reduce the volume of the battery. The interface can provide low- and high-supply voltages for system operation and microstimulation, respectively. Moreover, it guarantees a nonstop energy source by switching the charging and supplying path of the two-battery-based power supply to avoid improper device operation. The digital circuitry is employed to enhance reliability in communication and to provide the programmable stimulation amplitude, duration, and frequency as required by the nerve stimulation. The PSK demodulator based on the PLL technique is proposed to recover the clock and data from the received 256 kHz carriers.

In the pacing channel, the digital-to-analog converter (DAC) and a 3.2 V pulse generator are combined coordinately. A charge pump circuit with a less capacitor number is adopted to provide 3.2 V for the pulse generator [6]. This proposal enables the stimulation function with programmable arguments on the specification, such as the triggered pulse duration/amplitude and stimulation frequency, to be implemented according to the detection result of the MAFE.

A sensing channel with a MAFE is adopted to detect the stimulated signal from the paced neuron. Potentials of the stimulated objective (such as sinoatrial node (SA node) or atrioventricular node (AV node)) are detected and amplified by the preamplifier with a differential difference structure to achieve a programmable gain under a low-supply voltage. Following the signal processing stage, which is composed of a biquad low-pass (LP)/band-pass (BP) filter and an analog-to-digital converter (ADC) with real-time threshold detection, the cardiac waveform of the stimulated objective and its peak value can be obtained. The circuits and operations of sub-blocks will be presented in Sections III–V in detail. The function of the whole chip will be verified by *in vivo* experiment in Section VI.

III. Powering Interface and Pacing Channel

A. External Power/Data Transmitter

The external power/data transmitter, as shown in Fig. 2, consists of a power MOS switch used to control the signal on the coil, an RF choke ($\mathrm{L_{choke}}$) that provides a more stable DC current for the transistor $\mathrm{M_0}$, capacitances C_s and C_p that produce different resonance frequencies [7], and a primary coil for the coupling that can be modeled as the equivalent series of resistance R_s and inductance $\mathrm{L_1}$.

The class-E amplifier [7] combined with the PSK modulator is implemented in the transmitter to minimize the energy in the switch states of the phase of the transmission coil current. The controlled signal ($\mathrm{V_g}$) at the output of XOR gate along with the input of the data and clock can control the transistor $\mathrm{M_0}$ to generate a PSK signal at the drain of the transistor. The detailed

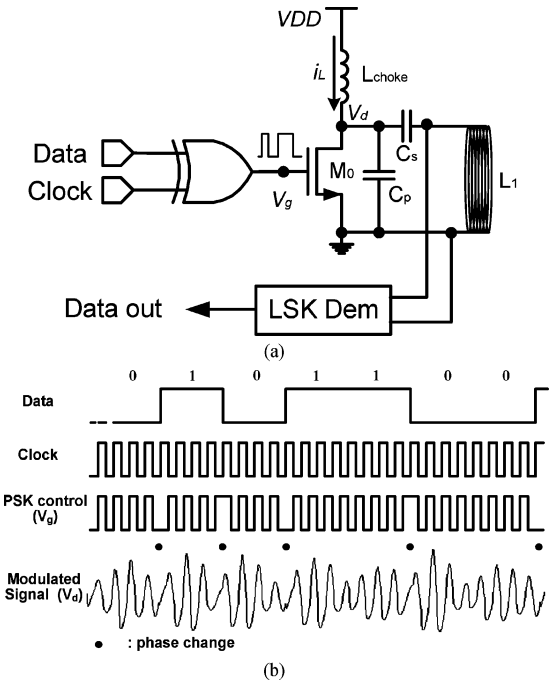


Fig. 2. (a) External device circuit (in a battery-based DSP). (b) PSK modulation scheme.

modulation scheme is also shown in Fig. 2(b). Moreover, the phase changes with 180° within two carrier cycles are independent of the Q of the LC tank to reduce the required power dissipation. As M_0 is turned on, C_p is equivalently shorted to ground, and the resonance frequency ω_s can be derived as

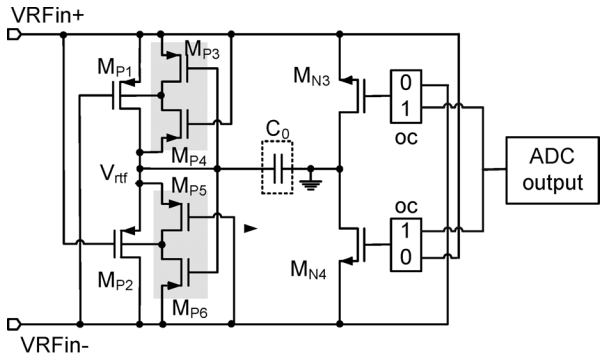
$$\omega_s = \frac{1}{\sqrt{L_1 C_s}}. \tag{1}$$

Otherwise, the resonance frequency under the turned-off status is revised as

$$\omega_p = \frac{1}{\sqrt{L_1 \frac{C_s C_p}{C_s + C_p}}}. \tag{2}$$

B. CMOS Bridge Rectifiers With Leakage Current Reduction and Back Telemetry Mechanism

The current mode CMOS bridge rectifier is widely used in biomedical applications [8]. The LC tank circuit in the receiver converts the AC carrier to a DC voltage to charge/supply the detectors and the charger circuit. To improve the degraded power conversion efficiency resulting from the time-varied coupling voltage in the coil, the latch up and body effect in the rectifier should be eliminated as soon as possible. The utilization of additional auxiliary transistors M_{P3}–M_{P6} in the rectifier design [9], as shown in Fig. 3, can dynamically control the substrate voltage of M_{P1} and M_{P2} to reduce the dropout voltage between the source and the body of transistors, and then further eliminate the body effect. Moreover, the bodies of the transistors M_{P1} and M_{P2} are connected to a potential higher than their source voltage. Therefore, the leakage can be reduced, and the voltage of rectification increases because the parasitic BJTs are turned off all the time.



oc / function	Operation
Mode 0	Rectification
Mode 1	Sensed Data Transmission

Fig. 3. CMOS full-wave bridge rectifier with leakage reduction and sensed data transmission mechanism.

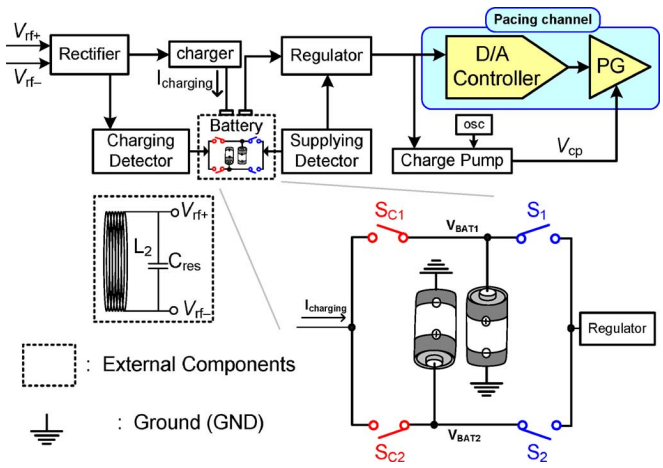


Fig. 4. Block diagram of a two-battery-based power management system.

The telemetry inside the proposed IMSoC is a bidirectional interface [10]. Aside from transmitting the parameters and rectifying the power from external devices in the implanted system, the telemetry using the load shift keying (LSK) technique transmits wireless data from the implanted sensing channel to the external devices.

To reduce the required turns of the extra coils, the bidirectional communications, including rectification and sensed data transmission, share the unique coil (L_2) to save the area of the implantable device. The operation mode depends on the data inside "oc" in Fig. 3 between rectification and sensed data transmission.

C. Two-Battery-Based Power Management System

Fig. 4 demonstrates the architecture of the two-battery-based power management system with pacing channel, including a two-battery network with path switch, two detectors with charging and supplying, a charger circuit, a regulator, and a charge pump for the high-voltage pacing requirement.

The charging and supplying detectors, as shown in Fig. 5, control the switches "$S_{C1,2}$" and "$S_{1,2}$", respectively, in the

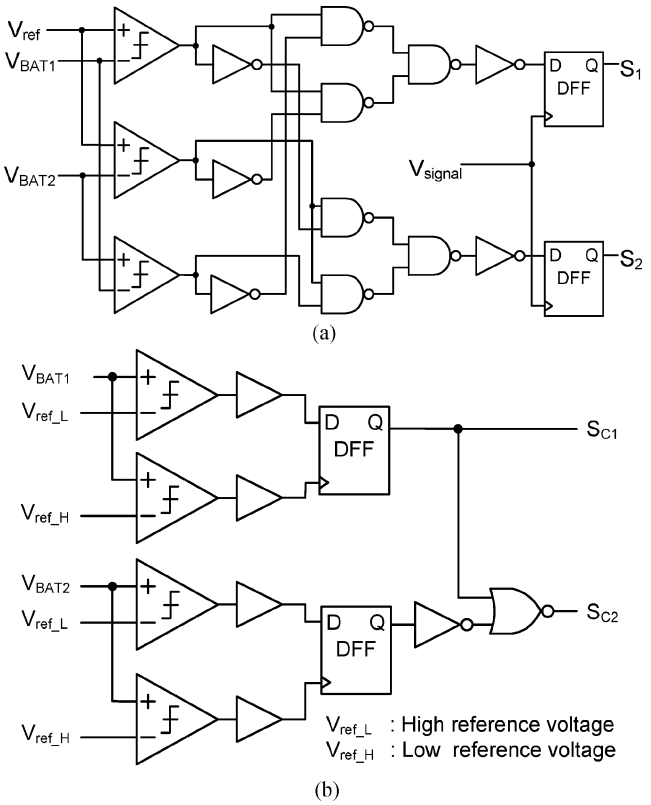


Fig. 5. (a) Supplying detector. (b) Charging detector.

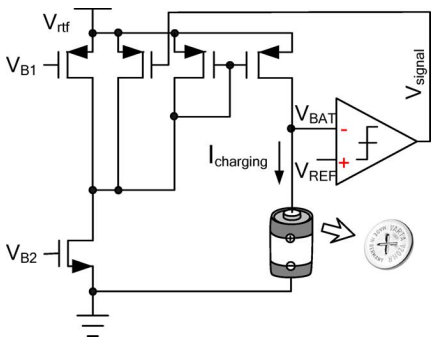


Fig. 6. Control circuit of the charger.

two-battery network to provide a nonstop energy source for the IMSoC. If the system is operating, the supplying detector [Fig. 5(a)] compares the output voltage of the working battery with a reference value, and the switches exchange their logic; the output voltage of the working battery is less than the desired value. Simultaneously, the charging detector [Fig. 5(b)] compares the output voltage of the idle battery with two reference values to decide if the battery has a charging request. The control circuit of the charger [11], as shown in Fig. 6, is employed to provide the stable current $\mathrm{I_{charging}}$ if the potential of the idle battery is less than the $\mathrm{V_{REF}}$ of 1.4 V. All the operations in the proposed power management system are automatic and can guarantee the working battery with at least 72% charge capacity.

The charger circuit, which consists of a differential pair with a current source, a current mirror, and a comparator, is employed to provide a constant current ($\mathrm{I_{charging}}$) of about 2 mA to charge the rechargeable batteries (2 pieces of *Vatra*® V6HR:

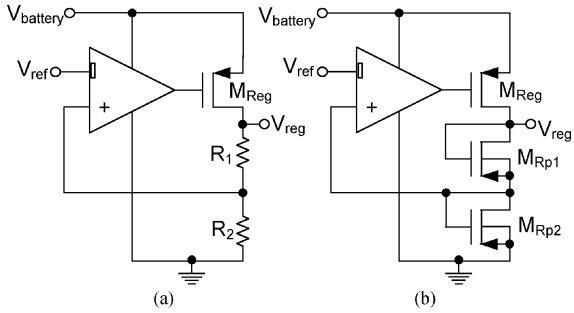


Fig. 7. (a) Conventional LDO regulator. (b) Low quiescent current LDO regulator.

NiMH rechargeable battery that can be recharged 1000 times with a normal output voltage of 1.2 V). The regulator, followed by the two-battery network, provides a stable supply voltage to the analog and digital circuits in the IMSoC.

In the proposed IMSoC, the regulator plays the role of suppressing the voltage variation of the battery and of providing a more stable supply voltage to the system and the charge pump. Fig. 7(a) [12] shows a conventional regulator that consists of an error amplifier, a PMOS pass element, and one set of feedback network with two divided resistors. The drawback is that the divided resistors must be large enough to reduce the passing quiescent current, but it results in a large area. Therefore, a low-dropout (LDO) regulator [Fig. 7(b)] with two pseudo-resistors, $\mathrm{M_{Rp1}}$ and $\mathrm{M_{Rp2}}$, as the feedback network is employed [13] to solve the problem of a large area. Moreover, the error amplifier is operated in a sub-threshold region to save on power consumption. Finally, the regulated voltage of 1 V is applied to operate most of the circuits in the IMSoC.

D. Dual-Voltage Programmable Pacing Channel

Fig. 8 shows the proposed pacing channel with low-voltage (D/A controller) and high-voltage (PG, Pulse generator) parts [13]. The low-voltage part is composed of an offset DAC, a high-to-low conversion circuit, and a low-power comparator. A low-power (965 nW) level shift buffer and three transistors in the output stage comprise the high-voltage interface. The supply voltage in the output is 3.2 V generated by the output of the charge pump [6], as shown in Fig. 4; this value is also the full amplitude of the stimulation. According to the different cases of the patients, the required strength of stimulation can be adjusted by controlling the logic parameters of an offset DAC using the system controller. Caused by the different supply voltages between the PG of up to 3.2 V and the D/A controller with a 1.4 V supply, the charge-redistribution circuit [13] is utilized to serve as a bridge. Furthermore, at the circuit design level, an equivalent model [14], [15] is required to simulate the behavior of the heart. To obtain the corresponding value of each component, the cathode and anode are assumed 10 $\mathrm{mm^2}$ and 50 $\mathrm{mm^2}$, respectively. Moreover, the faradic resistance (43 $\mathrm{k\Omega}$) is assumed that the electrode for pacing is made of 5 mm-stainless steel [16].

Human systole has a particular frequency under normal conditions. Simultaneously, the peak pulses (R-wave) should be naturally triggered by the same frequency. The target of the proposed IMSoC is to provide stimulation pulses to protect the

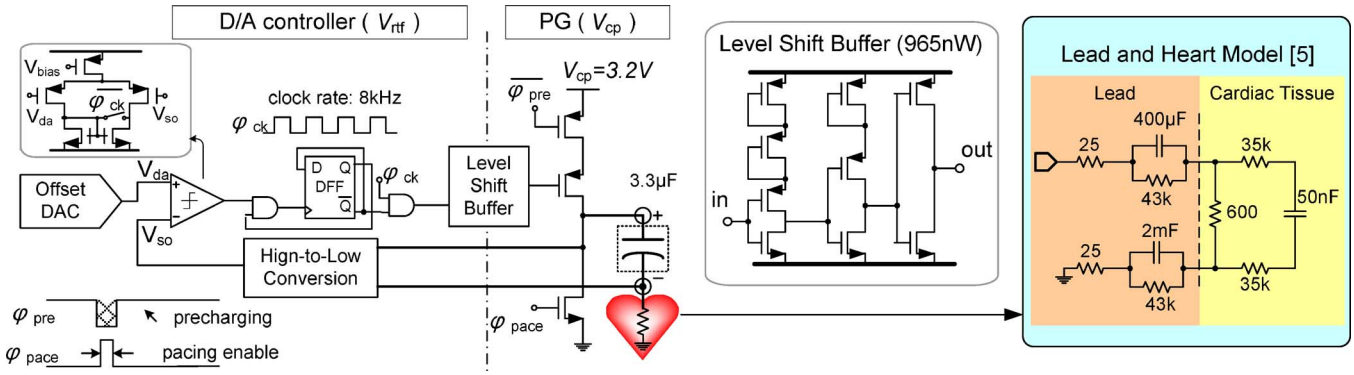


Fig. 8. Pacing channel with a heart model [14].

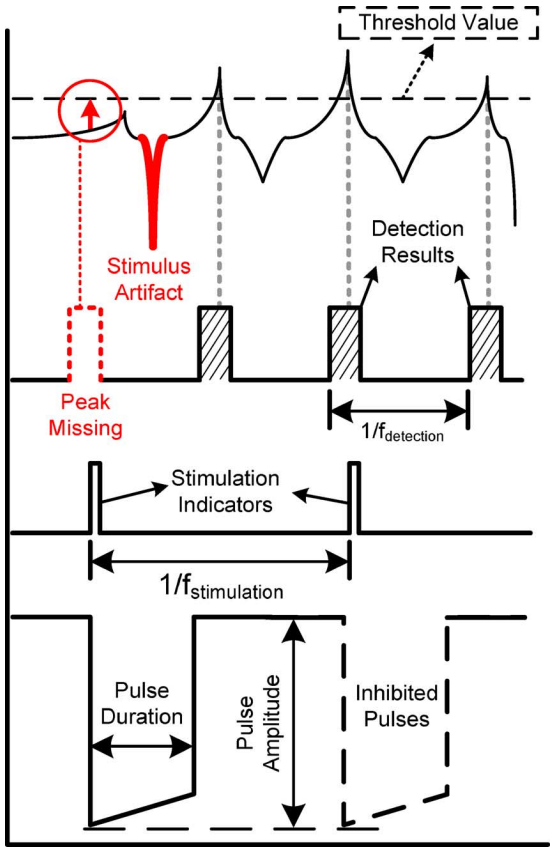


Fig. 9. Operation of the proposed IMSoC and the stimulation parameters.

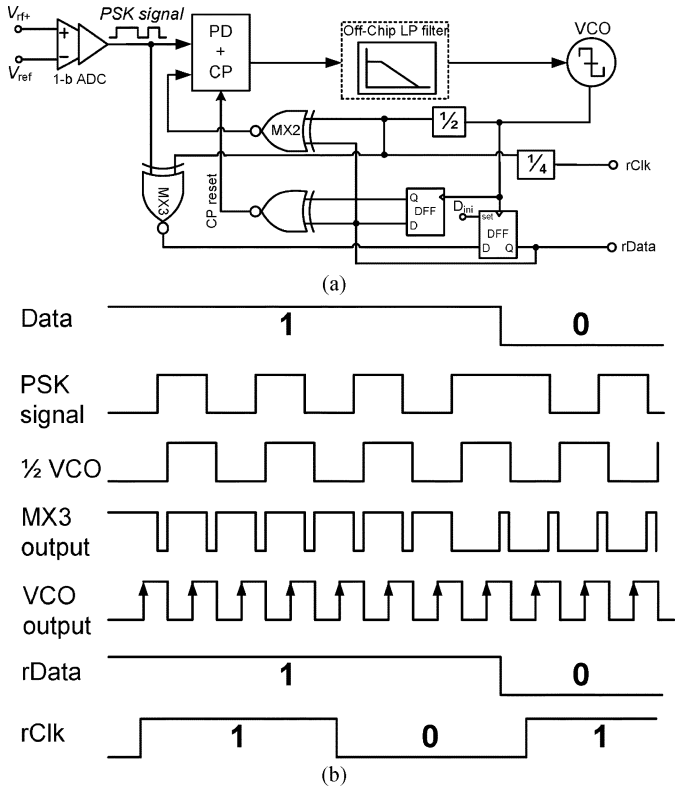


Fig. 10. (a) PSK demodulator with the PLL technique. (b) Relative operation.

heart from the lack of R-waves. As shown in the bottom of Fig. 9, the parameters of the stimulation include pulse duration, pulse amplitude, and stimulation frequency ($f_{stimulation}$). All stimulation parameters can be programmed by a system controller according to the control signal frame [Fig. 11(b)]. The detailed signal flowchart of the system controller will be described in the next Section. The pacing channel is enabled to generate the stimulation pulses, and the peak value of the R-wave is overlooked (the top of Fig. 9) within the stimulation indicators. The stimulation frequency depends on the physiology characteristics of the patients, and the decisions on the two other parameters (i.e., pulse amplitude and pulse duration) depend on the strength–duration curve [15].

IV. Digital Circuitry

A. PLL-Based PSK Demodulator

The PLL-based PSK demodulator is used to capture and restore the required clock and data, which are transmitted to the system controller to update the stimulation parameters. The circuit and operation of the PSK demodulation are shown in Fig. 10. Initially, the input analog signal from the coil coupling is converted to digital codes [8] as the modulated PSK signal by a 1-bit ADC. The digital PLL circuit synchronizes certain signals, such as the PSK data, the oscillating signal of the voltage-controlled oscillator (VCO), and the recovered data, by detecting the phase difference [17].

To recover the clock and data, the frequency of the VCO output signal is double than that of the PSK carrier when the

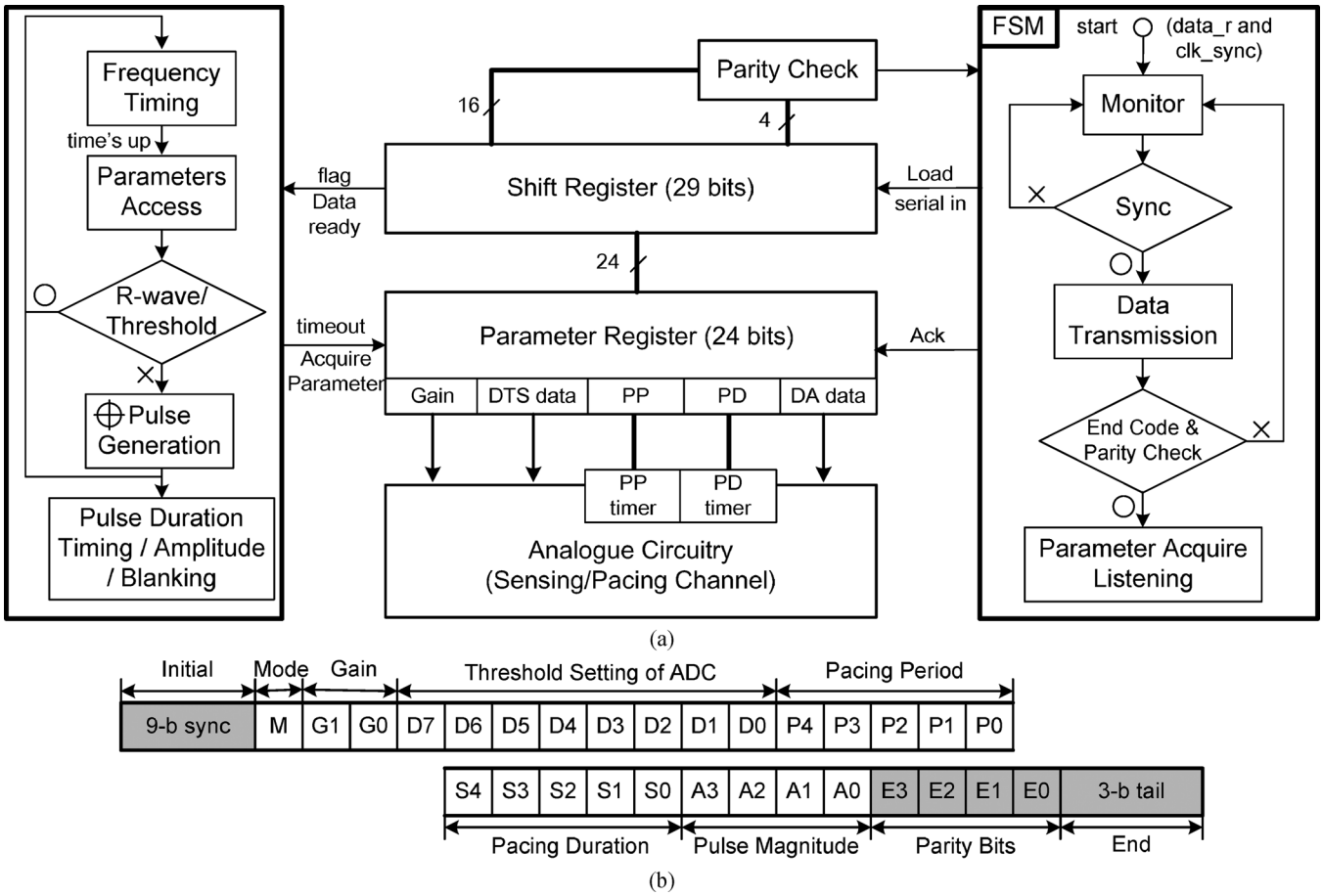


Fig. 11. (a) Signal flowchart of the system controller. (b) Format of the 41-b control signal frame.

PLL is locked in the phase. The PSK modulated signal and the half-frequency signal of the VCO are calculated logically by the exclusive-NOR gate MX3. The calculated result is on standby at the D flip-flop (DFF). Furthermore, according to the operation in Fig. 10(b), the final recovered PSK demodulated data (rData) can be acquired correctly at the output of the DFF, which was clocked by the output of the VCO. However, in the output of the phase detector, the error pulses, which result from the phase difference of two transition edges between the PSK signal and the output signal of MX2, could destroy the lock of the PLL at an instant time and result in a clock recovery error. To avoid the errors from the phase transitions, the signal "CP reset" is used to generate a signal and maintain constant voltage at the output of the charge pump during the phase transition, then it can ensure that the output voltage of the charge pump is stable when the phase transition of the PSK signal occurs.

TABLE I
DEFINITION AND PROPERTIES OF THE SYSTEM CONTROLLER PARAMETERS

Register [bit #]	Parameters	Properties
Mode[1]	Filter Function	Lowpass/Bandpass
Gain [2]	Amplification Rate	Preamplifier: 20/30dB SCamp @ ADC: 2/5 times
DTS data [8]	Threshold value of R-wave Detection	200–600 mV
PP [5]	Pacing Period (Frequency)	32 ms–2 s (0.5–31.25 Hz)
PD [5]	Pulse Duration	62.5 μ s–1.94 ms
DA data[4]	Pulse Magnitude	-0.2–3.2 V

B. System Controller

In the telemetry system, initial identification bits, parity bits, and end codes are used together to sustain the system controller with an online accuracy protection function [17]. The system controller in the proposed IMSoC is designed according to the algorithm in Fig. 11, including the shift registers for the store of the logic parameters, the functions of data confirmation, and the operation identification. The parameters mapping the registers and the properties are listed in Table I.

The proposed system controller is composed of a finite state machine (FSM), a series of logic registers, and a commander. The FSM receives data from the external device, and then it monitors its characteristics to determine the location of the start/end frames. The parity bits before the end frame are executed by a system controller, which waits for the timeout

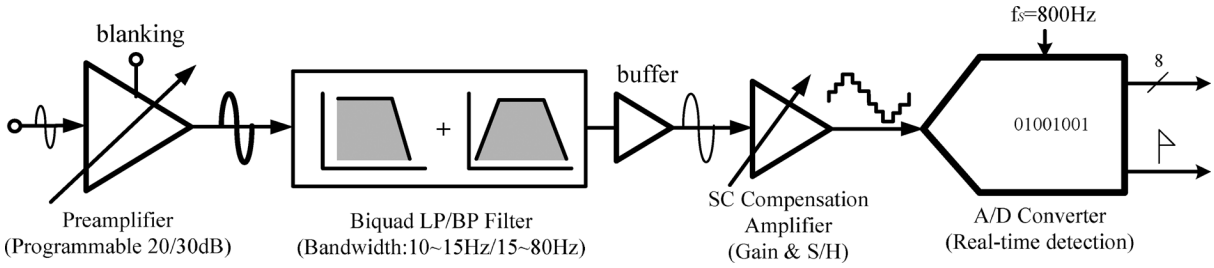


Fig. 12. Block diagram of the monitoring analog front end.

signal from the pacing period. If the correct frame is received, an acknowledgement (Ack) signal is replied to indicate the reception completely. Otherwise, the data frame is ignored because no Ack is replied. The start (sync) bits, parity bits, and end bits are helpful in guaranteeing data correction.

According to the R-wave detection and the data stored in the registers, the commander determines if the stimulation pulse is required for the patients. For example, in a practical application, the surgeon decides the logic parameters depending on the disease of the patient and delivers them to the system controller. In a healthy condition, the patient's heart completes the systole normally to generate the regulated R-waves. Otherwise, if the patient suffers from a heart disease that causes the elimination of the original level of R-wave (refer to the mark in Fig. 9, which indicates that the peak value of the R-wave is missing), the commander enables the pacing channel to trigger the stimulation pulse with a fixed frequency and the preset duration/magnitude until the patient's systole is restored.

V. Sensing Channel

The sensing channel includes a MAFE and an LSK modulator. The main components inside a MAFE, as shown in Fig. 12, are a programmable-gain preamplifier with the structure of a differential difference amplifier (DDA), a second-order filter with an optional LP/BP response, and a successive approximation ADC (SAADC) with real-time threshold detection.

A. Programmable-Gain Preamplifier

The potentials of the stimulated objective are detected and amplified by the first-stage preamplifier with a differential difference structure to achieve a programmable gain under low-supply voltage [5], [18]. Referring to Fig. 13, the capacitance ratio between C_{d1}/C_{d2} and C_f determines the amplification of the 21/31 dB, respectively. Blanking switches are implemented in the amplifier [5] to prevent the saturation of the MAFE from the large stimulation pulses [19] induced by the pacing generator of a pacing channel. Moreover, to avoid any possible problems due to the different DC levels of input electrodes, this preamplifier is designed under a band-pass function to eliminate the large DC shift in the output.

B. Second-Order Continuous-Time Filter With LP/BP Response

A second-order filter based on the operational transconductance amplifier-C (OTA-C) structure with an LP/BP response is used on the MAFE to filter the out-of-band interference. The sensing channel operated in two modes includes the ECG

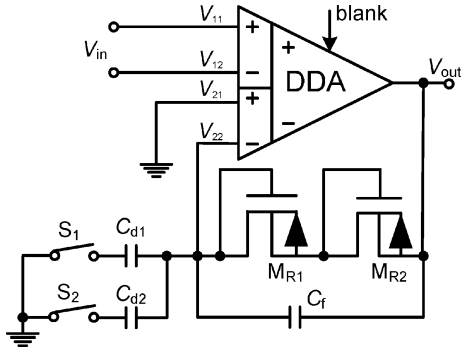


Fig. 13. Circuit diagram of the programmable-gain preamplifier.

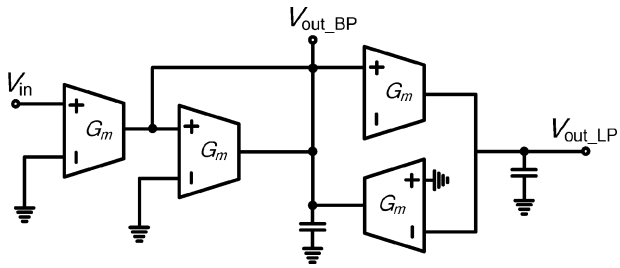


Fig. 14. Second-order LP/BP filter.

full waveform with an LP filter and the detection of R-wave magnitude with a BP filter. In Fig. 14, the second-order filter, which provides the LP/BP outputs (V_{out_LP}/V_{out_BP}), uses only 4 OTAs to save power and area. To achieve low transconductance (G_m), the techniques of source degeneration and current cancellation are employed in the design of OTA, which is also operated in a sub-threshold region to save on power consumption [5].

C. SAADC With Real-Time Threshold Detection

The final stage of the sensing channel before the LSK modulator is a SAADC with real-time threshold detection, the timing and block diagrams of which are demonstrated in Fig. 15 [5]. A programmable switched capacitor amplifier, which serves as a sample-and-hold circuit prior to the comparator, is developed with a gain of 2/5 times. The proposed real-time detection ADC provides two functions, including threshold detection and A/D conversion. They can be reused by SAADC in the sensing mode to save on power consumption, as the threshold detection requires circuits, including a DAC, an S/H, and a comparator. Thus, the proposed ADC consumes only 41 nW by sharing most of the components for these two functions. Based on the

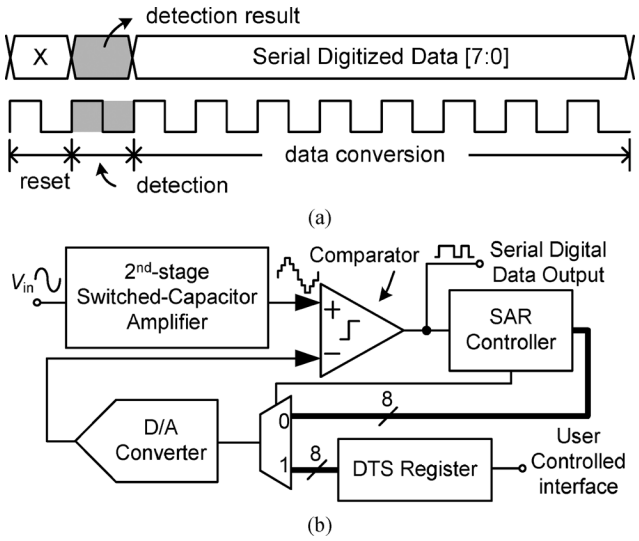


Fig. 15. (a) Timing and (b) block diagrams of real-time detection ADC.

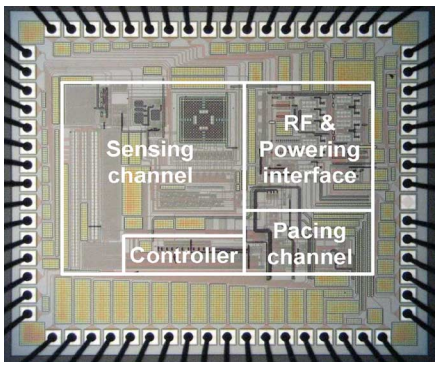


Fig. 16. Chip microphotograph of the proposed IMSoC.

timing diagram shown in Fig. 15(a), the functions of amplification, threshold detection, and A/D conversion are implemented during each sample-and-hold period, respectively.

VI. *In* Vivo Experiment

The proposed IMSoC was fabricated using the TSMC 0.35 μm 2P4M process with an area of 1.5×1.6 mm^2. The microphotography of the chip is shown in Fig. 16.

Four male 10-week SD rats weighing approximately 250–300 g each were used. The experiments conducted in the present study were approved by the Animal Research Committee of National Chiao Tung University. The rats were anesthetized with intraperitoneal injection of sodium pentobarital (50 mg/kg) and were mechanically ventilated with room air. Body temperature was maintained at $\sim$ 37°C throughout all surgical procedures via a servo-controlled heating pad. After anesthetization, the rats were placed in dorsal recumbency. The trachea was palpated, and a midline incision from the caudal end of the larynx to the suprasternal was made. Using blunt dissection, the sternothyroideus muscle from the sternomastoideus was separated. The sheath was carefully incised to expose the carotid artery, jugular vein, and vagus nerve.

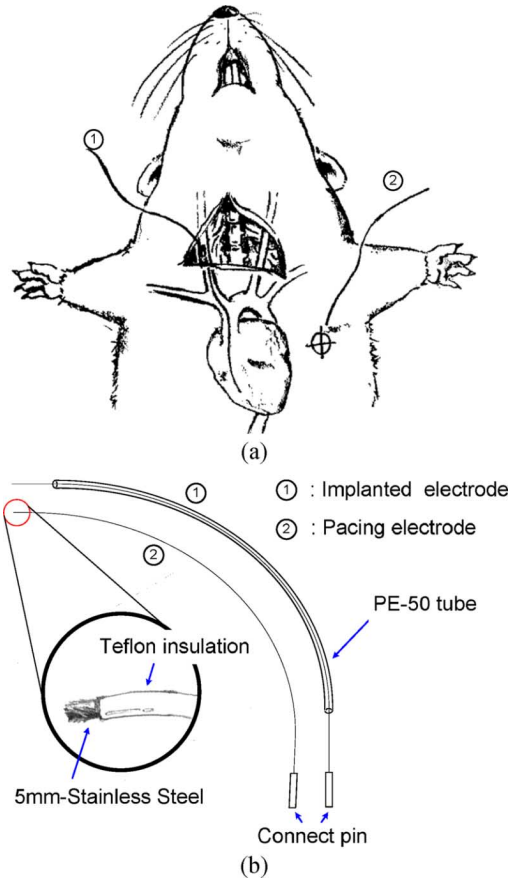


Fig. 17. Animal surgical setup. (a) Carotid artery cannulation. (b) Implanted and pacing electrode diagram.

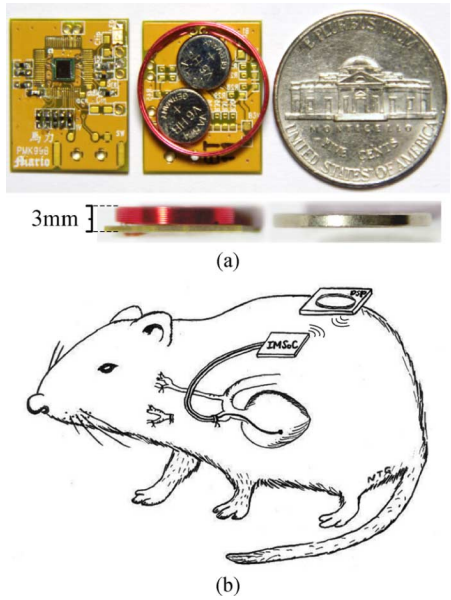


Fig. 18. (a) Top/bottom views and the scale of implanted device. (b) Communication between the implanted IMSOC and the external DSP device.

The right internal carotid artery was cannulated with a heparinized saline-filled catheter (200 U/ml, PE-50, with internal and external diameters of 0.58 and 0.965 mm, respectively; Clay Adams Co., USA). The catheter was then inserted bevel-up into the artery and toward the right ventricle, with its curvature directed towards the midline, as shown in Fig. 17(a). Next, the

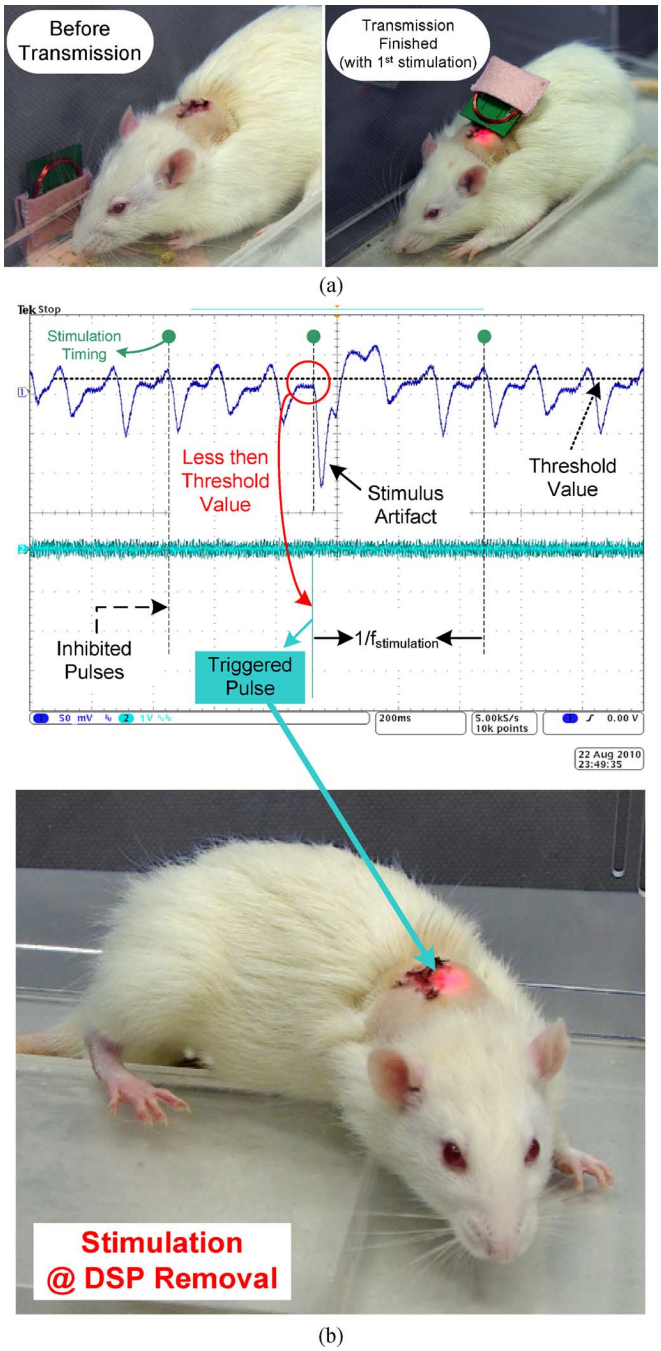


Fig. 19. *in vivo* experiment results. (a) Before and after parameter transmission. (b) Inhibited and triggered pulse with artifact to emit LED.

TABLE II
IMSoC Specifications

General		
Technology	TSMC 0.35 μm 2P4M	
Chip area	1.25×1.85 mm^2	
Carrier frequency	256 kHz	
Digital Blocks		
PSK Demodulator	power	1.76 μW @ 1 V
	sampling frequency	4 MHz
System Controller	power	260 nW @ 1 V
	operation frequency	32 kHz
Programmable Ranges	stimulation frequency	0.5–31.25 Hz
	stimulus amplitude	0–3.2 V
	stimulus duration	62.5 μs –1.94 ms
Power Interface and Pacing Channel		
Rectifier	2 V output with induced voltage of 2.9 V_{pp}	
Regulator	power	7 μW @ 1V
Charge Pump	power	10 μW
	output voltage (@ 1 V input voltage)	3.2 V
	pumping clock frequency	16 kHz
Power Management (Supply Detector, Charge Detector, and Charger)	power	20 μW
	charging current	2 mA
	Battery (6 mAh @ 1.2 V supply voltage)	2 x V6HR, (1000 times recharging)
D/A Controller	power	42nW @ 1 V
	operation frequency	8 kHz
Pulse Generator	power (pacing period = 1 s; pulse duration = 0.5ms)	15.5μW @ 3.2 V
Monitoring Analog Front End @ 1.4 V		
Preamplifier	power	40 nW
	Input referred noise	1.1 $μV_{rms}$
	3-dB bandwidth	0-140 Hz
	DC gain	21/31 dB
Biquad Low-Pass/ Band-Pass Filter	power	126 nW (with buffer)
	3-dB Bandwidth	
	Low-Pass	0–15 Hz
	Band-Pass	15–80 Hz
Real-time Detection ADC	power	71 nW (with SCAMP)
	resolution	8 bits
	sampling frequency	800 Hz
	sample-and-hold gain	2/5 times

homemade electrode (no.15140/13848, 50 μm in diameter; California Fine Wire Co., USA) was deposited in the lumen with PE-50 catheter, as shown in Fig. 17(b), was advanced into the artery, and was stopped at the appearance of a ventricular curve. The electrode was coiled in a single loop at the site of cannulation and was subsequently sutured to the underlying muscle.

The anesthetized animal was also given a dorsal midline incision (4 cm). Blunt dissection was used to tunnel subcutaneously into the implanted site and create a pocket for the IMSoC. The IMSoC, which was coated with the biocompatible polymer polymethyl-methacrylate (Cranioplastic, C.M.W. Laboratories, Ltd., Blackpool, UK), was inserted through a dorsal midline incision in the skin distal to the neck. Next, the IMSoC was connected to the electrode externalized at the back (Fig. 18). Finally, the incision was sutured with 5/O nylon (Prolene, Ethicon, Johnson & Johnson Medical Ltd., N.S.W., Australia) and covered with two strips of elastoplast (Leukoplast, Hamburg, Germany) to prevent the tearing of the wound.

Fig. 19 demonstrates the *in vivo* experiments conducted by implanting the IMSoC into the rats (Fig. 18) and presents one measured closed-loop behavior of triggering and inhibition. The IMSoC receives the input RF power and the configuration of the stimulus parameters from the battery-based DSP maintained by the rat's side. In Fig. 19(a), as the parameter transmission is

TABLE III
COMPARISON OF PAPERS ON PACEMAKERS

Functions		JSSC'04 [20]	TCASI'04 [21]	TCASI'05 [22]	This work	*Brand-X Pacemaker
Process/Die Area		0.5 μm/49 mm^2	0.35 um/1.3 mm^2	0.13 μm/1 mm^2	0.35 μm/4.6 mm^2	N/A
RF-Coupling Transmission		×	×	×	✓	×
Rechargeable		×	×	×	✓	×
Programmable pacing		✓	×	×	✓	×
Multiplex B.W. / gain		×/×	×/✓	×	✓/✓	×
EGM Sensing		✓	✓	×	✓	✓
R-wave detection		×	×	✓	✓	✓
Voltage / Power	detection	N/A	N/A	1 V / 100 nW	1 V / 237 nW	3.2 V/ 55 0μW
	sensing	2.8 V / 8 μW	1.8 V/3.2 μW	N/A		
	Programmable		N/A	N/A	1 V / 260 nW	N/A
	Whole system	2.8 V / 8 μW	1.8 V / 3.2 μW	1 V / 100 nW	1 V / 48 μW	3.2 V / 550 μW

*brand-X: a widely used pacemaker product in hospitals provided by National Taiwan University Hospital Yun-Lin Branch, Yun-Lin, Taiwan

completed, the first stimulation occurs, accompanying the illumination of the red light-emitting diode (LED). The maximum operation distance of the IMSoC is approximately 25–45 mm in the animal experiment. The MAFE amplifies the EGMs measured from the implanted catheter and subsequently recognizes the R-beat at a detection rate of 1 kHz. When one R-beat is present within a stimulation period of 400 ms, the stimulus is inhibited by the controller. Conversely, intracardiac stimulation (amplitude: -3.2 V; pulse duration: 0.5 ms) is performed at the detected R-R beat interval longer than 400 ms in the conscious rodent experiment. Simultaneously, the stimulation is visually indicated by illuminating the LED. One stimulus artifact appears after 20 ms of the intracardiac stimulation, as shown in Fig. 19(b). The specification summary of the entire IMSoC is presented in Table II, including the digital blocks, powering interface, pacing channel, and MAFE.

The proposed IMSoC employing the endocardial as the stimulated model can be regarded as a pacemaker. Unlike that in some studies on the pacemaker [20]–[22] and commercial products, as shown in Table III, the proposed IMSoC provides not only the basic functions, such as sensing and detection, but also some practical techniques, including programmable pacing parameters, low-power MAFE with multiplex bandwidth/gain, and smart power management.

VII. CONCLUSION

A low-power IMSoC with smart powering management, immediate signal acquisition, and wireless telemetry system, is developed. A 237 nW analog front-end senses the bio-signal and replies to the system controller if the stimulation is required. Moreover, the required stimulation pulse decided by user-defined parameters from the external DSP can be carried out by a digital controller and a pacing channel. The *in vivo* experiment is studied to demonstrate closed-loop behavior and reliability. Compared with the recent pacemakers in the market, the proposed IMSoC features low power consumption, ultra small size, and rechargeable mechanism.

ACKNOWLEDGMENT

The authors would like to thank the Chip Implementation Center (CIC) of Taiwan for its technical support and the CBIC Laboratory members M-Y. Huang, C-P. Wang, and C-J. Cheng for their assistance.

REFERENCES

[1] G. Wang, W. Liu, M. Sivaprakasam, and G. A. Kendir, "Design and analysis of an adaptive transcutaneous power telemetry for biomedical implants," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 52, no. 10, pp. 2109–2117, Oct. 2005.

[2] P. Cong, N. Chaimanonart, W. H. Ko, and D. J. Young, "A wireless and batteryless 130 mg 300 μW 10 b implantable blood-pressure-sensing microsystem for real-time genetically engineered mice monitoring," in *Proc. IEEE Int. Solid-State Circuits Conf.*, Feb. 2009, pp. 428–429.

[3] P. Li and R. Bashirullah, "A wireless power interface for rechargeable battery operated medical implants," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 54, no. 10, pp. 912–916, Oct. 2007.

[4] M. Ghovanloo and K. Najafi, "A wireless implantable multichannel microstimulating system-on-a-chip with modular architecture," *IEEE Trans. Neural Syst. Rehabil. Eng.*, vol. 15, no. 3, pp. 449–457, Sep. 2007.

[5] S. Y. Lee, C. J. Cheng, and M. C. Liang, "A low-power bidirectional telemetry device with a near-field charging feature for a cardiac microstimulator," *IEEE Trans. Biomed. Circuits Syst.*, vol. 5, no. 4, pp. 357–367, Aug. 2011.

[6] S. Y. Lee, Y. C. Su, M. C. Liang, J. H. Hong, C. H. Hsieh, C. M. Yang, Y. Y. Chen, H. Y. Lai, J. W. Lin, and Q. Fang, "A programmable implantable micro-stimulator SoC with wireless telemetry: Application in close-loop endocardial stimulation for cardiac pacemaker," in *Proc. IEEE Int. Solid-State Circuits Conf.*, Feb. 2011, pp. 44–45.

[7] G. Wang, W. Liu, M. Sivaprakasam, M. Zhou, J. D. Weiland, and M. S. Humayun, "A wireless phase shift keying transmitter with Q-independent phase transition time," in *Proc. IEEE 27th Engineering in Medicine and Biology Society Conf.*, Sep. 2005, pp. 5238–5241.

[8] A. Facen and A. Boni, "A CMOS analog frontend for a passive UHF RFID tag," in *Proc. ACM Int. Low Power Electron. Design Symp.*, Oct. 2006, pp. 280–285.

[9] M. Ghovanloo and K. Najafi, "Fully integrated wideband high-current rectifiers for inductively powered devices," *IEEE J. Solid-State Circuits*, vol. 39, no. 11, pp. 1976–1984, Nov. 2004.

[10] S. Atluri and M. Ghovanloo, "An integrated full-wave CMOS rectifier with built-in back telemetry for RFID and implantable biomedical applications," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 55, no. 10, pp. 3328–3334, Nov. 2008.

[11] P. Li and R. Bashirullah, "A wireless power interface for rechargeable battery operated medical implants," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 54, no. 10, pp. 912–916, Oct. 2007.

[12] R. J. Milliken, J. Silva-Martinez, and E. Sanchez-Sinencio, "Full on-chip CMOS low-dropout voltage regulator," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 54, no. 9, pp. 1879–1890, Sep. 2007.
[13] C. J. Cheng, C. J. Wu, and S. Y. Lee, "Programmable pacing channel with a fully on-chip LDO regulator for cardiac pacemaker," in *Proc. IEEE Int. Conf. Asian Solid-State Circuits*, Nov. 2008, pp. 285–288.
[14] A. Bolz and M. Schaldach, "Model of the pacing behaviour of electrostimulation systems based on the electrochemical properties of the electrodes," in *Proc. IEEE 15th Engineering in Medicine and Biology Society Conf.*, Oct. 1993, pp. 855–856.
[15] J. G. Webster, *Design of Cardiac Pacemakers*. Piscataway, NJ: IEEE Press, 1995.
[16] L. A. Geddes and R. Roeder, "Measurement of the direct-current (faradic) resistance of the electrode-electrolyte interface for commonly used electrode materials," *Ann. Biomed. Eng.*, vol. 29, pp. 181–186, 2001.
[17] W. Xu, Z. Luo, and S. Sonkusale, "Fully digital BPSK demodulator and multilevel LSK back telemetry for biomedical implant transceivers," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 56, no. 9, pp. 714–718, Sep. 2009.
[18] R. R. Harrison and C. Charles, "A low-power low-noise CMOS amplifier for neural recording applications," *IEEE J. Solid-State Circuits*, vol. 38, no. 6, pp. 958–965, Jun. 2003.
[19] L. Lentola, A. Mozzi, A. Neviani, and A. Baschirotto, "A 1-μA front end for pacemaker atrial sensing channels with early sensing capability," *IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process.*, vol. 50, no. 8, pp. 397–403, Aug. 2003.
[20] L. S. Y. Wong, S. Hossain, A. Ta, J. Edvinsson, D. H. Rivas, and H. Nääs, "A very low-power CMOS mixed-signal IC for implantable pacemaker applications," *IEEE J. Solid-State Circuits*, vol. 39, no. 12, pp. 2446–2456, Dec. 2004.
[21] A. Gerosa, A. Maniero, and A. Neviani, "A fully integrated dual-channel log-domain programmable preamplifier and filter for an implantable cardiac pacemaker," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 51, no. 10, pp. 1916–1925, Oct. 2004.
[22] J. N. Rodrigues, T. Olsso, L. Sornmo, and V. Owall, "Digital implementation of a wavelet-based event detector for cardiac pacemakers," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 52, no. 12, pp. 2686–2698, Dec. 2005.

Shuenn-Yuh Lee (M'98) was born in Taichung, Taiwan, in 1966. He received the B.S. degree from National Taiwan Ocean University, Chilung, Taiwan, in 1988, and the M.S. and Ph.D. degrees from National Cheng Kung University, Tainan, Taiwan, in 1994 and 1999, respectively.

In 2002 and 2006, he was an Assistant Professor and Associate Professor at the Institute of Electrical Engineering, National Chung Cheng University, Chia-Yi, Taiwan, respectively, where he is currently a Full Professor. His current research interests include design of analog and mixed-signal integrated circuits (ICs), including filter, high-speed analog-to-digital converter (ADC)/digital-to-analog convertor (DAC), and sigma-delta ADC/DAC, biomedical circuits and systems, low-power and low-voltage analog circuits, and radio-frequency front-end integrated circuits for wireless communications.

Dr. Lee is a member of Circuits and Systems (CAS) Society, Solid-State Circuits Society, Communication Society, and Medicine and Biology Society of IEEE.

Mario YuCheng Su (S'08) was born in Chiayi, Taiwan, in 1984. He received the B.S. degree in electrical engineering from National Chung Cheng University, Taiwan, in 2006.

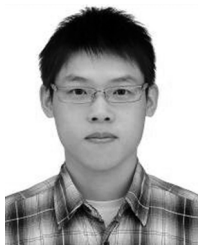
He is currently working toward the Ph.D. degree at the Institute of Electrical Engineering, National Chung Cheng University, Chia-Yi, Taiwan. He is the scholarship holder of the Sandwich-Program between National Science Council (NSC), Taiwan, and Deutscher Akademischer Austausch Dienst (DAAD), Germany, to carry out a research in Chair of Integrated Analog Circuits and RF Systems (IAS), RWTH Aachen University, Germany. His research interests include the design of low-voltage and low-power analog integrated circuits as well as biomedical circuits and systems.

Ming-Chun Liang was born in Pingtung, Taiwan, in 1981. He received the B.S. degree from National Cheng Kung University, Taiwan, in 2004.

He is working toward the Ph.D. degree at the Institute of Electrical Engineering, National Chung Cheng University, Chia-Yi, Taiwan. His research interests include the design of low-voltage and low-power analog integrated circuits as well as biomedical circuits and systems.

You-Yin Chen received the Ph.D. degree in electrical engineering from the National Taiwan University, Taiwan, in 2004.

He is an Associate Professor at the Department of Biomedical Engineering of the National Yang Ming University in Taipei, Taiwan. His research interests are to carry out engineering-based modeling and experimental studies of brain function with applications to understanding and treating neurological disease. Currently, he is focusing clinically-related studies on Parkinson's disease in human and animal model. His approaches use the combination of neural images and neural signal analysis to investigate processing in a variety of brain areas.



Cheng-Han Hsieh was born in Taichung, Taiwan, in 1987. He received the B.S. degree in electrical engineering from National Chung Cheng University, Taiwan, in 2009.

He is working toward the Ph.D. degree at the Institute of Electrical Engineering, National Chung Cheng University, Chia-Yi, Taiwan. His research interests include the design of pipelined analog-to-digital converter, and biomedical circuits and systems.

Chung-Min Yang was born in Taichung, Taiwan, in 1986. He received the B.S. and M.S. degrees in electrical engineering from Da-Yeh University, Dacun, Changhua, Taiwan, and National Chung Cheng University, Taiwan, in 2008 and 2010, respectively.

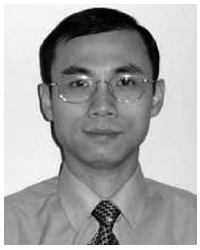
His research interests include the design of power management, data modulation, clock and data recovery (CDR), and biomedical circuits and systems.

Hsin-Yi Lai was born in Taipei, Taiwan. She received the Ph.D. degree from the Institute of Electrical Control Engineering, National Chiao Tung University (NCTU), Taiwan, in 2011.

She is currently a Postdoctoral Fellow in the Institute of Electrical Control Engineering, NCTU. Her research interest is in neuroengineering, which involves the neural implant device, analysis of neural ensemble recordings, signal classification and recognition, neuroinformatics, brain-machine interfaces (BMI), neural image, and photoacoustic image. Her goal is to carry out engineering principles and technologies to develop the biocompatible implant and analyze biomedical signals and images for understanding and treating neurological disease.

Jou-Wei Lin holds the certificate of cardiovascular medicine and Ph.D. degree in medical informatics.

His main research interests are the applications of biomedical methodologies in cardiovascular studies. He has obtained a series of research grants with topics including the development of preventive decision support systems; construction of intelligent agents for health management; applications of national language processing tools to evaluate quality of care; and hypothesize biological models to illustrate physiological/pathological pathways in cardiovascular medicine. His research results have been published in top journals such as *Lancet*, *Journal of American College of Cardiology*, *Journal of Clinical Oncology*, *Diabetes Care*, *Journal of Clinical Endocrinology and Metabolism*, *Atherosclerosis*, and *Journal of American Medical Informatics Association*.



Qiang Fang (M'98) received the B.S. degree in applied physics from Tsinghua University, Beijing, China, and the Ph.D. degree in biomedical engineering from Monash University, Melbourne, Australia, in 1991 and 2000, respectively.

He joined Royal Melbourne Institute of Technology (RMIT) University, Melbourne, Australia, in 2000 and is currently a Senior Lecturer in the School of Electrical and Computer Engineering, RMIT. His major research interests include intelligent and miniaturised medical instrumentation, wearable and implantable body sensor network and pervasive computing technologies applicable to healthcare delivery.