Precise CMOS Current Sample/Hold Circuits Using Differential Clock Feedthrough Attenuation Techniques

Chung-Yu Wu, Chih-Cheng Chen, and Jyh-Jer Cho

Abstract—**New CMOS current sample/hold (CSH) circuits capable of overcoming the accuracy limitations in conventional circuits without significantly reducing operating speed are proposed and analyzed. A novel differential clock feedthrough attenuation (DCFA) technique is developed to attenuate the signal-dependent clock feedthrough errors. Unlike conventional techniques, the DCFA circuit allows the use of dynamic mirror techniques, and results in no additional finite output resistance errors or device mismatch errors. The test chip of the proposed fully differential CSH circuit with multiple outputs has been fabricated in 1.2-μm CMOS technology. Using a single 5-V power supply, experimental results show that the signal-dependent clock feedthrough error current is less than ± 0.4 μA for the input currents from -550 μA to 550 μA. The acquisition time for a 900–μA step transition to 0.1% settling accuracy is 150 ns. For a 410–μA_{p-p} input at 250 kHz with the fabricated fully-differential CSH circuit clocked at 4 MHz, a total harmonic distortion of -60 dB, and a signal-to-noise ratio of 79 dB have been obtained. The active chip area and power consumption of the fabricated CSH circuit are 0.64 mm^2 and 20 mW, respectively. Both simulation and experimental results have successfully verified the functions and performance of the proposed CSH circuits.**

I. Introduction

CURRENT-MODE circuits offer many potential advantages such as low voltage operation [1], [2], easy manipulation of signals [3], [4], and higher operating speed [5], [6], which make current-mode techniques an attractive alternative to conventional voltage-mode circuits. Additionally, in some applications, such as the readout of infrared detectors [7] or optical sensors [8], the output signals of the detectors or transducers are inherently currents. The direct use of current-mode circuits would simplify the design in such cases.

For current-mode data acquisition systems, current sample/hold circuits (CSH) are frequently required to freeze fast moving signals before processing by the system. Several CSH circuits have been reported [2], [5], [9]–[13]. However, the precision of these CSH circuits is limited mainly by clock feedthrough errors [1], [10], [14], [15]. Several clock feedthrough reduction techniques based on current cancellation ideas have been proposed [14], [15]. However, more errors are inevitably introduced by the additional current mirrors due to the finite output resistance effect [5], [12], [17]. Moreover, the gain accuracy and linearity of the current mirrors would be degraded when device mismatches occur [12], and it is not feasible to apply dynamic current mirror techniques to these circuits [17]. Another technique using Miller feedback [18] to reduce the signal-dependent clock feedthrough error voltage could be applied directly to the conventional CSH circuits. But the feedback switch in the Miller feedback circuitry still results in a signal-independent error voltage. In the CSH circuit, even if the error voltage is independent from the input current, the resulting error current still depends on the input current.

Manuscript received January 11, 1994; revised July 11, 1994. This work was supported by the United Microelectronics Corporation, Hsin-Chu, Taiwan, Republic of China, under Contract C81065.

C.-Y. Wu and C.-C. Chen are with the Integrated Circuits and Systems Laboratory, Department of Electronics Engineering, National Chiao-Tung University, Taiwan, Republic of China.

J.-J. Cho is with the United Microelectronics Corporation Hsin-Chu, Taiwan 300, Republic of China.

IEEE Log Number 9405724.

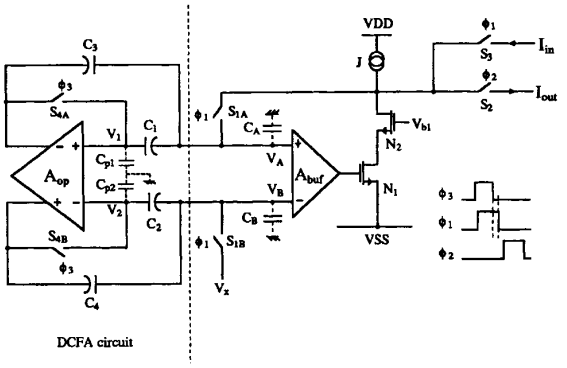

Fig. 1. Proposed CSH circuit with the differential clock feedthrough attenuation (DCFA) circuitry.

This paper presents new CSH circuit techniques capable of reducing the clock feedthrough errors and capacitive coupling errors [1], [16] without significantly degrading operating speed. Experimental results show that the proposed CSH circuit, fabricated by 1.2–μm CMOS technology, can obtain a current S/H function with a held step error of less than ± 0.4 μA for input ranging from -550 μA to 550 μA, while the acquisition time for a 900 μA step transition is 150 ns to 0.1% accuracy.

II. Proposed CSH Circuit

Fig. 1 shows the proposed CSH circuit. The amplifier $A_{\rm buf}$ is a differential voltage buffer, which amplifies the differential-mode component between its two inputs with a small gain and attenuates the common-mode component. The transistors N_1 and N_2, as well as $A_{\rm buf}$, form the core circuit to sample-and-hold the input current. The fully-differential operational voltage amplifier $A_{\rm op}$, a pair of feedback switches S_{4A} and S_{4B}, and four capacitors (C_1, C_2, C_3, and C_4), constitute the proposed differential clock feedthrough attenuation (DCFA) circuit. In the sample mode, the switches S_{1A}, S_{1B} and S_3 are closed. At the same time, switches S_{4A} and S_{4B} are also closed, which causes the amplifier $A_{\rm op}$ to be self-biased to the threshold point of its transfer characteristics. Through the closed-loop feedback, the gate voltage of N_1 is charged by the

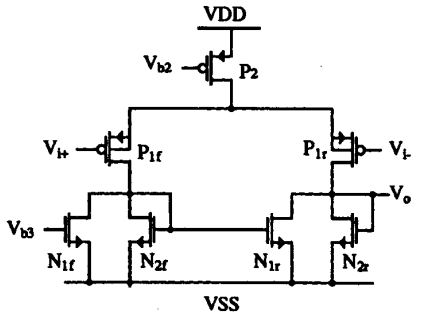

Fig. 2. The circuit diagram of the voltage buffer A_{buf} used in Fig. 1.

TABLE I
SIMULATED SIGNAL-DEPENDENT CLOCK FEEDTHROUGH ERRORS FOR THE INPUT RANGING FROM -550 μA to 550 μA

CIRCUIT	Clock Feedthrough Error
Conventional CSH [5], [14]	+/- 13.0 uA
Conventional CSH with Miller feedback [18]	+/- 12.0 uA
Proposed CSH without DCFA	+/- 4.5 uA
Proposed CSH with DCFA (Fig. 1)	+/- 0.23 uA
Proposed CSH with DCFA and 10% device mismatch (Fig. 1)	+/- 0.27 uA

voltage buffer A_{buf}, so that the drain current of N_1 is forced to be $(J + I_{\text{in}})$. To switch the circuit into the hold mode, switches S_{4A} and S_{4B} are turned off first, which enables the amplifier A_{op}. Then switches S_{1A} and S_{1B} are turned off and S_2 is turned on. The voltages at the input nodes of A_{buf} are ideally retained by the capacitors on these two nodes. Thus the drain current of N_1 is still equal to the value during the sample mode.

Actually, the turn-off transients of S_{1A}, S_{1B}, S_{4A}, and S_{4B} result in the clock feedthrough errors onto the charge holding nodes V_A, V_B, V_1, and V_2, respectively. Since the drains and the sources of S_{4A} and S_{4B} are at the threshold point of A_{op} during the sample mode, the charges injected from their turn-off transients are signal-independent, and the resulting error are common-mode if S_{4A} and S_{4B} are well matched. However, there exists a signal-dependent difference between the charges injected from S_{1A} and S_{1B}; this is due to the fact that V_A is signal-dependent, while V_B is signal-independent. Through the DCFA circuit, the difference between ΔV_A and ΔV_B caused by the injected charges from S_{1A} and S_{1B} is coupled to the input nodes of the amplifier A_{op} through the capacitors C_1 and C_2. The outputs of A_{op} are coupled to the charge holding nodes V_A and V_B through C_3 and C_4 to form a negative feedback loop. The negative feedback loop attenuates the difference between ΔV_A and ΔV_B.

For simplicity, it is assumed that

1) $C_1 = C_2$, $C_3 = C_4$, $C_A = C_B$, and $C_{p1} = C_{p2}$, where C_{p1} (C_{p2}) is the input capacitance of the amplifier A_{op} at the positive (negative) input.
2) The operational amplifier A_{op} is fully balanced and the common-mode voltage at the outputs is stabilized at $V_{\text{cm-op}}$ through a common-mode feedback, such that $V_{O+} \approx \frac{A_{\text{op}}}{2}(V_{i+} - V_{i-}) + V_{\text{cm-op}}$, and $V_{O-} \approx -\frac{A_{\text{op}}}{2}(V_{i+} - V_{i-}) + V_{\text{cm-op}}$.

Based on these two assumptions, it can be shown that the effective clock feedthrough error voltage at the gate node of N_1 is

$$\Delta V_{g1} = A_{\text{vd}}\left[\frac{Q_A - Q_B}{(1-\gamma)C_1 + (1+\gamma A_{\text{op}})C_3 + C_A}\right] + A_{\text{vcm}}\left[\frac{\frac{Q_A+Q_B}{2}}{(1-\gamma)C_1 + C_3 + C_A} + \Delta V_{s2}\right] \quad (1)$$

where $\gamma = \frac{C_1}{C_1+C_{p1}}$ and $\gamma \approx 1$, if $C_1 \gg C_{p1}$, A_{vd} (A_{vcm}) is the differential (common-mode) voltage gain of the amplifier A_{buf}, Q_A (Q_B) is the charge injected from S_{1A} (S_{1B}), and ΔV_{s2} denotes the common-mode error voltage caused by S_{4A} and S_{4B}.

Equation (1) shows that the effective capacitance for the differential-mode charge injection is $[(1-\gamma)C_1 + (1+\gamma A_{\text{op}})C_3 + C_A]$, where the capacitance C_3 is magnified by the gain factor $(1 + \gamma A_{\text{op}})$ provided by the DCFA circuit. Consequently, the differential charge injection error can be significantly reduced if the ratio $\left(\frac{A_{\text{op}}}{A_{\text{vd}}}\right)$ is sufficiently large. Though the signal-independent common-mode charge injection error is not attenuated by the DCFA circuit, it can be attenuated by the low common-mode gain A_{vcm} of the voltage buffer A_{buf}. As a result, both differential-mode and common-mode clock feedthrough errors are reduced significantly in this circuit. Note that the differential gain A_{vd} must be appropriately designed to trade the reduction of the clock feedthrough errors with the dynamic range. If A_{vd} is too small, the clock feedthrough errors are reduced, but a large voltage swing at the positive input of A_{buf} would be required to track the input current swing in the sample mode. This decreases the dynamic range. To obtain a compromise between the accuracy and the dynamic range, the differential gain A_{vd} is chosen to be 1 while the common-mode gain A_{vcm} is designed to be as low as possible.

The circuit diagram for the amplifier A_{buf} used in Fig. 1 is shown in Fig. 2. Besides the reduction of the clock feedthrough errors, the buffer amplifier A_{buf} also increases the isolation of the charge holding nodes from the output nodes in the hold mode; this reduces the capacitance coupling error caused by the output voltage swing.

Table I shows the simulated signal-dependent clock feedthrough errors of the proposed CSH circuit for input current ranging from -550 μA to 550 μA. (The signal-independent offset is nulled out.) For comparison, the simulated results of conventional CSH circuits [5], with and without the Miller feedback circuitry [18], are also shown. The dimensions of the transistors and the capacitors in these circuits are suitably chosen to have the same settling-time constant in the sample mode. The dimensions of the critical devices for the circuit in Fig. 1 are listed in Table II. From Table I, it can be seen that only a slight reduction of clock

TABLE II.
DEVICE DIMENSIONS OF THE CIRCUIT IN FIG. 1

Device	Dimension
N_1, N_2	(W/L)=(184 um / 3 um)
S_{1A}, S_{1B}, S_{4A}, S_{4B}	NMOS (W/L)=(20 um / 2 um)
C_1, C_2, C_3, C_4	2 pF
Bias Current J	760 uA

feedthrough errors is obtained by applying the Miller feedback [18] to the conventional CSH [5]. The proposed CSH circuit without the DCFA circuit is three time more effective as compared to the conventional CSH circuit. With the DCFA circuit added, the clock feedthrough errors can be further reduced by another factor of twenty.

In the derivation of (1), it is assumed that $C_1 = C_2$, $C_3 = C_4$, $C_A = C_B$, and $C_{p1} = C_{p2}$. It can be shown that the errors caused by the mismatches in these capacitors for the charge injection from S_{1A} and S_{1B} are also attenuated by the gain factor $A_{\rm op}$. For the charges injected from S_{4A} and S_{4B}, detailed analysis shows that the differential error voltages between nodes V_A and V_B caused by the mismatch of capacitors can be approximately expressed as

$$(\Delta V_A - \Delta V_B) \approx \left(\frac{Q_{4B} - Q_{4A}}{C_{m12}}\right) + \left(\frac{\Delta C_{12}}{C_{m12}}\right)\left(\frac{\frac{Q_{4A}+Q_{4B}}{2}}{C_{m12}}\right) \tag{2}$$

where $C_1 = C_{m12} + \frac{\Delta C_{12}}{2}$, and $C_2 = C_{m12} - \frac{\Delta C_{12}}{2}$. Q_{4A} (Q_{4B}) is the charge injection from S_{4A} (S_{4B}). In (2), the first term is due to the charge injection difference between S_{4A} and S_{4B}. Since the sources and the drains of S_{4A} and S_{4B} are at the threshold point of $A_{\rm op}$ during the sample mode, the charge difference between Q_{4A} and Q_{4B} is small. The second term comes from the common-mode charge injection which is attenuated by the mismatch factor $\frac{\Delta C_{12}}{C_{m12}}$. Note that the mismatch of C_3 and C_4 results in negligible errors for the charges injected from S_{4A} and S_{4B}, since C_3 (C_4) simply functions as a dc blocking capacitor between the node V_A (V_B) and the negative (positive) output of $A_{\rm op}$.

The simulated results of the circuit in Fig. 1 with 10% device mismatches are also shown in Table I. From the simulated results and the discussions above, it can be shown that the clock feedthrough currents are significantly reduced by the DCFA circuit even in the case of large mismatches of capacitors and switches.

III. FULLY DIFFERENTIAL VERSION

In high precision applications, fully differential configurations are more attractive because it provides a 6 dB increase for the dynamic range, and a higher immunity against power line noises and clock feedthrough errors. A fully differential CSH circuit derived directly from the circuit in Fig. 1 is shown in Fig. 3. The circuit depicted in the lower half of this figure consisting of an operational voltage amplifier, four capacitors, and two switches is the DCFA circuit. The circuits in the upper half are the core circuits to sample/hold the input currents. The voltage buffer amplifier $A_{\rm buf}$ required herein is constructed by the five transistors P_3, P_{4f}, P_{4r}, N_{3f}, and N_{3r}. During the sample mode (ϕ_1, ϕ_3 high and ϕ_2 low), the common gate node of P_{1f} and P_{1r} is connected to the common source node of P_{4f} and P_{4r} through the switch S_5 to form a common-mode feedback loop. If the common-mode input is zero, the voltage at the common source node of P_{4f} and P_{4r} ideally remains at the quiescent value, and thus the currents of P_{1f} and P_{1r} only offer the dc bias currents J. If non-zero $i_{\rm cm}$ is present at the inputs, this common-mode component is detected at the common source node of P_{4f} and P_{4r}, which adjusts the currents of P_{1f} and P_{1r} to be $(J - i_{\rm cm})$. The common-mode component $i_{\rm cm}$ of the inputs is thus taken away from the inputs by the upper PMOS branches consisting of (P_{1f}, P_{2f}) on the left and (P_{1r}, P_{2r}) on the right. The differential part $\pm i_d$ of the input currents are detected at the gate-drain shorted nodes of N_{3r} and N_{3f}, which adjust the currents of N_{1f} and N_{1r} to be $(J + i_d)$ and $(J - i_d)$, respectively.

When the circuit is switched to the hold mode (ϕ_1, ϕ_3 low and ϕ_2 high), the common gate node of P_{1f} and P_{1r} is connected through the switch S_6 to a fixed-bias voltage $V_{\rm bcm}$, which can be designed to make the currents of P_{1f} and P_{1r} equal to the bias current J. Consequently, the common-mode part of the input is eliminated in the hold mode. The differential parts of the input currents are held and fed to the outputs from the transistors (N_{1f}, N_{2f}) and (N_{1r}, N_{2r}), respectively.

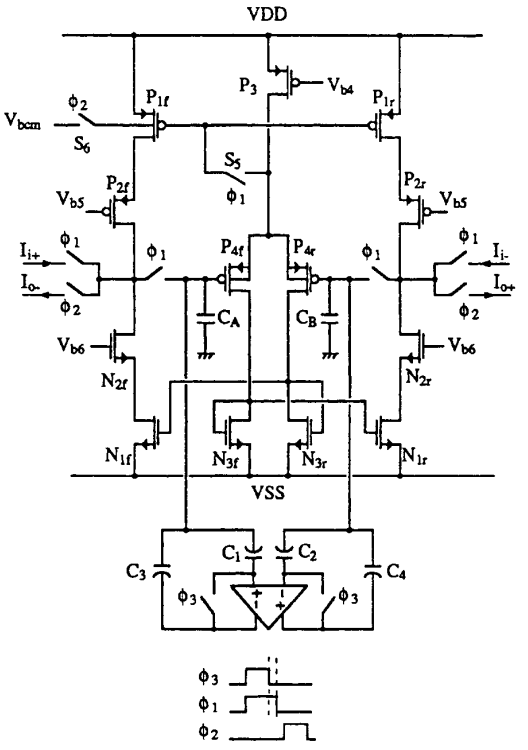

Fig. 3. The proposed fully differential dynamic-mirror CSH circuit.

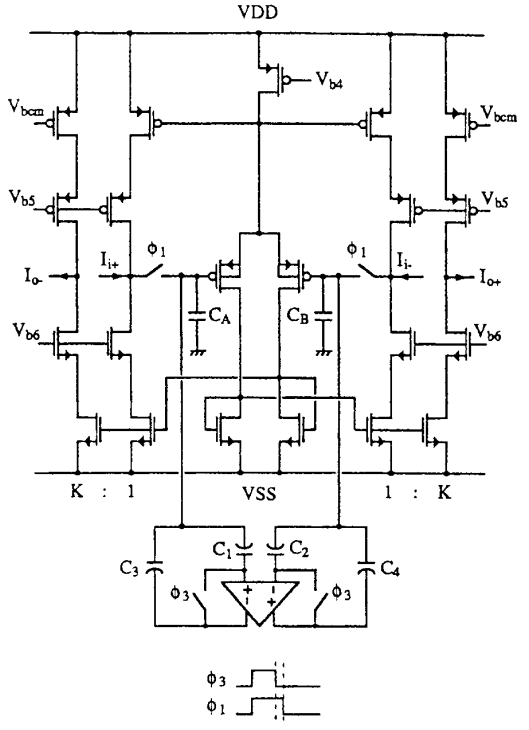

Fig. 4. The proposed fully differential CSH circuit with scaled/multiple outputs.

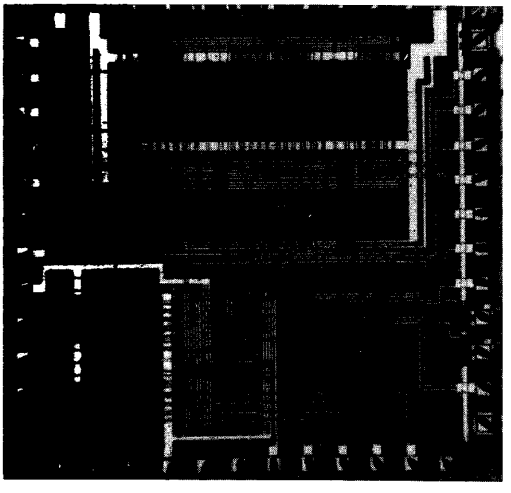

Fig. 5. Proposed fully differential CSH circuit.

In some applications, multiple outputs are required simultaneously to serve as feedback, to drive multiple loads, or to get a scaled output. The circuit of Fig. 3 can be modified to meet this requirement by adding additional current mirrors. Fig. 4 shows the resulting circuit. In this circuit, the mismatch of mirror transistors becomes another potential error source and therefore special care is required for the layout of these mirror transistors.

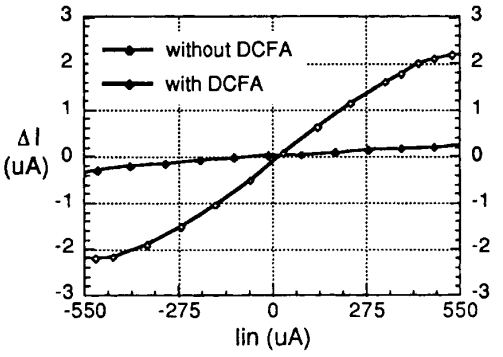

Fig. 6. Measured signal-dependent hold pedestal errors versus input current level.

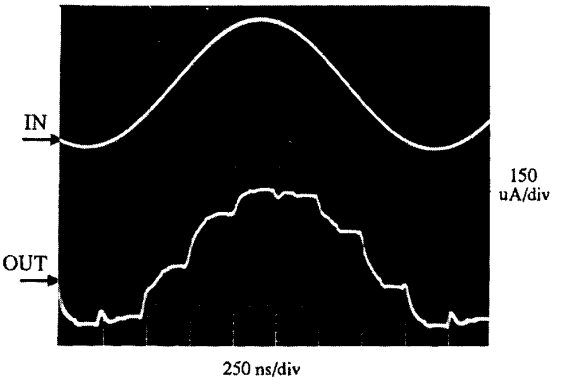

Fig. 7. Measured waveforms of the CSH circuit to sample/hold a 500 kHz, 900 μA $_{p-p}$sinusoid input at 4 MHz clock rate.

IV. Experimental Results

The fully differential CSH circuit of Fig. 4 was designed and fabricated in 1.2-μm CMOS N-well technology. A photograph of the experimental chip is shown in Fig. 5. The active chip area and power consumption of the fabricated fully-differential CSH circuit is 0.64 mm^2 and 20 mW, respectively. The switches are NMOS devices with (W/L) =(20 μm/2 μm). Dummy devices are not added to these NMOS switches to facilitate the measurement of the clock feedthrough errors. The external input clock is buffered by a chain of inverters to achieve the internal clock transition time of 1 ns. For comparison, the circuit of Fig. 4 with the DCFA removed and appropriate capacitors added was also fabricated in another test chip.

Fig. 6 plots the measured signal-dependent hold pedestal error currents as a function of the dc input current level. Two curves for the CSH, with and without the DCFA circuitry, are shown. Comparing these two curves, it is shown that the DCFA circuitry can reduce the signal-dependent clock feedthrough errors by a factor of 5.

The waveform for the CSH to sample/hold a 500 kHz sinusoidal input with peak-to-peak amplitude of 900 μA at 4 MHz clock rate is shown in Fig. 7. The acquisition time for a 900 μA step transition to 0.1% accuracy is 150 ns. The

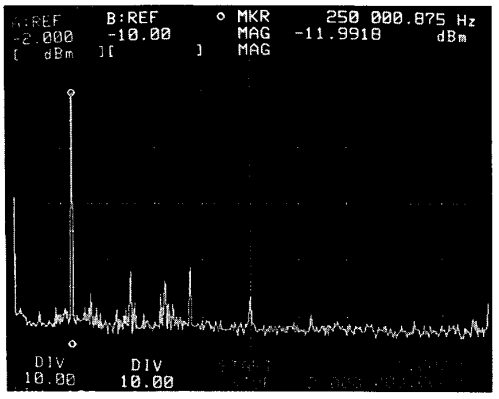

Fig. 8. Output spectrum of the CSH circuit for the 250 kHz, 410 μA $_{p-p}$ sinusoid input at 4 MHz clock rate.

TABLE III.
MEASURED PERFORMANCE OF THE CSH CIRCUIT

Acquisition time (0.1% accuracy)	150 ns
Gain error (- 550 uA ~ 550 uA)	- 57 dB
Common-mode input range	- 450 uA ~ 450 uA
Hold pedestal (- 550 uA ~ 550 uA)	less than +/- 0.4 uA
THD (f_{ck} = 4 MHz) (250 kHz, 410 uA_{p-p})	- 60 dB
SNR (f_{ck} = 4 MHz) (0.1 % THD, 2 MHz B.W.)	79 dB
CMRR (low frequecncy)	54 dB
Input resistance	750 Ω
Output resistance	1M Ω
Power consumption*	20 mW
Technology	1.2-um CMOS
Power supply	5V
Active area*	0.64 mm^2

* The power consumption and chip area are measured for a CSH circuit of unity gain.

output spectrum of the CSH circuit clocked at 4 MHz for the input at 250 kHz with peak-to-peak amplitude of 410 μA is shown in Fig. 8. Note that the spectrum is observed from a single ended output. When the signal frequency is below 250 kHz, the total harmonic distortion is smaller than −60 dB. The corresponding signal-to-noise ratio is 79 dB. As the signal frequency is increased to 500 kHz, the total harmonic distortion is increased to −49 dB. The performance of the experimental CSH circuit is summarized in Table III.

V. CONCLUSION

New techniques for the design of CSH circuits are proposed to improve the performance limitations in conventional circuits. Clock feedthrough errors are reduced using a new differential clock feedthrough attenuation circuits without degrading the linearity and operating speed. Both simulation and experimental results have verified the capability of the DCFA circuit to get about 5 times of improvement in reducing the signal-dependent clock feedthrough errors. The proposed CSH circuits also show a high immunity against the C_{gd} capacitive coupling errors from the outputs.

ACKNOWLEDGMENT

The United Microelectronics Corporation (UMC), Taiwan, R.O.C., is greatly acknowledged for the fabrication of the experimental chip. The authors also would like to thank the reviewers for their valuable comments and suggestions on the manuscript.

REFERENCES

[1] C. Toumazou, F. J. Lidgey, and D. G. Haigh, Eds., *Analouge IC Design: The Current-Mode Approach.* London: Peter Peregrinus, 1990.
[2] R. H. Zele and D. J. Allstot, "Low-voltage fully-differential cmos switched-current filters," in *Proc. 1993 IEEE Custom Integr. Circuits Conf.*.
[3] P. Real, D. H. Robertson, C. W. Mangelsdorf, and T. L. Tewksbury, "A wide-band 10-b 20-ms/s pipelined adc using current-mode signals," *IEEE J. Solid-State Circuits*, vol. 26, pp. 1103–1108, Aug. 1991.
[4] Z. Wang, "Current-mode integrated circuits for analog computation and signal processing: a tutorial," *Anal. Integr. Circuits Signal Processing J.*, vol. 1, no. 1, pp. 287–295, 1991.
[5] J. B. Hughes, N. C. Bird, and I. C. Macbeth, "Switched currents–a new technique for analogue sampled-data signal processing," in *Proc. IEEE Int. Symp. Circuit Syst.*, 1989, pp. 1584–1587.
[6] S. S. Lee, R. H. Zeles, D. J. Allstot, and G. Liang, "CMOS continuous-time current-mode filters for high-frequency applications," *IEEE J. Solid-State Circuits*, vol. 28, pp. 323–329, Mar. 1993.
[7] N. Bluzer and A. S. Jenser, "Current readout of infrared detectors," *Opt. Eng.*, vol. 26, No. 3, pp. 241–248, Mar. 1987.
[8] P. Aubert, H. J. Oguey, and R. Vulleumier, "Monolithic optical position encoder with on-chip photodiodes," *IEEE J. Solid-State Circuits*, vol. 23, no. 2, pp. 465–473, Apr. 1988.
[9] J. B. Hughes and K. W. Moulding, "Switched-current signal processing for video frequencies and beyond," *IEEE J. Solid-State Circuits*, vol. 28, no. 3, pp. 314–322, Mar. 1993.
[10] T. S. Fiez, G. Liang, and D. J. Allstot, "Switched-current circuit design issues," *IEEE J. Solid-State Circuits*, vol. 26, no. 3, pp. 192–202, Mar. 1991.
[11] R. H. Zele, D. J. Allstot, and T. S. Fiez, "Fully-balanced CMOS current-mode circuits," *IEEE J. Solid-State Circuits*, vol. 28, no. 5, pp. 569–575, May 1993.
[12] D. G. Nairn and C. A. T. Salama, "A ratio-independent algorithmic analog-to-digital conerter combining current mode and dynamic techniques," *IEEE Trans. Circuit Syst.*, vol. 37, no. 3, pp. 319–325, Mar. 1990.
[13] S. J. Daubert and D. Vallancourt, "A transistor-only current-mode ΣΔ modulator," *IEEE J. Solid-State Ciruits*, vol. 27, No. 5, pp. 821–830, May 1992.
[14] H. C. Yang, T. S. Fiez, and D. J. Allstot, "Current-feedthrough effects and cancellation techniques in switched-current circuits," in *Proc. IEEE Int. Symp. Circuit Syst.*, 1990, pp. 3186–3188.
[15] M. Song, Y. Lee, and W. Kim, "A clock feedthrough reduction circuit for switched-current systems," *IEEE J. Solid-State Circuits*, vol. 28, no. 2, pp. 133–137, Feb. 1993.
[16] C. Toumazou, J. B. Hughes, and N. C. Battersby, Eds., *Switched Currents: an Analouge Technique for Digital Technology.* London: Peter Peregrinus, 1993, pp. 315–316, ch. 12.
[17] G. Wegmann and E. A. Vittoz, "Analysis and Improvements of accurate dynamic current mirrors," *IEEE J. Solid-State Circuits*, vol. 25, no. 3, pp. 699–706, June 1990.
[18] P. J. Lim and B. A. Wooley, "A high-speed sample-and-hold technique using a Miller hold capacitace," *IEEE J. Solid-State Circuits*, vol. 26, no. 4, pp. 643–651, Apr. 1991.