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Improved Electrical Performance of NILC Poly-Si TFTs Manufactured Using H_2SO_4 and HCl Solution

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In this study, we fabricated a NILC surface on a SiO_2-coated silicon wafer, and then used HCl solution and $H_2SO_4 + H_2O_2$ solution to do surface treatment. The treatment could reduce Ni or $NiSi_2$ that was trapped at the surface of silicon and therefore the electrical characteristics of these devices were improved.

INTRODUCTION

Low-temperature polycrystalline silicon (poly-Si) thin-film transistors (TFTs) have attracted considerable interest for their application in active-matrix liquid crystal displays (AMLCDs) (1,2). Intensive studies on reducing the crystallization time and temperature of amorphous silicon (α-Si) have been carried out. Nickel-induced lateral crystallization (NILC) is one of these efforts (3,4). Unfortunately, poly-Si/oxide interfaces and grain boundaries trap Ni and $NiSi_2$ (Ni-related defects), which degrades its electric performance (5,6). Several metal gettering methods have been employed to reduce the amount of undesired metallic impurities in Si. However these gettering methods are complicated and require high process temperatures. In this study, we used a simple and low thermal budget chemical treatment to reduce Ni residuals.

EXPERIMENTAL

The process of poly-Si films began with four-inch wafer where a 100nm thick undoped amorphous silicon (α-Si) layer was deposited on a 500nm thick oxide coated silicon wafer by LPCVD system. The 50nm TEOS oxide was deposited by PECVD and patterned to desired Ni lines, and a 5nm thick Ni was deposited on the α-Si by E-gun. After annealed at 540°C for 36 hours, the unreacted Ni metal and TEOS oxide on these samples were removed by chemical etching. Then, these samples were divided three part; one was soaked in $H_2SO_4 + H_2O_2$ (3:1) solution at 80°C for 20 minute (H_2SO_4-NILC TFTs), another was in HCl solution at 25°C for 2 hours (HCl-NILC TFTs) and the other wasn't done anything (con-NILC TFTs). Reactive ion etching (RIE) was employed to form poly-Si islands. After the RCA clean, a 100nm TEOS oxide and a 100nm poly-Si were deposited by PECVD and LPCVD respectively and then defined gate. The 40KeV P ions were implanted at a dose of 5E15 cm^{-2} to form the source / drain and gate region, and then performed at 600°C for 24 hours. Followed by a deposition of the passivation layer and definition of contact holes, a 500nm thick Al electrode was deposited and patterned. Finally, these finished devices were sintered at 400°C for 30 minutes and treated with NH_3 plasma. The schematic diagram of the key process is illustrated in Figure 1.

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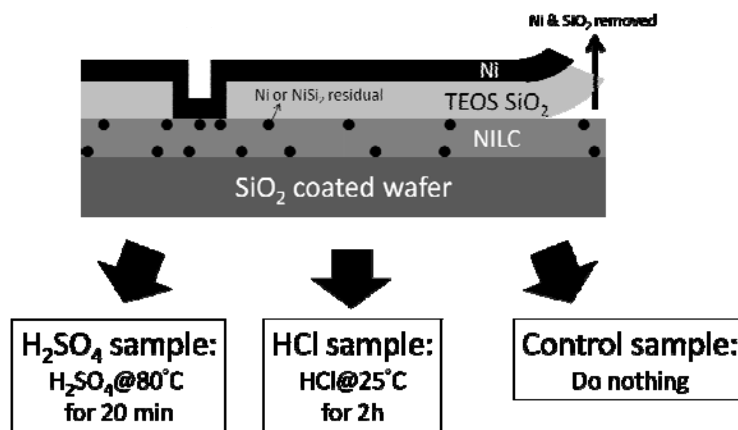

Figure 1. Schematic diagram of the key process by H_2SO_4

RESULTS AND DISCUSSION

Figure 2. shows the I_{DS}-V_{GS} transfer characteristics and field-effect mobility (μ_{FE}) of H_2SO_4-NILC TFTs, HCl-NILC TFTs and control-NILC TFTs. It was found that H_2SO_4-NILC TFTs and HCl-NILC TFTs have superior electrical characteristics such as high field-effect mobility, low threshold voltage, low subthreshold slope and high on/off current ratio, especially HCl-NILC TFTs. As showed in **TABLE I.**, the device parameters were extracted at W / L = 10μm / 10μm. The threshold voltage (V_{TH}) was defined as the gate voltage required to achieve a normalized drain current of I_{DS} = (W / L) × 100 nA at V_{DS} = 5 V. The subthreshold slope (S.S.) and the on/off current ratio were measured at V_{DS} = 5 V, while the μ_{FE} was measured at V_{DS} = 0.1 V. Compared to con-NILC TFTs, the μ_{FE} of HCl-NILC TFTs is 172% increased and on/off current ratio is 387% improved.

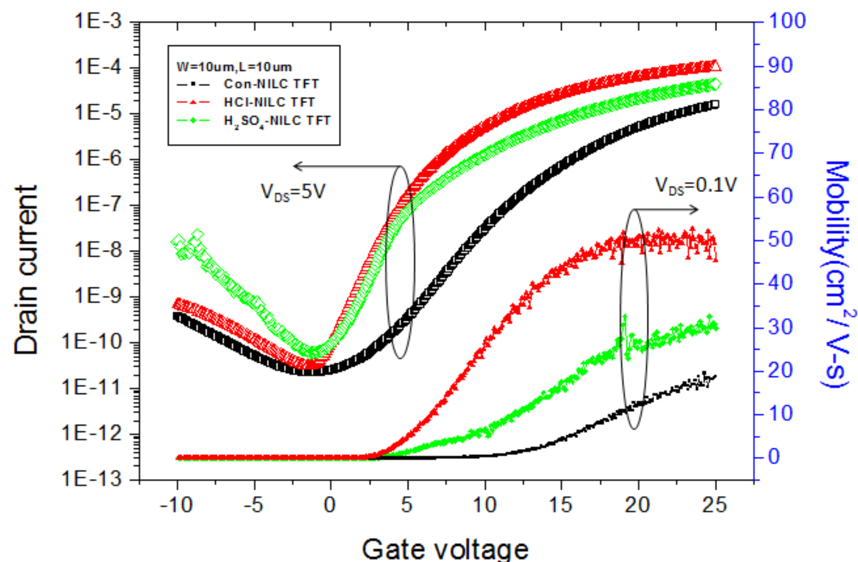

Figure 2. Typical I_{DS}-V_{GS} transfer characteristics and field-effect mobility of H_2SO_4-TFTs, HCl-TFTs and control-TFTs.

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TABLE I. Average values of the field-effect mobility, threshold voltage, subthreshold slope, on/off current ratio of TFTs.

W/L=10um/10um	Con-NILC TFT	HCl-NILC TFT	H_2SO_4-NILC TFT
Mobility μ_{FE} (cm^2/Vs)	19.43	52.78	32.48
Threshold Voltage V_{TH} (V)	12.56	4.20	5.66
Subthreshold Slope S.S. (V/dec)	2.08	1.27	0.52
On/Off Current Ratio (10^5)	7.13	34.77	7.61

In Figure 3., we use Levinson's and Proano's method to calculate the trap charge densities (7,8), and the results showed that the Ni trap densities of HCl-NILC TFT and H_2SO_4-NILC TFT are 3.61×10^{12} cm^{-2} and 5.05×10^{12} cm^{-2} respectively. These values were lower than the control sample which was 7.28×10^{12} cm^{-2}. It indicated that the Ni or $NiSi_2$ residuals at the surface of NILC were reduced effectively after HCl or H_2SO_4 treatment. That could be the reason for the electrical characteristics' enhancement.

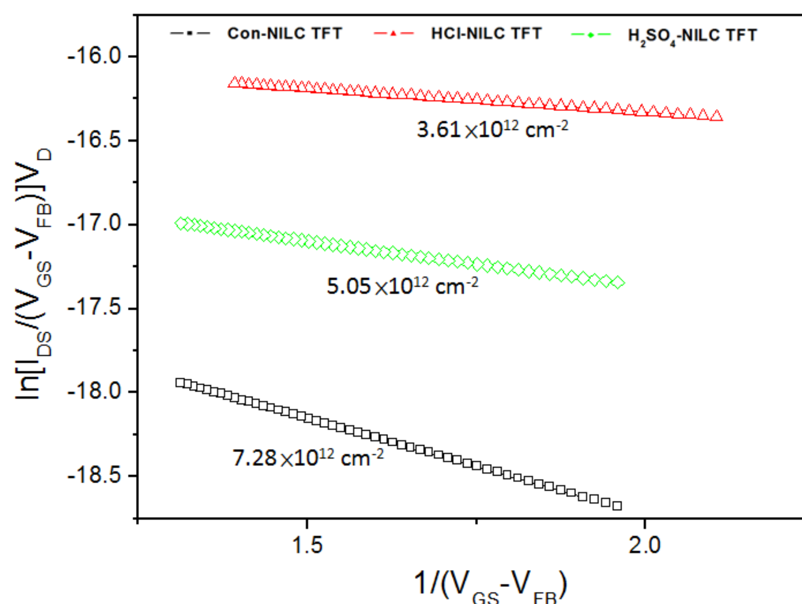

Figure 3. The trap charge densities of all samples. They can be estimated from the slope of the linear segment of $\ln[I_{DS}/(V_{GS}-V_{FB})]$ vs. $1/(V_{GS}-V_{FB})^2$.

Conclusion

An investigation of poly-Si TFTs using HCl and H_2SO_4 solution treatment had led to the development of a simple and effective process to improve the TFT electrical properties. It was found that HCl and H_2SO_4 solution treatment TFT exhibited higher μ_{FE}, superior S.S., lower V_{TH}, higher on / off current ratio and lower Ni trap state density as compared with typical NILC TFTs. That was because after chemical solution treatment, the Ni or $NiSi_2$ residuals at the surface of Si were reduced. That could be the reason for electrical properties enhancement.

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