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Improved Performance of NILC Poly-Si Nanowire TFTs by Using Ni-Gettering

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Nickel contamination inside nickel-metal induced lateral crystallization polycrystalline silicon is an issue to fabricate high performance nanowire thin film transistors. The phosphorous-doped α-Si/chem-SiO_2 films were employed as Ni-gettering layers to investigate effect of Ni residues on the performance of NILC poly-Si NW TFTs. It was found that the performance of NW TFTs was greatly improved after Ni-gettering process.

Introduction

Low-temperature polycrystalline silicon (poly-Si) thin-film transistors (TFTs) have attracted considerable interest for their application in active-matrix liquid crystal displays (AMLCDs) on cheap glass substrate (1). Recently, high performance poly-Si nanowire (NW) TFTs have been fabricated by nickel-metal induced lateral crystallization (NILC) (2-3). Since NILC grain could be formed parallel to the channel direction, it becomes feasible to form Si NWs with nearly monocrystalline structures (4). Unfortunately, poly-Si/oxide interfaces and poly-Si grain boundaries trap Ni and $NiSi_2$ precipitates, thus increasing leakage current (5-8) and shifting the threshold voltage (9). Since the poly-Si/oxide interfaces/volume ratio of NW TFTs was much higher than that of tradition NILC TFTs, effect of Ni residues on the performance of NILC NW TFTs should be investigated. In this study, phosphorous-doped α-Si/chem-SiO_2 films were used to investigate effect of Ni residues on the performance of NILC NW TFTs.

Experimental

Two kinds of NWs were investigated in this study. One was designated as "NILC NW" which was a poly-Si NW fabricated with traditional NILC methods, and another was "GETR NW" which utilized the same traditional NILC method with an additional Ni-gettering process. An approach for making NILC NW channels similar to Ref. (2) and (10) was followed. The detailed procedures were basically identical to those described in the Ref. (10), like gate dielectric deposition and source/drain formation. In this study, the major difference was NILC process performed before NW channel was defined. NILC length was about 17 μm after lateral crystallization at 540°C for 24 h.

As for GETR NW, an additional Ni-gettering process (11) was carried out to reduce the Ni concentration in NILC film. The gettering structure (phosphorous-doped α-Si/chem-SiO_2) is shown in Fig. 1(a). After gettering at 550°C for 12 h, phosphorous-

doped α-Si and chem-SiO_2 layers were removed using 5% tetra-methyl ammonium hydroxide (TMAH) and 1% DHF solution, respectively. For comparison, NILC films were also subjected to an extended heat treatment as Ni-gettering condition. These two poly-Si films were then subjected to an anisotropic etching to form poly-Si spacers (NWs) in a self-aligned manner. The device structure is illustrated in Fig. 1(b).

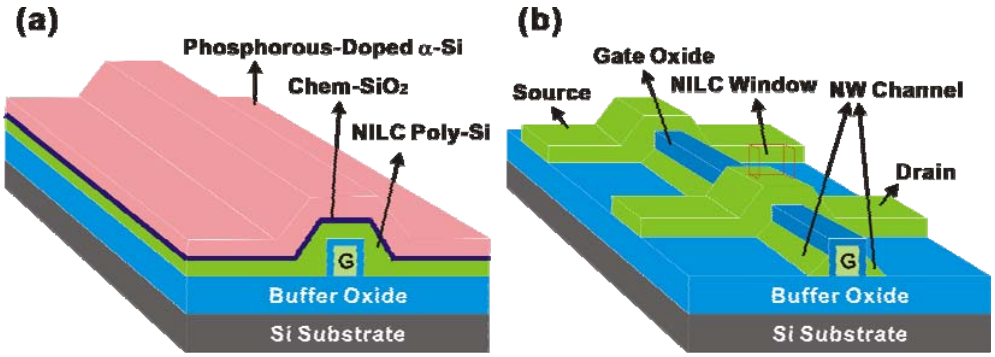

Fig. 1 (a) Ni-gettering structure fabricated with phosphorous-doped α-Si capped on the chem-SiO_2. (b) The schematic of the proposed poly-Si NW TFT structure.

Results and Discussion

The TFT devices with a couple of NW channels have a nominal channel (L) of 0.8 μm and an effective channel width (W) of 140 nm (2 × W_{NW}). Typical I_D-V_G transfer characteristics of NW TFTs at V_D = 0.5 and 3 V are compared in Fig. 2. The measured and extracted key device parameters are summarized in Table I. The threshold voltage (V_{TH}) is defined at a normalized drain current of I_D = (W/L) × 100 nA at V_D = 0.5 V. The subthreshold swing (S.S.) is extracted at V_D = 0.5 V. The field-effect mobility (μ_{FE}) is extracted from the maximum value of transconductance at V_D = 0.5 V. The leakage current (I_{OFF}) is defined as the minimum drain current along the gate voltage at V_D = 3 V.

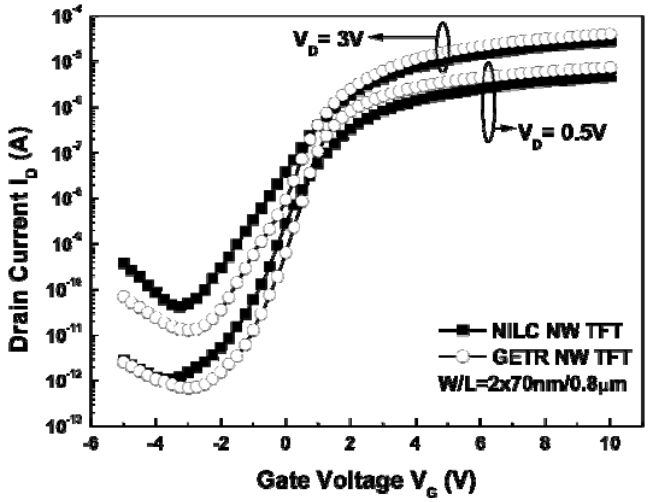

Fig.2 I_D-V_G transfer characteristics of NILC poly-Si NW TFTs with and without Ni-gettering.

As shown in TABLE I, ten NILC and GETR NW TFTs were measured. The performance of NILC NW TFTs was improved after Ni-gettering process. GETR NW TFTs had lower I_{OFF}, higher I_{ON}/I_{OFF} ratio, and higher μ_{FE} compared with NILC NW TFTs. This improvement indicates the trap state density (N_{trap}) was effectively reduced using phosphorous-doped α-Si gettering processes. The trap state density of the TFTs was extracted using Levinson and Proano's method (12). The trap density of GETR NW TFTs is 2.52×10^{12} cm^{-2}, which is less than that of NILC NW TFTs (3.95×10^{12} cm^{-2}). Since GETR grains (boundaries) were similar to NILC grains, the reduction in N_{trap} values implies that those Ni-related defects have been reduced using phosphorous-doped α-Si/chem-SiO_2 gettering structure (11).

TABLE I. Device characteristics for ten NILC NW TFTs with and without Ni-gettering.

Parameters (W/L=2x70nm/0.8μm)	**GETR NW TFTs**	**NILC NW TFTs**
I_{OFF} (pA)	13.0 ± 5.4	81.9 ± 95.7
I_{ON}/I_{OFF} ratio (10^6)	3.2 ± 1.0	1.4 ± 1.2
μ_{FE} (cm^2/V-s)	140.7 ± 38.2	117.3 ± 17.8
S.S. (mV/dec)	418 ± 63	395 ± 66
V_{TH} (V)	0.35 ± 0.22	0.19 ± 0.40

Besides, as shown in TABLE I, the V_{TH} of the NILC NW TFT is 0.19 V, which is less than that of GETR NW TFT (0.35 V). This is because Ni residues could cause a high density of positive charge at the oxide/NILC poly-Si interface (13). The negative shift of V_{TH} of NILC NW TFT was due to the presence of these positive charges and nickel-related donor-like defects.

Summary

In this study, high performance NILC NW poly-Si TFTs with a couple of 70-nm NW channels were fabricated, and then improved by Ni-gettering process. The phosphorous-doped α-Si/chem-SiO_2 films were employed as Ni-gettering layers to reduce Ni residues within NILC poly-Si film. After Ni-gettering process, the performance of NILC NW TFTs was improved. GETR NW TFTs had lower I_{OFF}, higher I_{ON}/I_{OFF} ratio, and higher μ_{FE} compared with NILC NW TFTs.

Acknowledgments

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