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High Performance and Reliability of Poly-Si Thin-Film Transistors Using Nickel Drive-In Induced Laterally Crystallization

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In this study, polycrystalline silicon thin film transistors using drive-in Ni induced lateral crystallization (DILC) was proposed. In DILC, F^+ implantation was used to drive Ni in the α-Si layer. To reduce the Ni contamination, the remained Ni film was then removed, and subsequently annealed at 590°C. It was found DILC TFTs exhibit high field-effect mobility, low threshold voltage, low subthreshold slope, high on-state current, lower trap state density, smaller standard deviations, and low off-state leakage current compared with conventional Ni-metal-induced lateral crystallization (MILC) TFTs.

Introduction

Low-temperature polycrystalline silicon (LTPS) thin-film transistors (TFTs) have attracted considerable interest for their application in active-matrix organic emitting diode displays (AMOLED). Metal-induced lateral crystallization of Silicon (MILC) is one of these methods to fabricate LTPS film. In MILC, the crystallization of poly-Si was preceded by migration of nickel silicides through α-Si, and resulting in needlelike Si grains. However, there were still some regions between poly-Si grains remained un-crystallized. These defects might degrade the transfer characteristics of TFT devices.

In this letter, a novel fabrication process has been developed to reduce the Ni concentration and minimizes the trap-state density of polycrystalline silicon (poly-Si) TFTs using nickel drive-in induced laterally crystallization (DILC). The DILC poly-Si was prepared by collision between fluorine ion (F+) implantation with nickel (Ni) through the designed pattern into amorphous-Si (α-Si) layer after annealing at 590 ℃ for 3 hr.

Experimental

A 120-nm-thick undoped amorphous silicon (α-Si) layer was deposited onto a 500-nm-thick oxide-coated silicon wafer by low pressure chemical vapor deposition (LPCVD) system. A 65-nm-thick cap-oxide was deposited and patterned to form 20-μm-wide lines, and a 20-Å-thick Ni film was then deposited. Samples were subjected to F+ implantation to drive Ni in the α-Si layer, as shown in Fig.1. For the α-Si layer under the Ni line, the projection range was set at the middle of the α-Si layer. At the same time, for the α-Si layer under the oxide layer, it was located at the cap-oxide/α-Si interface. The dosage of F+ ranged from 2×1012 to 2×1015 cm-2. The ion-accelerating energy was 35 KeV. The preparation of DILC poly-Si began with four-inch Si wafer. To reduce the Ni contamination/concentration, the remained Ni film and cap-oxide were then removed by chemical etching, and subsequently annealed at 590°C for 3 h to form the DILC poly-Si. For the purpose of comparison, conventional MILC was prepared (1). It is worthy to note

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that this DILC processes do not need any additional thermal annealing step and are compatible with MILC TFT processes.

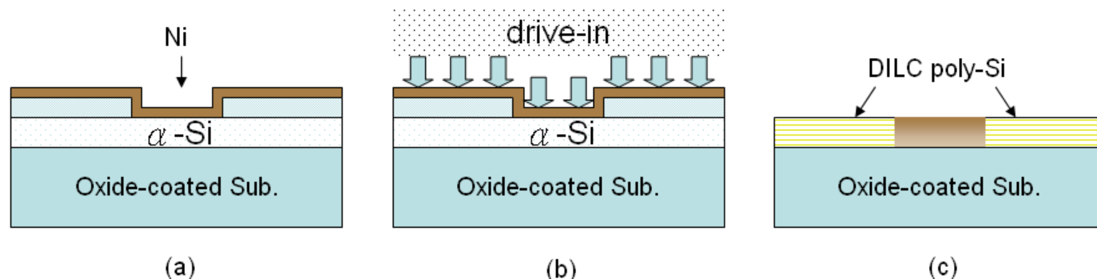

Figure 1. Schematic illustration of F+ implantation process to drive Ni in the α-Si layer.

Results and Discussion

The I_D-V_G transfer characteristics are shown in Fig. 2 and the key parameters are summarized in the Table I. It was found that DILC TFTs have superior electrical characteristics, such as high field-effect mobility, low threshold voltage, low subthreshold slope, high on-state current and low off-state leakage current. This indicates that the trap-state density (Nt) in DILC poly-Si was effectively reduced. These results are similar to our previous study on improving the electrical properties of MILC TFTs using F+ implantation (2), in which MILC poly-Si was subjected to F+ implantation. It was also found F atoms can improve performance and reliability of MILC TFTs. Unfortunately, the minimum off currents were nearly unchanged due to the high Ni contamination. In contrast to this study, the Ni concentration inside the poly-Si was controlled/ limited by F+ implantation dosage. The Ni concentration inside the DILC poly-Si was less than that in MILC. As a result, the minimum off current of DILC was less than that of MILC TFT, as shown in Fig. 2.

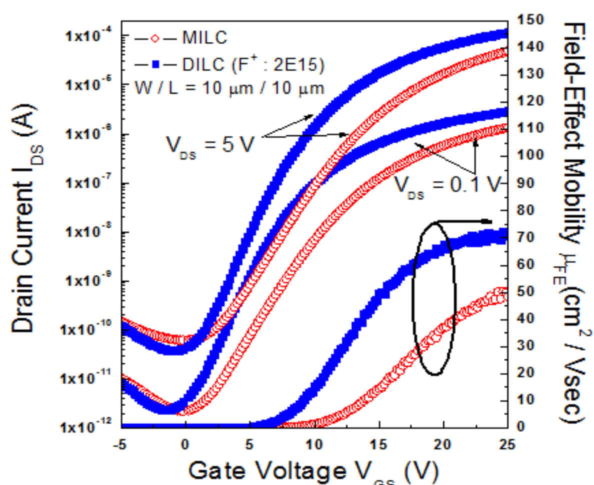

Figure 2. I_D-V_G characteristics of MILC and DILC poly-Si TFTs, respectively.

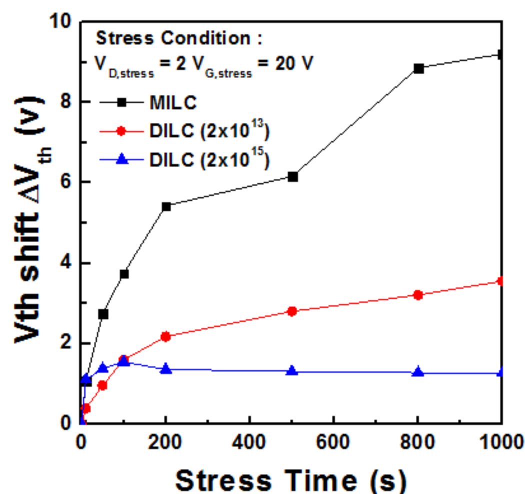

Figure 3. The threshold shift versus stress time for the MILC and DILC poly-Si TFTs.

The other important issue of poly-Si TFTs is their reliability, which was examined under hot-carrier stress. As shown in Fig. 3, the Vth shift of DILC TFTs is greatly

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improved. This is because weaker Si-H and Si-Si bonds were replaced by stronger Si-F bonds, which could not be broken under hot-carrier stress (3, 4), thus leading to improved electrical reliability.

Table I. Device characteristics for MILC and DILC poly-Si TFTs.

	MILC	DILC
Mobility μ_{FE} (cm^2 / Vs)	50.3	72.3
Threshold Voltage V_{TH}(V)	10.49	6.83
Subthreshold Slope S.S (V/dec.)	2.49	1.64
On / Off ratio	7.89×10^5	3.03×10^6

Summary

Significant improvements on the DILC poly-Si TFT devices performance, including higher field-effect mobility, superior subthreshold slope, lower threshold voltage, higher ON/OFF current ratio, lower trap-state density (Nt) and device reliability.

Acknowledgments

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