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Flow Rate's Influence on Low Temperature Silicon Oxide Deposited by Atmospheric Pressure Plasma Jet for Organic Thin Film Transistor Application

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Low temperature processes and high quality gate insulator are very important for organic thin film transistors (OTFTs). We utilized atmospheric pressure plasma jet (APPJ) to deposit silicon oxide as gate insulator of OTFTs at low temperature. We found carrier gas's flow rate would influence the deposition mechanism which lead to influence surface roughness and film quality. Leakage current density of our proposed silicon oxide was about 2.53E-8 A/cm^2 at 0.5 MV/cm. Our proposed OTFTs shows a low subthreshold swing of only 700 mV/dec., a low threshold voltage of -0.8 V, a low operation voltage of -2 V. The low-voltage OTFTs would reduce the power consummation of flexible display.

Introduction

Organic thin film transistors attracted many researchers and companies to investigate and develop due to their future applications mainly consist of flexible display and flexible electronics. Flexible displays are considered as the revolutionary product because it could be applied for e-paper, e-book, and large area screen which would decrease the use of woods, keep environment, and make our life colorful (1-4). On the other hand, flexible electronics, including ratio frequency identification smart card (RFID) and sensors such as pressure sensor, gas sensor, bio-sensor, and electronic artificial skin (5-6). In recent years, although the performance of OTFTs have great improvement, there are still some issues influencing the development of OTFTs. These issues of OTFTs mainly include low mobility, stability, low temperature and low cost processes and high operation voltage. The mobility of organic thin film transistors is only about 0.001~10 cm^2/V-s, much lower than silicon-base MOSFET and polysilicon TFT. The mobility of OTFTs is dominated by organic material and ordering of organic material (7-8). On the other hand, stability of organic semiconductor material is a serious problem. Electrical characteristics of OTFTs would be degraded by oxygen, moisture, and organic solvent and so on (9-10). Some researchers believed that oxygen would diffuse into active layer and formed impurities in the organic semiconductor layer but these studies resulting from environment influence are not very clear. These environment factors may lead to the degradations of on current, threshold voltage shift, and subthreshold swing. However, another pending problem of OTFTs is high operation voltage (11-13). The high operation voltage would result in high active power consumption, not suitable for the low-power protable electronics. Active power consumption is on current multiplied by operation voltage. However, we could not decrease the on current because higher on current could increase operation speed to overcome RC time delay. Therefore, decreasing operation voltage is urgent for OTFTs. In order to keep the magnitude of on current and decrease operation voltage, increasing the capacitance per unit area is the one of the ways to obtain

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the goal. Capacitance is positive proportional to dielectric constant and negative proportional to thickness of insulator. Therefore, many studies used high-k material or thinner insulator as the gate insulator to decrease the operational voltage (14-15). Gate insulator materials mainly consist of polymer, metal oxide, and nanocomposite. Polymer is suitable for low cost processes such as spin, inject, and print. However, the drawbacks of polymer include lower dielectric constant, longer baking time, and more holes pin-holes. Metal oxide materials usually have high dielectric constant such as HfO_2, Ta_2O_5, TiO_2, Al_2O_3, AlN, Si_3N_4 (14-19) and so on but these material often fabricated by CVD or PVD which is high cost and low throughput processes for flexible electronics.
In our work, we focus on developing and investigating low temperature and low cost processes to fabricate high quality silicon oxide as a gate insulator for OTFTs. Silicon dioxide is a kind of very cheap and rich resource in the world and used as main gate insulator for MOSFET. Band gap of silicon dioxide is about 9 eV which is good to be used as a gate insulator. In addition, good stability and reliability of silicon oxide were also proposed in many researches. The highest process temperature of OTFTs usually happened in gate insulator. So decreasing the processes temperature of gate insulator is very important for OTFTs due to the plastic substrate could not sustain high temperature. For the purpose of low cost and high throughput processes, atmospheric pressure plasma jet (APPJ) was utilized in this paper. Figure 1 shows the basic structure of atmospheric pressure plasma jet. Because APPJ could be operated in atmospheric pressure it is suitable for large area application which is very important for cost down (20-23). Effect of carrier gas's flow rate on SiO_2 would be discussed by us. We mainly measured the surface roughness and leakage current density to determine the quality of gate insulator. Good quality of silicon oxide deposited by APPJ had been developed by us and leakage current density was suppressed below 2.53E-8 A/cm^2 at 0.5 MV/cm in MIM structure. The thickness of our demonstrated silicon oxide is only 9.08 nm so the operation voltage of OTFTs was about -2 V. Threshold voltage is about 0.8 V, mobility is about 0.66 $cm^2/V\text{-}s$, and subthreshold swing is about 700 m V/decade in our proposed OTFTs.

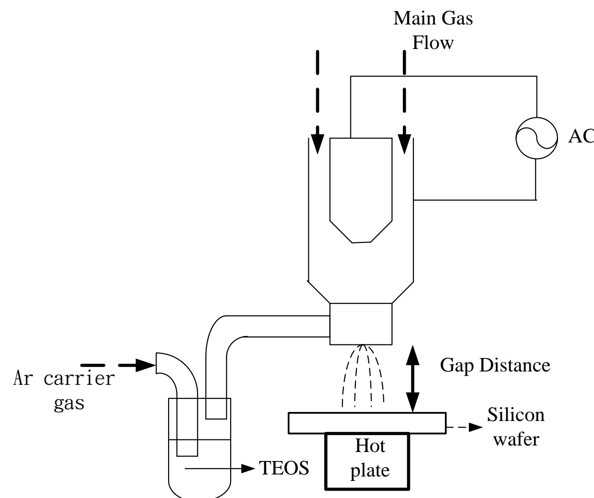

Figure 1 Schematic of the atmospheric-pressure plasma jet for the deposition of silicon oxide.

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Experiment

We used bubble method to carry the precursor into the plasma region and selected Ar as the carrier gas. Ar flow rate would influence the concentration of the precursor at nozzle which would influence the deposition rate and the quality of silicon oxide. The flow rate was selected from 60 ~ 300 sccm for analyzing the effect of flow rate on gate dielectric. The experimental detail was shown in Table I.

TABLE I. The detail experimental parameters of silicon oxide deposited with different flow rate were shown here.

Experimental parameters	
Main gas	CDA
Speed (mm/sec)	30
Gap distance (cm^2)	2.2
Scanning times	60
Ar flow rate (sccm)	60~300
Substrate temperature (℃)	150

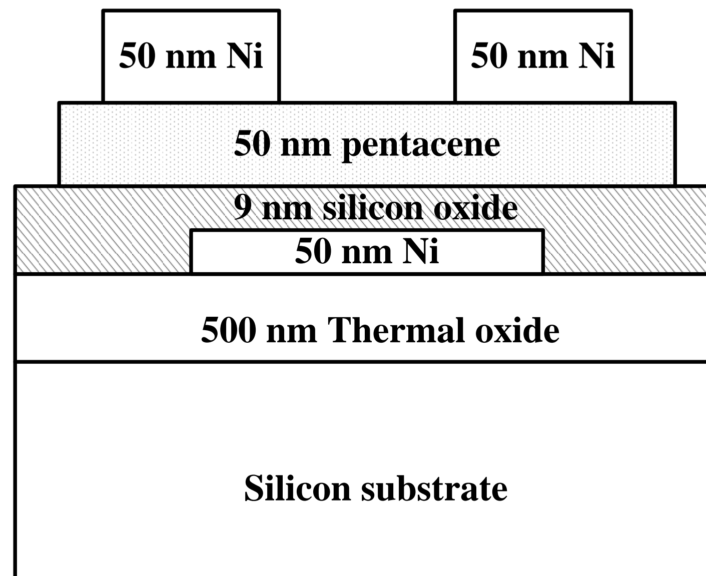

Figure 2 Top structure of organic thin film transistors fabricated with a low-temperature silicon dioxide deposited by APPJ.

We selected substrate temperature at 150 ℃ because every parameter test must be suitable for plastic substrate. Finally, we integrated our proposed silicon oxide into pentacene-based organic thin-film transistors. The 500 nm thermal silicon dioxide was grown on the top of p-type silicon wafer as the isolation layer. Gate electrode with a 50 nm thick Ni layer and Source/ Drain electrodes with 50 nm thick nickel layer were

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deposited by E-gun. Silicon oxide deposited by APPJ at 150 ^{o}C under an atmospheric pressure with 60 scanning times was used as gate insulator. The 50 nm pentacene material obtained from Aldrich was evaporated by thermal coater. During deposition of pentacene active layer, the substrate was heated to 70 ^{o}C at a pressure of $1x10^{-6}$ Torr. Figure 2 shows the top contact structure of OTFTs. The length and width of OTFTs were separately about 500 μm and 2000 μm.

Results and Discussion

From Figure 3, we could obviously found that the leakage current density increased with increasing the carrier gas flow rate. The gas flow rate at 60 sccm and 100 sccm could suppress the leakage current density below 2.53E-8 A / cm^2 at 0.5 MV /cm. However, when the flow rate over 200 sccm the leakage current was increase over 1E-6 A / cm^2 which is larger than 2.53E-8 about two order. From Figure 4, the thickness and roughness were increased with increasing the flow rate of carrier gas. The AFM plots were shown in Figure 5. The roughness of silicon oxide increased rapidly when the flow rate over 200 sccm. The rapid deposition rate would cause silicon oxide too loose to suppress leakage current.

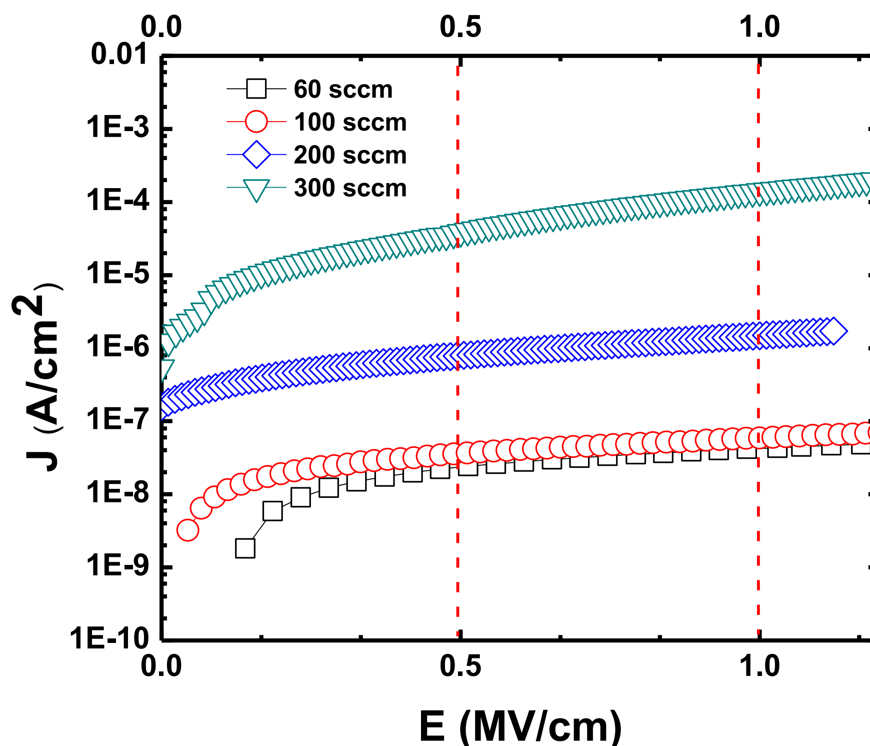

Figure 3 Plot of leakage current density versus electric field (*J-E*) of our APPJ- SiO_2 deposited with different carrier gas's flow rates.

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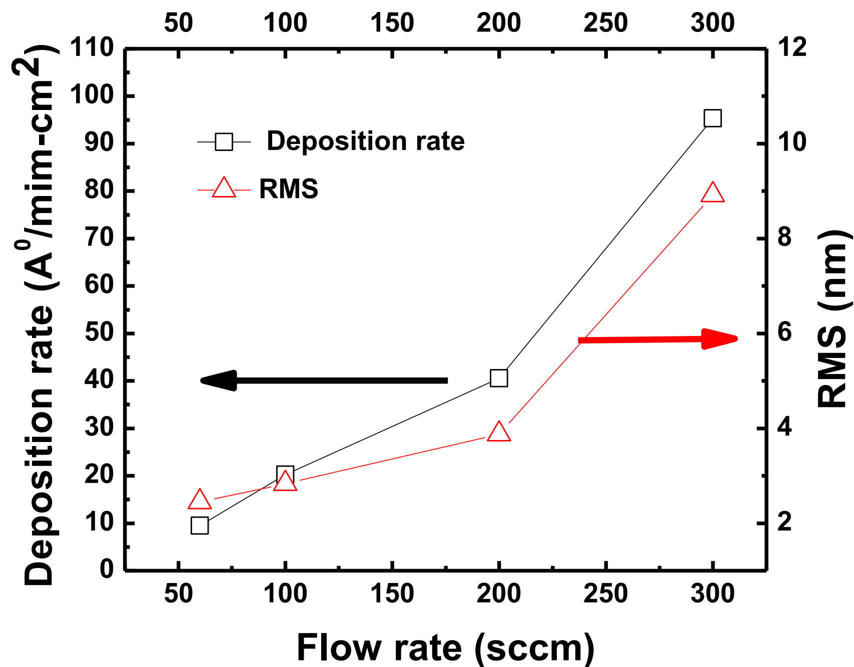

Figure 4 Deposited rate and RMS of silicon oxide deposited with different kinds of Ar flow rates of atmospheric pressure plasma jet.

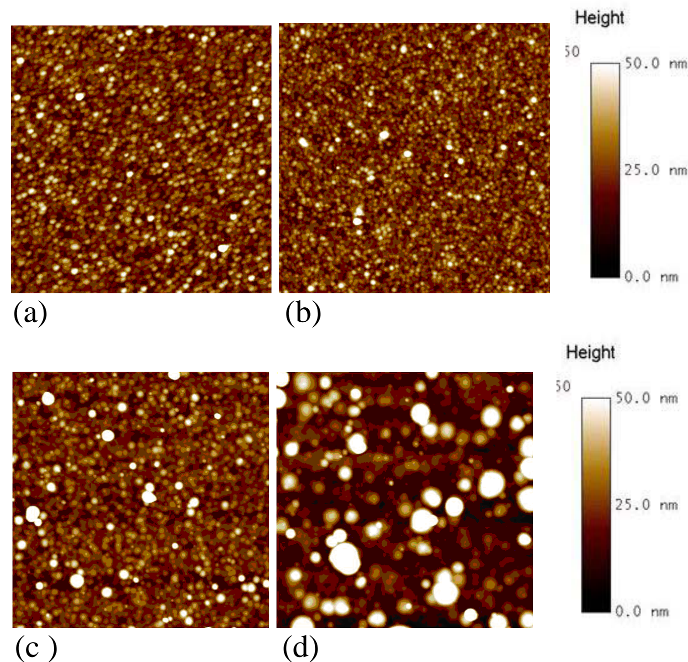

Figure 5 AFM images of silicon oxide fabricated with different Ar flow rates of atmospheric pressure plasma jet.
(a) 60 sccm (b) 100 sccm (c) 200 sccm (d) 300 sccm

In addition, we used SEM to get top view of silicon oxide surface which was shown in Figure 6. When the flow rate was increased the pellets was also increased obviously on

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the silicon oxide surface. These pellets must be decreased because the surface roughness would scatter transport carriers which would decrease the mobility of OTFT. On the hand, there are some researches indicated that organic molecules ordering and grain size would be degraded with high surface roughness which would decrease the mobility of organic semiconductor. In our experiment, the roughness of silicon oxide could be decreased by decreasing the flow rate and the pellets also could be decreased, which would increase the possibility of application for OTFT. Figure 7 shows the XPS of silicon oxide deposited with different flow rates. Carbon exited in silicon oxide was increased with increasing the flow rate. We used TEOS as the precursor for depositing silicon dioxide. Some precursor may not be decomposed completely and then deposited on the surface of sample to form the impurities which may consist of C-H, C-O, and C-O-O in our demonstrated silicon oxide. This phenomenon may be more serious when the flow rate increases. CVD reactions are homogeneous, heterogeneous, or a combination of both. Homogeneous reactions nucleate in the gas phase and lead to particle formation. The greatest single problem in CVD technology. Most CVD processes are chosen to be heterogeneous reactions. That is, they take place at the substrate surface rather than in the gas phase and form the desirable film deposit. In general, increasing temperature leads to increase film deposition rate, greater density, and improved structural perfection and crystallinity of the deposits. The quality of silicon oxide deposited by APPJ in this thesis was also improved with increasing temperature in lower flow rate. It is very important to control temperature and flow rate for depositing silicon oxide at heterogeneous reactions. Although silicon oxide deposited by APPJ in air may combined some particles or impurities good quality of insulator was obtained by well controlling temperature, flow rate, and other parameters of APPJ.

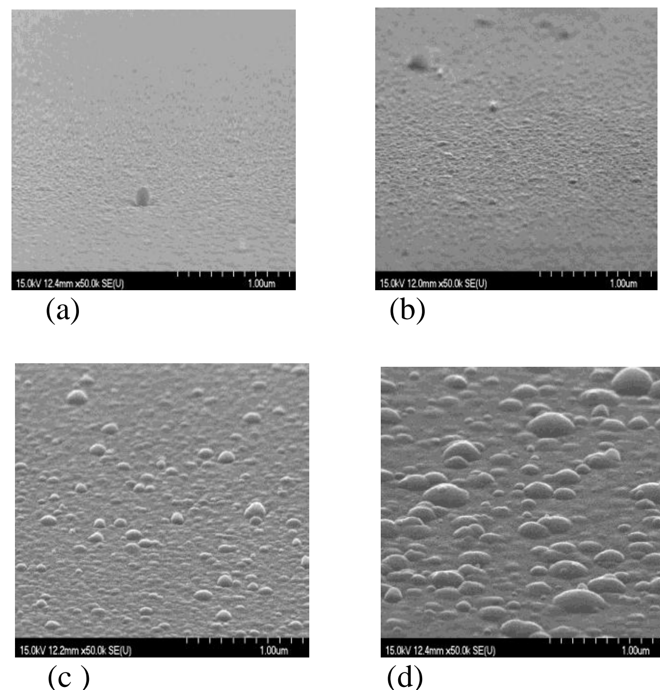

Figure 6 SEM images of silicon oxide fabricated with different Ar flow rates of atmospheric pressure plasma jet.
(a) 60 sccm (b) 100 sccm (c) 200 sccm (d) 300 sccm

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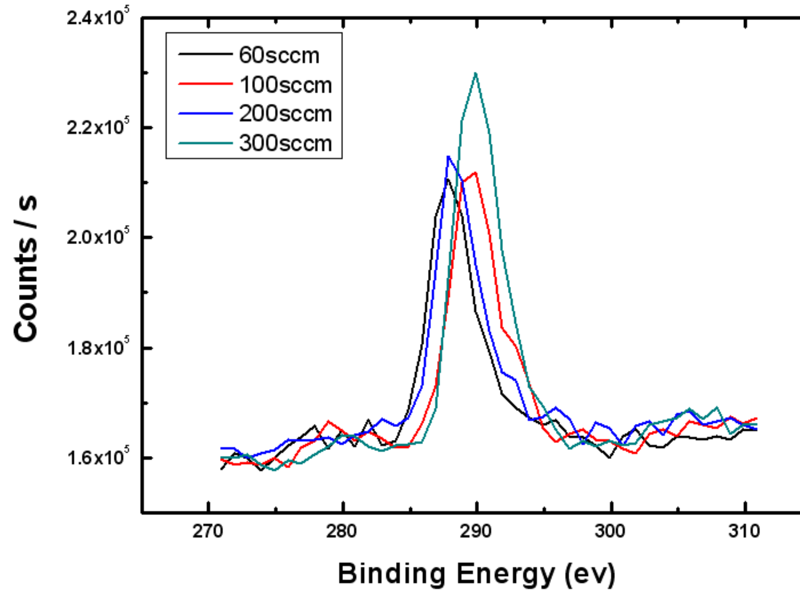

Figure 7 X-ray Photoelectron Spectroscopy spectra of SiO_2 (APPJ) deposited with different Ar flow rates.

The I_D–V_D characteristics shown in Figure 8 are well behaved and suggest possible operation at -2 V, which has the advantage of reducing the power consumption ($I_D \times V_D$) in circuit operations. The transfer characteristics (I_D–V_G), as shown in Figure 9, enable the extraction of the mobility and V_T from the $|I_D|^{1/2}$ versus V_G plot. The mobility was extracted in saturation region from the following equation:

$$I_{DS} = \left(\frac{WCi}{2L}\right)\mu(V_G - V_T)^2 \qquad [1]$$

Where Ci is the capacitance per unit area of the gate insulator, and V_T is the threshold voltage. Our device shows mobility was about 0.66 cm^2/Vs, threshold voltage was as low as -0.8 V, and the subthreshold swing was as low as 0.7 V/ decade. Subthreshold swing was extracted from the following relationship:

$$S = \frac{dV_G}{d(\log I_D)} = \ln 10 \frac{dV_G}{d(\ln I_D)} = 2.3\frac{kT}{q}\left[1 + \frac{Cd + Cit}{Ci}\right] \qquad [2]$$

Where Cd is the depletion-layer capacitance density, Cit is interface state capacitance density, and Ci is the gate capacitance density. The low subthreshold swing indicates low interface state and high switch speed. The device shows a lower operation voltage about -2 V, a lower threshold voltage about -0.8 V, a good mobility 0.66 cm^2/V-s, and a good subthreshold swing about 700 mV/decade. Table II shows the summarize the characteristics and processes of OTFTs studied by other researches about low operation voltage or low temperature processes for comparing with this work (24-27). In deposition system, most researches used vacuum deposition system for fabricating their high-k material and subsequently processed with a high temperature annealing. Some researches utilized spinning technique to fabricated polymer or nanocomposite as gate insulator of

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OTFT but polymer or nanocomsite must bake for a long time. Our demonstrated silicon oxide was deposited at low temperature and atmospheric pressure by APPJ without annealing and shows good insulator quality. Our proposed OTFTs have lower operation voltage, subthreshold voltage, and subthreshold swing which are contributed by the thinner thickness, lower surface roughness, and higher quality gate insulator.

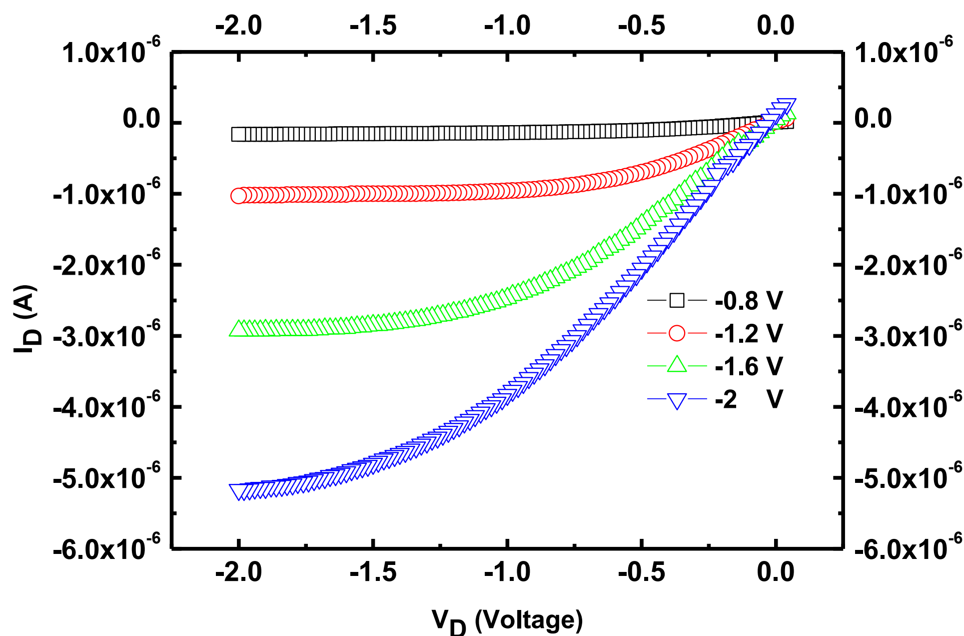

Figure 8 Output characteristics (I_D-V_{DS}) of OTFTs fabricated with SiO_2 deposited by APPJ.

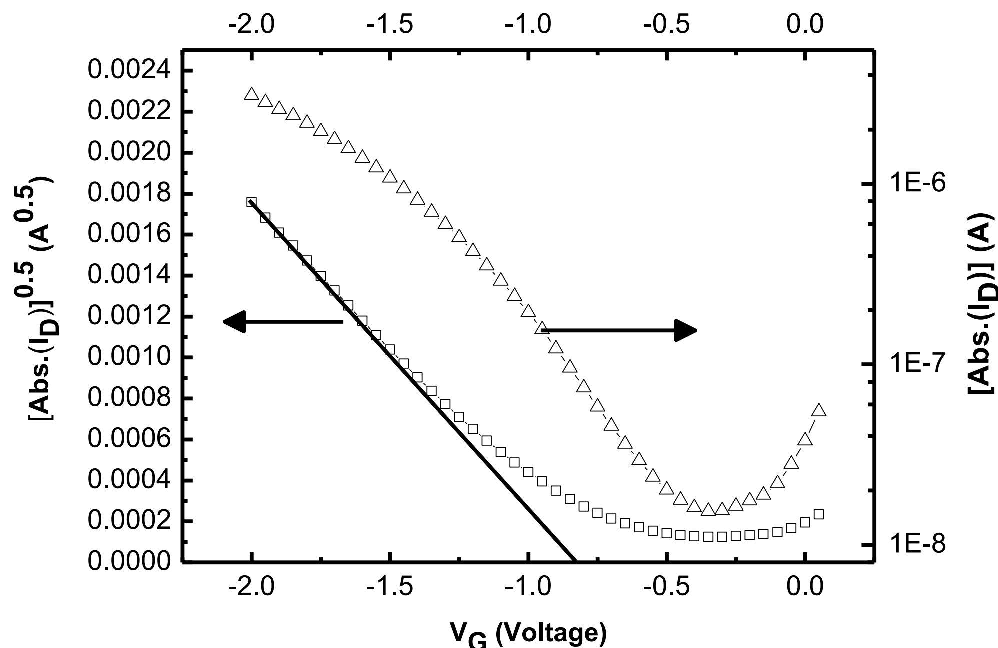

Figure 9 Transfer characteristics (I_D-V_G) and $|I_D|^{1/2}$-V_G of OTFTs with a thin SiO_2 deposited by APPJ.

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TABLE II. Comparison of this work with other researches about the characteristics of OTFTs fabricated at low temperature processes or operated at low voltage.

	Gate oxide material	Deposition method	Processes temperature (^{o}C)	Leakage current density (A/cm^2) at 0.5 MV /cm	Operation voltage (V)
Ref. [24]	AlN	Sputter	$150^{o}C$	1E-9~1E-8	-5
Ref. [19]	Ta_2O_5	E-gun	Unknowable	1E-7~1E-8	-3
Ref. [25]	Nanocomposite	spin	200 ^{o}C	1E-6~1E-7	-40
Ref. [26]	HfLaO	E-gun	$350^{o}C$	1E-7~1E-8	-2
In this paper	Silicon oxide	APPJ	150 ^{o}C	2.53E-8	-2

Conclusion

High quality SiO_2 was obtained by well controlling carrier gas's flow rate of APPJ and leakage current density was suppressed below 2.53E-8 A/cm^2 at 0.5 MV/cm. Flow rate of carrier gas seriously influenced the surface roughness and leakage current density of SiO_2. Therefore, we must control deposition mechanism in heterogeneous reactions to reduce the generation of nucleation. Nucleation could cause lots of pellets on the SiO_2 surface increasing the surface roughness and lead loose film. Good performance of OTFTs was obtained due to high quality and thinner thickness of SiO_2. Operation voltage was about -2 V, threshold voltage was about -0.82 V, and subthreshold swing was about 700 mV/dec. were shown in our OTFTs.

Acknowledgments

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