Power Management With a Low-Ripple High-Conversion-Ratio 80-V Output Voltage Boost Converter for Avalanche Photodiode System

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***Abstract*—Avalanche photodiodes (APDs) accompanied with the transimpedance amplifiers (TIAs) are often utilized as receivers in the communication system. A drawback of APDs is that the avalanche gain depends on temperature and varies with the bias voltage, leading to a decrease in the quality of communication. Moreover, the bias voltage for a high avalanche gain is up to 80 V, implying that a power module is inevitably required and raises the difficulty of integration. Therefore, a power management is proposed to provide an 80-V voltage and compensates the temperature dependence for a constant avalanche gain. The low-ripple high-conversion-ratio boost converter eliminates the LC resonance resulted from the nonideal effect of diodes to supress the output voltage ripple, implying that a high quality of bias voltage is guaranteed. Experimental results show that the output voltage ripple is 2.12 mV under the condition of 1-mA load current. A 97% accuracy of avalanche gain is proved to guarantee the high quality of APDs.**

***Index Terms*—Avalanche photodiodes (APDs), high-conversation-ratio boost converter, high reverse-biasing voltage, output voltage ripple.**

I. Introduction

In recent years, integration has led the trend of technology. In information technology, system integration links together different computing systems and software applications physically or functionally, to act as a coordinated whole. Avalanche photodiodes (APDs) are widely used in a variety of optical applications requiring high sensitivity since APDs can detect low-level light [1], [2]. The ability of APDs to operate in midwave infrared range (2–5 μm) wavelength region is useful in many applications such as remote sensing, thermal imaging, and chemical sensing in industrial and military operations and also in medical diagnostics [3]. APDs can offer high sensitivity, achieved via the internal gain provided by the multiplication.

Fig. 1 shows the generic transmission system with APD photoreceivers for long-haul transmission [4], [5]. On the transmission side, the current driver turns on the laser diode to enable the laser communication. The polarization-maintaining fiber transmits the signal to the modulator and erbium-doped fiber amplifier. Thus, the signal would be modulated to a facilitated signal for transmission. The single-mode fiber sends this signal through a long distance of 50–100 km. The Raman amplifier produces photons coherent with the incoming photons. Moreover, the optical information system possesses different number of wavelength-division multiplexing channels for different application. On the receiver side, the APDs receive the photon energy and carry out the corresponding current signal. The photodiode preamplifier, transimpedance amplifier (TIA), is added to modulate the signal. The TIA amplifies the single-ended input current $I_{\rm APD}$ and converts it into a voltage output signal. Some circuits such as limiting amplifiers, buffers, and a 50-Ω output driver are included to modify the output voltage of TIA. To keep the high performance, a constant avalanche gain is needed.

APDs operate with a high reverse voltage across the junction that excites the generation of electron–hole pairs in response to incident radiation. The electron-hole pairs are then swept by the applied field to be converted into a current signal, which is proportional to the radiation intensity [6]–[9]. In Fig. 2, conventional APD modules, which consist of APDs and the preamplifiers, which are usually TIAs, served as a receiver in the optical communication system and are supplied by an open-loop power management. Most APDs require high reverse-biasing voltages to activate the avalanche mechanism, and this high reverse-biasing voltage is usually between 40 and 60 V, while some APDs might require voltages as high as 80 V for a higher avalanche gain [10], [11].

In conventional open-loop power management design, as shown in Fig. 2, the voltage for APDs $V_{\rm APD}$ is stepped up from a supply voltage $V_{\rm in}$ between 1.8 and 3.3 V to 40 V by the first-stage dc–dc boost converter [11]–[15] and amplified again to 80 V by the second-stage charge-pump circuit. The first stage achieves a medium ratio conversion to convert the low input voltage to a high voltage for the next stage constituted by the charge pump. Considering the boost topology, the power switch, which is controlled by the signal V_G is required at

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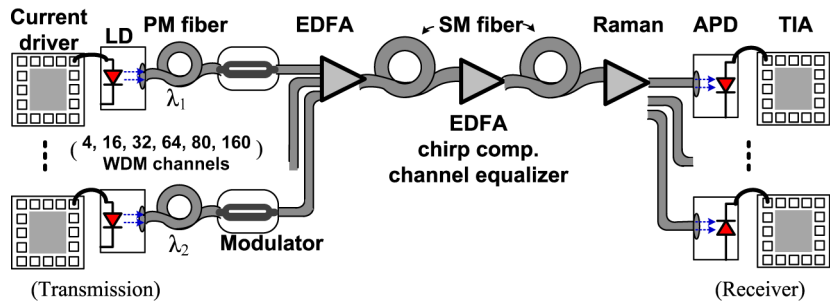

Fig. 1. Transmission system with the APD detectors.

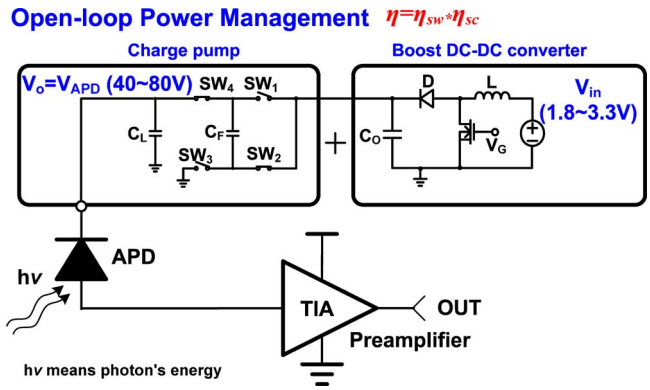

Fig. 2. Conventional APD module with the open-loop power management module.

least to control the energy delivery process in the inductor. The second stage pumps the voltage large enough to drive the APD according to the system requirement. Thus, one flying capacitor C_F and some switches are needed to complete the voltage conversion. The C_L is used to show the equivalent output and capacitance.

A distinctive feature of switching converters is the ripple voltage at the output [16]. In conventional two-stage designs, the first-stage output needs a bulky capacitor to reduce the voltage ripple. In the meanwhile, the similar size capacitor is also needed at the second-stage output. The two capacitors increase the printed circuit board (PCB) area and the volume of the system.

An intuitive way of facilitating the integration of the power management module is to get rid of the combination of the boost converter and the charge-pump circuit. Due to the demand of high conversion ratio in this application, a single charge-pump circuit is obviously not the suitable solution to provide this high voltage, and the boost converter becomes the better solution in this case. The hysteretic control in [11] presents a good solution for a fast transient response, and the fast reference tracking technique is proposed in [12] to fulfill the adaptive output requirement. The digital control method is also proposed in [13]. However, a voltage gain of at least ten is needed in this application. The obvious disadvantages when large conversion ratio is required are the following: 1) Near unity duty cycles lead to difficulties in the operation at higher switching frequencies, and 2) the boost switches suffer from both high voltage and current stresses, which leads to high power losses. Moreover, the low-ripple feature complicates the design for high-conversion-ratio boost converter. Furthermore, the conventional open-loop power management cannot dynamically vary the value of the high reverse-biasing voltage according to the temperature and environmental variation.

As a result, to keep a constant avalanche gain, this paper proposes the power management with the high-efficiency low-ripple high-conversion-ratio (LRHCR) boost converter and a feedback control system to directly provide a high quality and dynamic reverse-biasing voltage for APDs. The organization of this paper is described as follows. Section II introduces the features of the APDs, and Section III presents the design methodology of the closed-loop power management. Section IV shows the detailed circuit implementations. Experimental results shown in Section V verify the design of the proposed boost converter. Finally, a conclusion is made in Section VI.

II. Features of APDs

APDs are utilized to operate close to the avalanche point. The most distinctive feature between APDs and other photodiodes is that the APD builds a high electric field (>105 V/cm). When a single photon enters the APD from the optical fiber, this causes the photon to be absorbed and generates an electron–hole pair. The hole is accelerated by the strong electric field in the APD and undergoes lattice collision, changing a valence electron into a free electron. More and more free electrons are created due to repeated lattice collisions, so the current in the APD increases dramatically in an avalanche effect. APDs therefore are more sensitive compared to other semiconductor photodiodes [17]–[19]. The avalanche gain (M) is depending on the electric field which is across the avalanche layer, and the equation can be approximated as

$$M = \frac{1}{\left(1 - \left(\frac{U}{U_b}\right)^n\right)}. \tag{1}$$

Here, U and U_b are the reverse-biasing voltage applied to APD and the breakdown voltage, respectively. The parameter n is a number which depends on the resistivity and resistivity type of high-resistivity side of the junction. In general, the higher reverse-biasing voltage can obtain the higher gain. However, if the reverse-biasing voltage exceeds the breakdown voltage, a large current would flow through the APD and lead to a permanent damage. Moreover, the avalanche gain has a strong dependence on temperature. When the APD operates at lower temperature, the gain of APD is higher. Fig. 3 shows the avalanche gain of InGaAs APD [1]. A large variation in

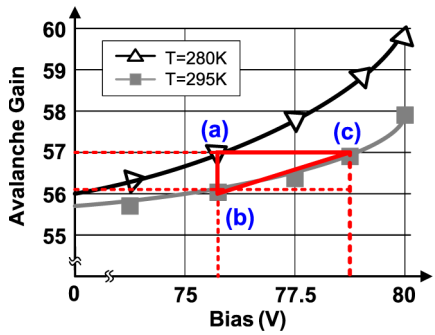

Fig. 3. Voltage and temperature dependences of APD avalanche gain.

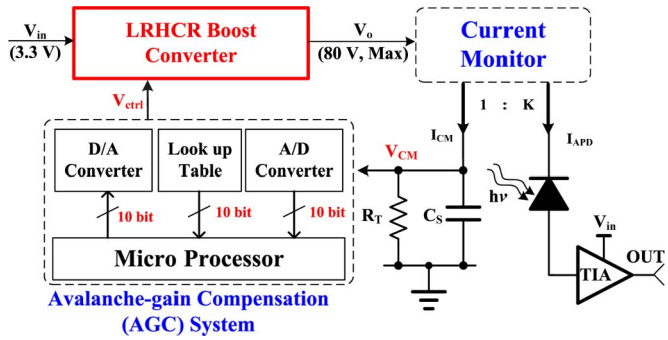

Fig. 4. Power management for the APD system.

the avalanche gain is resulted from the small variation in the reverse-biasing voltage.

Nowadays, the improving manufacturing process allows different types of APDs according to their application fields. Since the avalanche gain varies strongly with the applied reverse-biasing voltage and temperature, it is necessary to control the reverse-biasing voltage and compensate the temperature effect to keep a stable gain. As shown in Fig. 3, the avalanche gain of 57 is chosen for the target value, and the bias voltage is thus determined. The operation point of temperature and voltage is set at label (a) in the beginning. Due to the increasing temperature, the avalanche gain is decreased, and the operation point moved to label (b) accordingly. High temperature makes the gain smaller than the desired value. To maintain the constant avalanche gain, the feedback control system will move the operation point forward to label (c) by increasing the reverse-biasing voltage higher than the beginning value.

Altering the reverse-biasing voltage can maintain the avalanche gain through the voltage-mode control. In other words, the adjustment of bias voltage serves as the modulation factor. Since the voltage is provided from switching converters, the voltage ripple, which is inevitably originated in switching converters, would be similar to an external noise for the APDs. Too large ripple may be induced owing to the high ratio conversion of the switching converter to cause interference on the avalanche gain. On the other hand, too low reverse-biasing voltage may cause the avalanche gain not enough when driving the APDs. As a result, a low-ripple reverse-biasing voltage is demanded for high performance in the APDs.

III. Design of the APD Power Management Module

The avalanche gain depends on temperature and varies with the manufacturing process. Therefore, for typical systems in which the APDs must operate at a constant gain, the high reverse-biasing voltage must vary to compensate for the effects of the temperature and manufacturing process on the avalanche gain. Applying an adjusted reverse-biasing voltage across the APDs creates the corresponding avalanche gain during the APD operation. To maintain the constant gain in typical APD applications, the temperature coefficient must be kept within approximately $\pm 0.2\%/^{\circ}\mathrm{C}$, which corresponds to 100 $\mathrm{mV}/^{\circ}\mathrm{C}$. The APD system contains temperature-measuring devices such as thermistors, a type of resistor whose resistance varies significantly with temperature, which can be connected directly to the power supply for adjustment of output voltage. In some accurate systems, the microprocessor (μP) reads the resistance value and then issues necessary bias-adjustment commands to the power supply [5].

Fig. 4 shows the power management for the APD system. The biasing control circuit can be divided into four parts—the LRHCR dc–dc boost converter, the current monitor, the avalanche-gain compensation (AGC) system, and an APD-based receiver. The LRHCR dc-dc boost converter provides high output voltage to drive the APD-based receiver. The current monitor provides more than three decades of dynamic range and monitor current ranging from 500 nA to 4 mA with high accuracy. A current ratio of 1:10 is adopted in the current monitor to detect the APD current I_{APD}. The sensed current I_{CM} flows through the thermistor R_T and the sensing capacitor C_S and is converted to the sensing voltage signal V_{CM}. Therefore, V_{CM}, which obtains both the output voltage and temperature information, can be used as a reference to adjust the output voltage V_o by the AGC system.

The V_{CM} is then transmitted to the AGC system, which contains an analog-to-digital converter (ADC), a temperature lookup table for fast response, a μP, and a digital-to-analog converter (DAC). After receiving the voltage and temperature information from V_{CM}, the compensation, for both temperature and manufacturing variations, is calculated by correcting the thermistor curvature through the lookup table. The compensation value would be converted back to an analog control signal V_{ctrl} through the DAC. In this application, the 10-b DAC provides approximately 80-mV resolution when the output voltage varies from 25 to 80 V. The successive approximation register ADC is used due to the slow change of temperature. Moreover, the current steering DAC is used to drive the feedback resistor. A global bandgap reference is applied for the ADC, the DAC, and the LRHCR boost converter to prevent the mismatch issue. Moreover, the system has a calibration procedure in the beginning of the operation to reduce the mismatch seen at different modules. The AGC system then issues V_{ctrl} to the power supply to adjust the avalanche gain, by adjusting the value of the feedback voltage of the LRHCR boost converter. The operation flowchart is shown in Fig. 5. Furthermore, each dc current in the APDs is limited so as to reduce damage to the preamplifier and APDs due to excessive currents.

Because the APD is biased by the dc–dc boost converter, the output voltage ripple originated from the switching converter should be concerned. The ripple voltage would directly couple

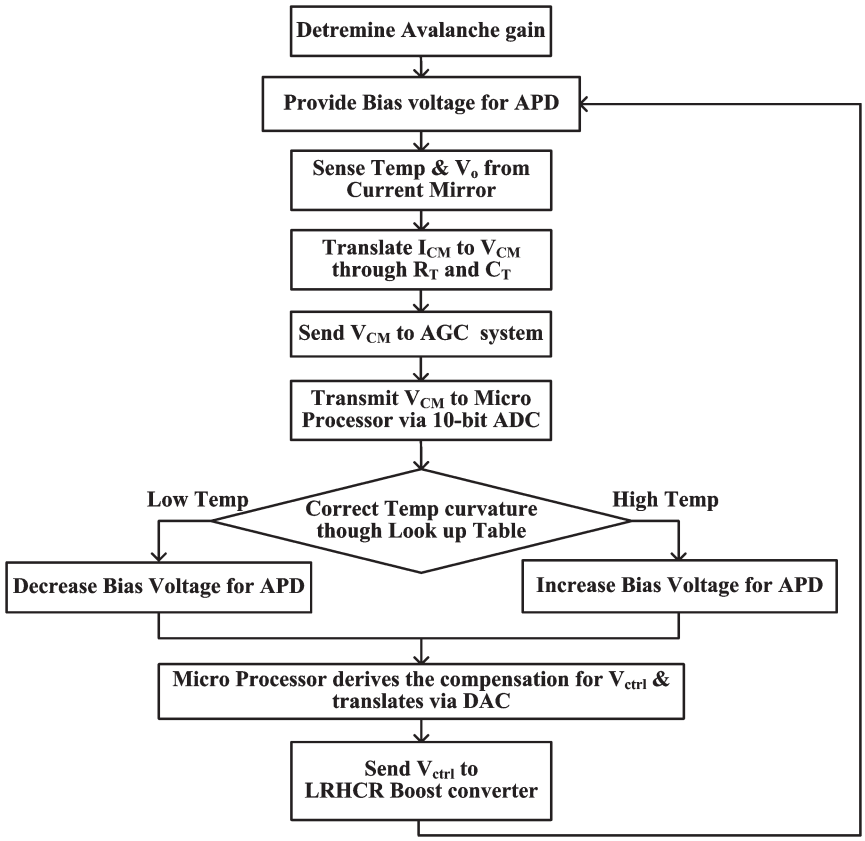

Fig. 5. Flowchart of the AGC operation.

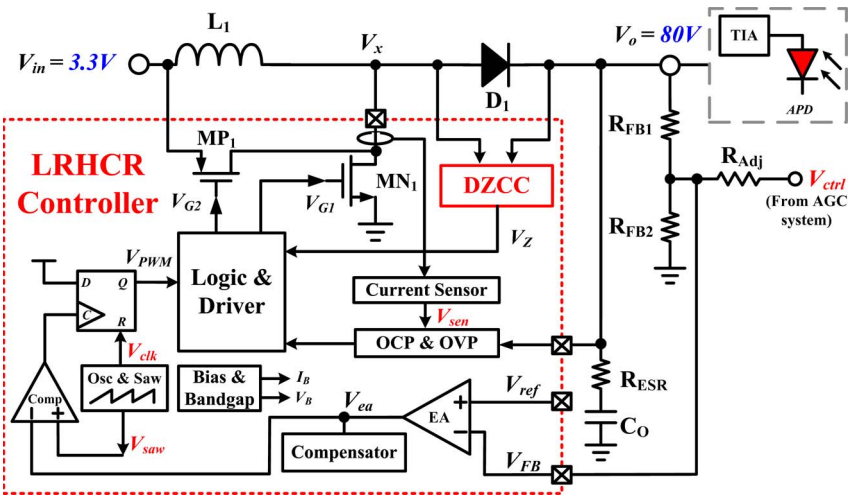

Fig. 6. Proposed LRHCR boost converter with the DZCC circuit.

to the TIA through the APD and causes the fluctuation on the received signal. To eliminate the interference, the ripple voltage must be small, and it is a challenge for the dc-dc boost converter [20], [21]. As a result, the LRHCR boost converter is proposed in Fig. 6. The output voltage V_o could be adjusted by the $V_{\rm ctrl}$ through the feedback resistor $R_{\rm Adj}$ to achieve the gain compensation. An external voltage reference $V_{\rm ref}$ is used in the LRHCR boost converter to prevent offset mismatch among the power management. Moreover, the dynamic zero current correction (DZCC) circuit in the LRHCR controller is proposed to reduce the occurrence of negative inductor current and thus improves the efficiency. More design considerations are detailed in the next section.

IV. Circuit Implementation

Since the ripple voltage is equivalent to the product of the inductor current and the equivalent series resistance (ESR) of the output capacitor, either the inductor current or the ESR should be minimized. The ESR is determined by the selection of output capacitor. Thus, the LRHCR boost converter is focused on the reduction of inductor current.

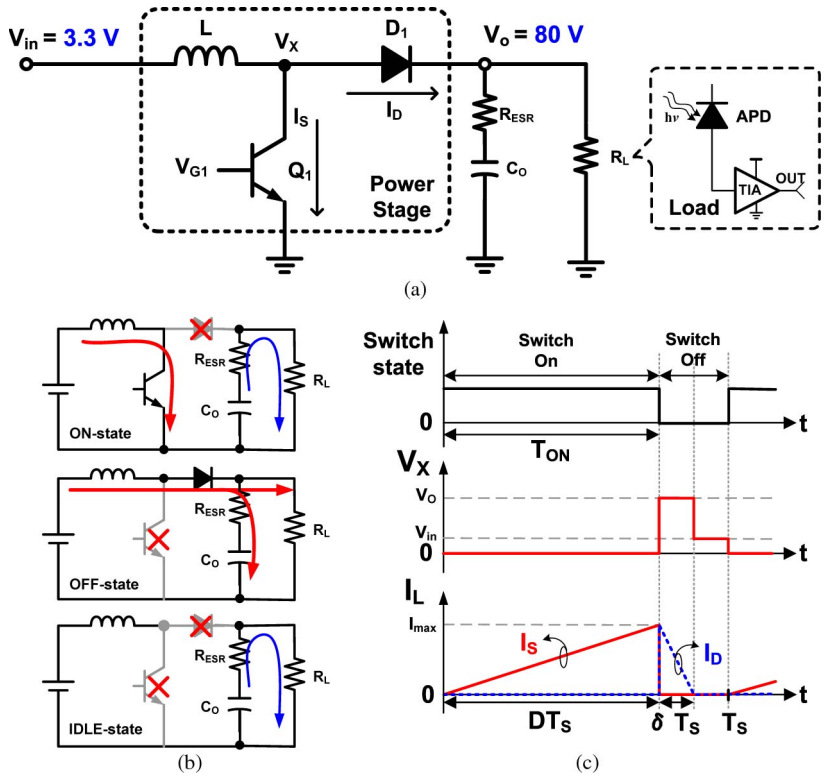

Fig. 7. (a) Simplified schematic of the boost converter. (b) Operation of boost converter in the DCM. (c) Timing diagrams.

A. *Selection of the Operation Mode*

The loop gain of the boost converter in the continuous conduction mode is approximately equal to 70 dB. The second pole and right-half-plane zero of the boost converter appear at low frequencies, and thus, a complicated compensator is needed to stabilize the system. However, since the maximum load current of the APD is less than 5 mA, it is suitable to force the boost converter to operate in the discontinuous conduction mode (DCM) for avoiding the unstable situation. Fig. 7(a) shows a simplified schematic of the boost converter without the control circuit. The operation principle of the DCM boost converter is shown in Fig. 7(b), including three inductor current states. In the on state, the Q_1 is on, and the D_1 is off. In the off state, the Q_1 is off, and the D_1 is on. An idle state exists when both the Q_1 and the D_1 are off and the inductor current is zero. The timing diagrams of the V_X and the I_L are shown in Fig. 7(c). In the inductor discharging phase, namely, the off state, the V_X is equal to the V_o, implying that the high voltage sustainability for power switch is needed in the high-conversion-ratio design.

The $i_{\mathrm{L,peak}}$ in (2) can be minimized through the increase of switching frequency for a smaller output voltage ripple. Moreover, a larger inductor also helps reduce $i_{\mathrm{L,peak}}$. In this design, an inductor of 82 μH is chosen, and the switching frequency is 200 kHz

$$i_{\mathrm{L,peak}} = \sqrt{\frac{2 \cdot T_S \cdot (V_o - V_{\mathrm{in}}) \cdot I_o}{\eta \cdot L}}. \tag{2}$$

The relationship between the V_{in} and the V_o can be derived as (3), where D is the ratio of power switch on time and T_S is the switching cycle. According to (3), the steady-state control duty

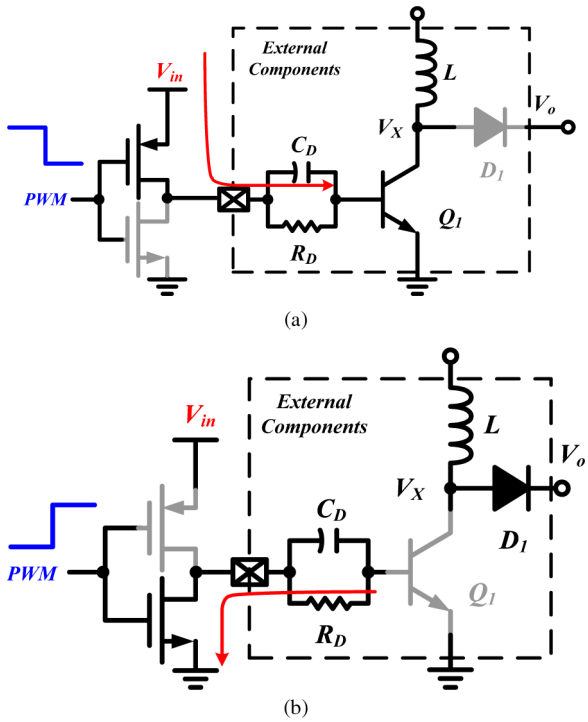

Fig. 8. Turn on and off procedures of the BJT power switch. (a) Turn-on state. (b) Turn-off state.

can be obtained [16]. It is obvious that the duty is very large to get high conversion ratio. Moreover, the D depends on the load current

$$\frac{V_o}{V_{\mathrm{in}}} = \frac{1 + \sqrt{\frac{2D^2 R_L T_s}{L}}}{2}. \tag{3}$$

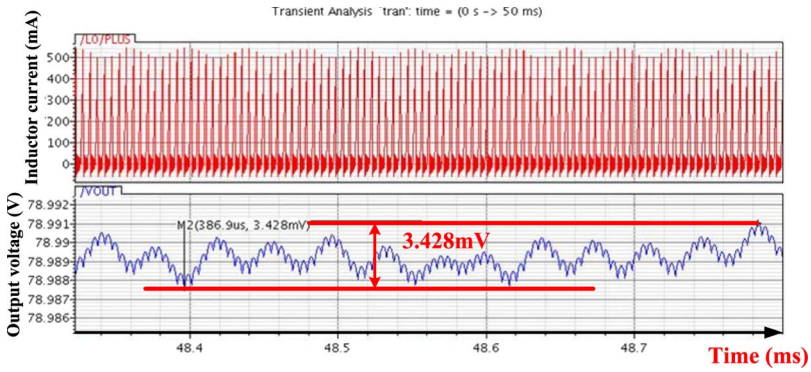

Fig. 9. Simulation result of inductor current and output voltage with BJT switch.

B. Selection of the Power Switch

Ideally, the turning on/off power switch depends on the pulse-width modulation control signal and the speed of the switch. However, when the power switch comes to a bipolar junction transistor (BJT) component, to fully turn off the BJT power switch would require a negative voltage. The external parallel resistor R_D and capacitor C_D are added to form this negative voltage, and the operation of BJT power switch is shown in Fig. 8.

The main problem encountered is that the unreleased charge remained on the external capacitor C_D in the power switch off-state period in such a large duty boost converter, which would lead to a different delay time for turning on the power switch. In other words, the time to charge the capacitor C_D for turning on the power switch varies and thus causes a fluctuation on the output voltage. The simulation result is shown in Fig. 9. The fluctuation of inductor current reflects on the output ripple voltage. The voltage difference is as large as 3.4 mV. It is hard to meet the low ripple requirement in the APDs.

As a result, a MOSFET-type power switch is a better solution for this circuit. Moreover, to have a compact solution, the power MOSFET is integrated into the chip in this design. An n-type power MOSFET is adopted in this converter. Since the output voltage of the boost converter is high as 80 V, the withstanding voltage of power MOSFET is extremely critical. Here, the power MOSFET uses the 80-V LDMOS to sustain the 80-V cross voltage.

C. Selection of Output Component

For an asynchronous boost converter, a Schottky diode is usually utilized to comprise the power stage due to the relatively low forward-voltage drop between approximately 0.15 and 0.45 V; this lower voltage drop translates into higher system efficiency.

Fig. 10 shows the nonideal switch waveform of boost converter. Initially, the diode conducts the inductor current, and the switch is in its off state. When the current turns to zero, the diode cannot turn off immediately, and thus, the negative current flows through the Schottky diode. The time it takes to remove the charge $Q_{\rm rr}$ accumulated within the Schottky diode is the reverse recovery time $t_{\rm rr}$, as shown in Fig. 10(b). The $t_{\rm rr}$ can be up to tens of nanoseconds for high-capacity power

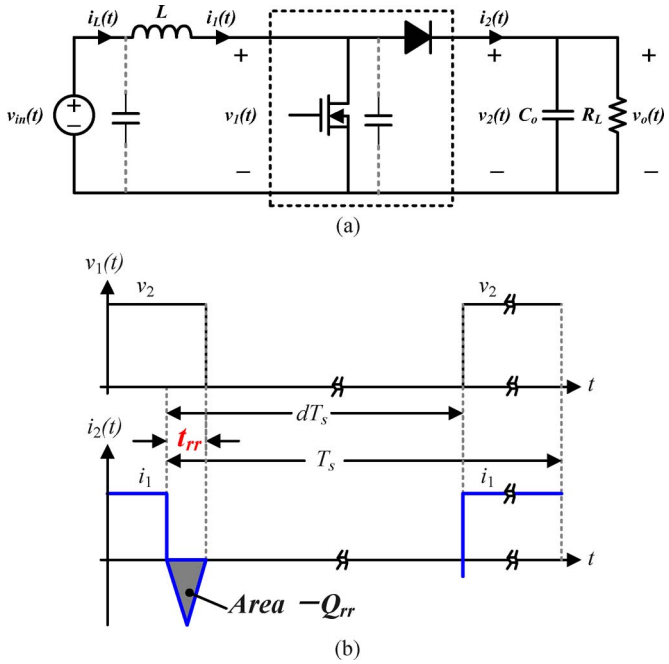

Fig. 10. Reverse recovery time. (a) Boost converter. (b) Switch waveform.

diodes, implying that the nonideal effect of diodes should be taken into consideration.

The output voltage and output current are derived in (4) and (5), respectively. The parameter d represents the duty ratio as shown in Fig. 10(b). As a result, the averaged model of the boost converter with the consideration of the reverse recovery loss is modified as shown in Fig. 11

$$\langle v_o(t)\rangle_{T_s} = \langle v_1(t)\rangle_{T_s} \cdot \frac{1}{\left(1+\frac{t_{\rm rr}}{T_S}\right)-d} \tag{4}$$

$$\langle i_2(t)\rangle_{T_s} = \left(\left(1+\frac{t_{\rm rr}}{T_S}\right)-d\right)\langle i_1(t)\rangle_{T_s} - \left[\frac{Q_{\rm rr}+t_{\rm rr}\langle i_1(t)\rangle_{T_s}}{T_s}\right]. \tag{5}$$

The conversion ratio is modified as

$$\frac{v_o}{v_{\rm in}} = \frac{1}{\left(1+\frac{t_{\rm rr}}{T_s}\right)-d}. \tag{6}$$

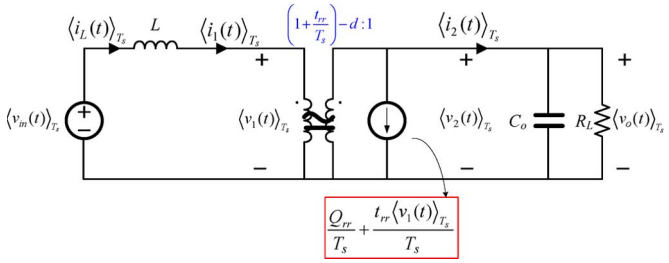

Fig. 11. Modified average model of boost converter with $t_{\rm rr}$ effect.

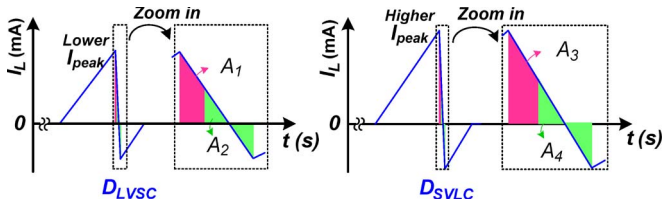

Fig. 12. Sketched inductor currents of diodes $D_{\rm SVLC}$ and $D_{\rm LVSC}$.

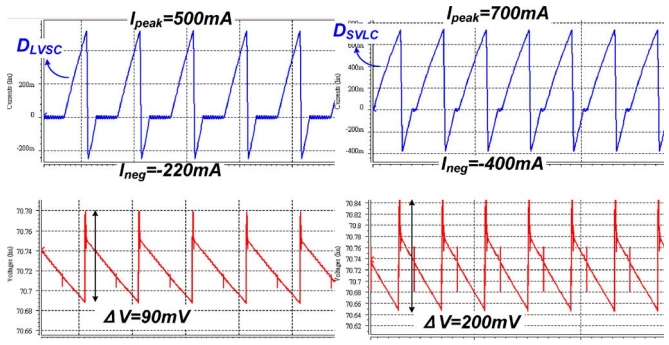

Fig. 13. Simulation results of diodes $D_{\rm SVLC}$ and $D_{\rm LVSC}$.

In a well-regulated condition with a constant ratio of v_o and $v_{\rm in}$, the d is increased due to the $t_{\rm rr}$, which leads to a higher peak inductor current. To eliminate the effect of reverse recovery energy, a faster $t_{\rm rr}$ is desired.

The steady-state inductor current is derived as

$$I_1 = \frac{I_2 + \frac{Q_{\rm rr}}{T_s}}{1-d}. \tag{7}$$

Due to the $Q_{\rm rr}$, a higher value is thus obtained, which should be avoided while working toward a low ripple voltage.

The conversion efficiency is also derived as

$$\eta = \frac{V_o \cdot I_2}{V_{\rm in} \cdot I_1} = \frac{1}{1+\frac{t_{\rm rr}}{(1-D)T_s}} \cdot \frac{1}{1+\frac{Q_{\rm rr}}{I_o T_s}}. \tag{8}$$

In general, the commercial Schottky diodes can be divided into two types. One is $D_{\rm SVLC}$, which has a small forward voltage and a large internal capacitance, implying high reverse recovery energy. The other is $D_{\rm LVSC}$, which instead has a large forward voltage and a small internal capacitance. The sketch and simulation results of the inductor currents with diodes ($D_{\rm SVLC}$ and $D_{\rm LVSC}$) are shown in Figs. 12 and 13, respectively. The simulation is set to provide an output voltage of 70 V, and the load current is 4 mA.

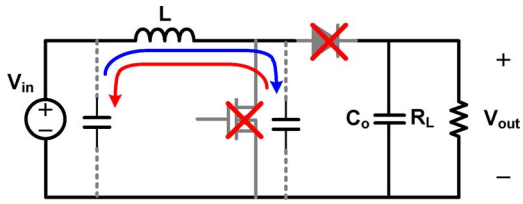

Fig. 14. LC resonance in the idle stage of the DCM operation.

In Fig. 12, the transmitted energy from input to output voltages can be divided into two parts. The first part, the area of A_1 (or A_3), is delivered to the load current. The areas of A_1 and A_3 are equal at the same load current. The other part, the area of A_2 (or A_4), is used to overcome the reverse recovery energy. Since the Shottky diode $D_{\rm SVLC}$ requires larger recovery energy to switch the state of Shottky diode, which is equal to area A_4, the peak current would be increased. The larger peak current induces a larger output voltage ripple. The increment of inductor current is critical particularly for a high-conversion-ratio boost converter demanding for low voltage ripple. The power consumption is increased even if the forward voltage of diode $D_{\rm SVLC}$ is smaller. Moreover, the maximum power would also be clamped by the longer reverse time from negative current. As a result, the Schottky diode $D_{\rm LVSC}$ with larger forward voltage and fast recovery time is utilized to reduce power consumption and voltage ripple.

The reverse recovery energy raises the peak inductor current due to the negative inductor current. Moreover, due to the existence of idle stage in the DCM operation, both power switch and diode are in the off state, and an LC resonance happens between the input capacitance and parasitic capacitance through the inductor, as shown in Fig. 14.

The LC resonance would lead to the oscillation at the output voltage due to the unreleased energy. In other words, the nonzero effect in the next inductor charging period causes a larger output ripple due to the $Q_{\rm rr}$. To eliminate the ripple resulted from the $Q_{\rm rr}$, both a small $t_{\rm rr}$ and a large inductor, which leads to a slow discharging slope of the inductor current, are desired. Moreover, the reverse recovery energy should be released in a short time, implying that a fast resonant frequency is desired. The LC resonant frequency f_o is shown in

$$f_o = \frac{1}{2\pi\sqrt{LC}}. \tag{9}$$

A tradeoff happens in the choice of inductor. As a result, an antiring control is proposed in the LRHCR boost converter to get rid of the nonideal effect.

D. Architecture of the Proposed LRHCR Boost Converter

The proposed LRHCR boost converter as shown in Fig. 6 adopts the DZCC circuit, as shown in Fig. 15. The voltages L'_X and V'_O are scaled values of the L_X and the V_O, respectively. The comparison of the L'_X and the V'_O can determine the zero inductor current. Here, the dynamic adjustment of the resistor value can accurately detect the zero current since the propagation delay and offset of the comparator can be compensated.

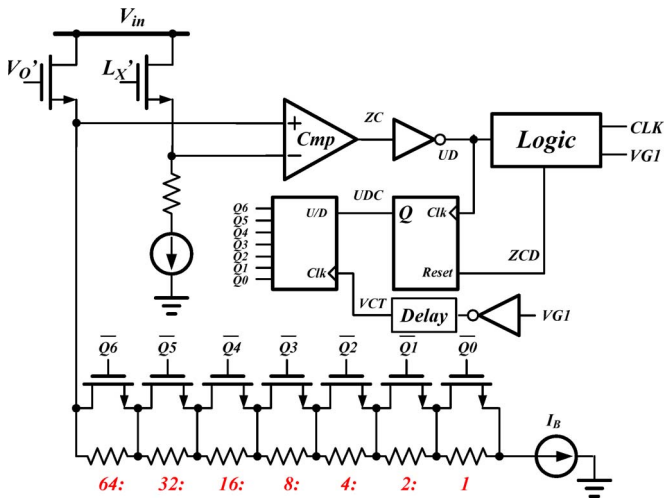

Fig. 15. Proposed DZCC circuit.

Whenever the inductor current is decreased below zero current, the DZCC would enlarge the resistor gradually to shorten the time of negative current through the control signals $Q[0:6]$ and simultaneously turn on the antiring MOSFET $MP1$ in Fig. 6 to prevent the negative current and LC resonance. The output ripple is therefore suppressed.

The output voltage is also adjusted by the signal $V_{\rm ctrl}$, which comes out from the AGC system in Fig. 4, to form a closed-loop power management system. Therefore, a constant APD gain is obtained, and the correctness of information can be guaranteed. The switching frequency is an important design parameter due to the tradeoff between switching ripple and switching loss. The switching periods have been intentionally fastened to reduce the switching ripple. The high-frequency spikes present in most cases are eliminated through the help of low-pass filter. Moreover, the low-pass filter also reduces the high-frequency di/dt and dv/dt rates, which minimize radiated and coupled noise to surrounding circuits through current loops and capacitances between PCB traces or component pins.

To get low output ripple, the switching noise needs to be further reduced by the low-pass filter. In this paper, a low-pass filter composed of a resistor (100 Ω) and a capacitor (0.1 μF) is added to suppress the output voltage ripple and switching noise. If the voltage ripple is seriously concerned, the low-pass filter can be replaced by a combination of an inductor (2.2 μH) and a capacitor (0.1 μF).

E. Small-Signal Analysis of LRHCR Boost Converter

Only a single pole exists in the LRHCR boost converter due to the DCM operation [22], [23]. The proportional–integral (PI) compensator is used to extend the bandwidth and enhance the stability. The Bode plot of the proposed boost converter is shown in Fig. 16. The zero in the PI compensator compensates the worst case that happened at the output pole, while the PI dominant pole is kept at the same frequency. As a result, the system stability is improved.

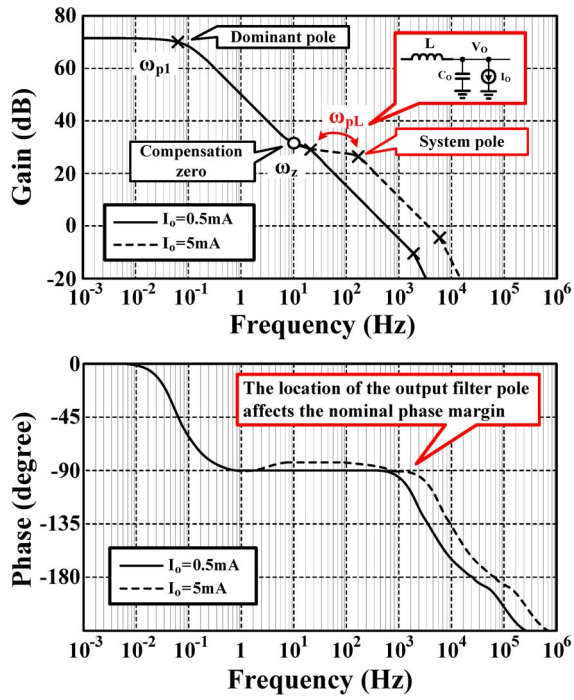

Fig. 16. Bode plot of the proposed LRHCR boost converter.

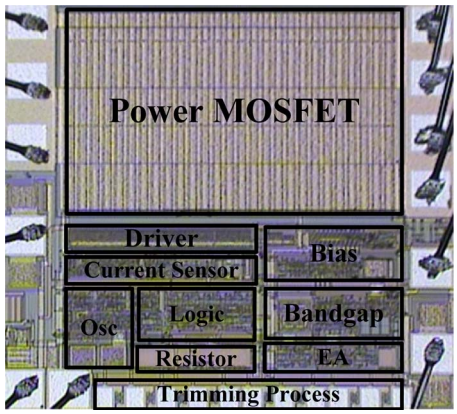

Fig. 17. Chip micrograph.

V. Experimental Results

The proposed LRHCR boost converter is fabricated in 0.5-μm United Microelectronics Corporation 80-V Bipolar, CMOS, DMOS (BCD) process. A chip micrograph is shown in Fig. 17. The occupied silicon area is $1050 * 1033$ μm^2. The external inductor and capacitor are 82 μH and 0.2 μF, respectively. Compared to the conventional design which cascades a boost converter and a charge-pump circuit, the silicon area is greatly reduced due to employing only a boost converter. This leads to a compact integration and an obvious cost down of APD-based optical receiver.

Fig. 18 shows the steady-state operation of the LRHCR boost converter when the V_o is regulated at 55 V and the load current values I_o are 1 and 3 mA. The inductor current I_L demonstrates that the boost converter works in the DCM operation. In Fig. 18(a), the peak inductor current $I_{\rm L,peak}$ is 300 mA, and the negative current $I_{\rm neg}$ is -150 mA. The peak of inductor current is inevitably raised due to the negative inductor

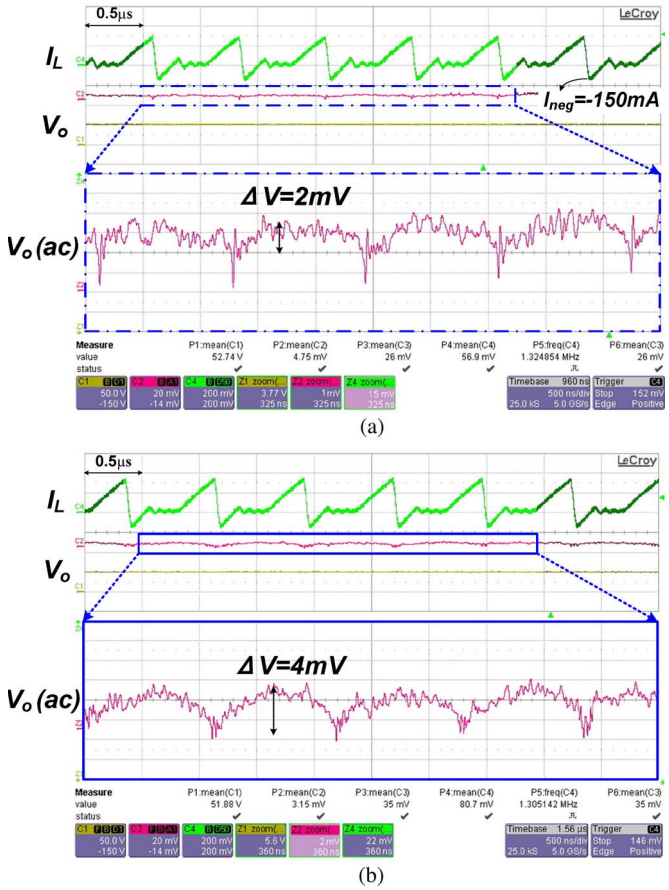

Fig. 18. Steady-state operation with load current values of (a) 1 and (b) 3 mA.

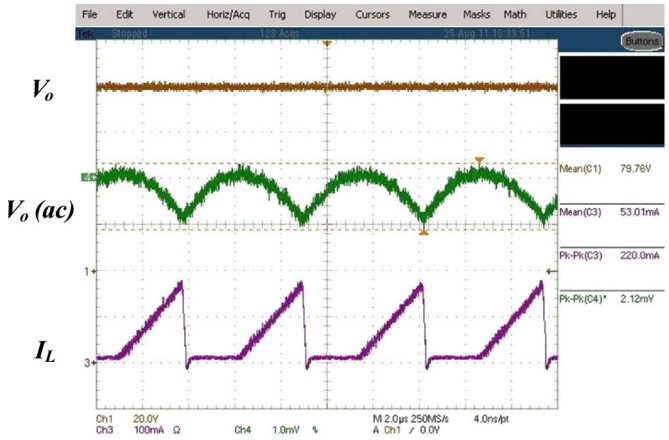

Fig. 19. Steady-state operation with the realization of DZCC circuit when the load current I_o is 1 mA.

current and the LC resonance. As a result, the voltage ripple values $Vo(\mathrm{ac})$ are 2 and 4 mV, as shown in Fig. 18(a) and (b), respectively.

However, it is hard to boost the V_o to 80 V due to the increasing inductor current caused by the effect of reverse recovery energy if the DZCC circuit is not enabled. After enabling the DZCC circuit, Fig. 19 shows a steady-state operation when the V_o is 80 V and the I_o is 1 mA. The output voltage ripple is suppressed to 2.12 mV due to the elimination of reverse recovery energy. These experimental results validate that the proposed boost converter can maintain the low ripple

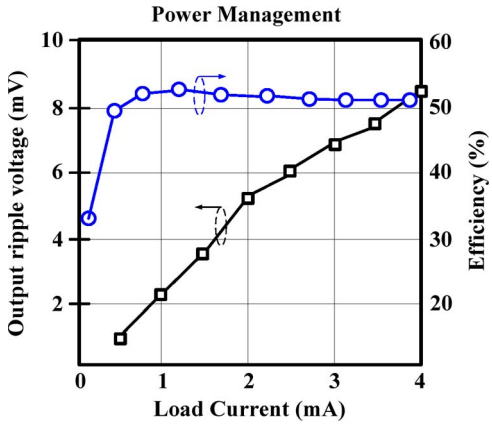

Fig. 20. Efficiency and output ripple voltage of the proposed power management.

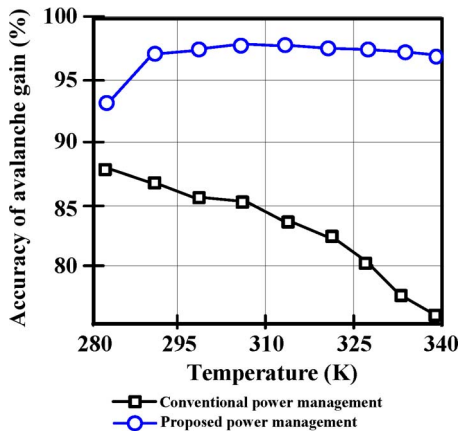

Fig. 21. Avalanche gain under the enable input of the DZCC circuit.

required for the APD communication system. Here, the low-pass filter is adopted to reduce the ripple voltage across the APD and thus guarantees the constant avalanche gain in each APD photodetector.

The efficiency is also measured when the output voltage is regulated at 80 V, as shown in Fig. 20. The maximum efficiency of 53% happens with a load of 1.2 mA. The conduction loss dominates the power consumption due to the relatively high inductor current level in this high-conversion-ratio topology. With the elimination of reverse recovery energy, both the efficiency and output ripple voltage are improved. The low ripple voltage reflects on a constant avalanche gain over a wide range of temperature variation, as shown in Fig. 21. Due to the nature of APDs, the avalanche gain decreases with the increase of temperature, leading to the decay on the accuracy of avalanche gain. The proposed power management maintains the accuracy of avalanche gain via the dynamic adjustment of bias voltage for APDs. Table I shows the summary of the performance.

Finally, a test board is shown in Fig. 22 to show the APD-based communication system.

VI. Conclusion

Traditional APD-based receivers are biased via external power modules in optical communications. Due to the nature

TABLE I
PERFORMANCE OF THE PROPOSED LRHCR BOOST CONVERTER

Technology		0.5 μm 80 V BCD process
Chip Area		1.09 mm^2 (1050 μm × 1033 μm)
Inductor / DCR		82 μH / 100 mΩ (nominal)
Capacitor / ESR		0.2 μF / 50 mΩ (nominal)
Switching frequency		200 kHz
Input voltage (V_{in})		3.3V
Maximum Output voltage (V_o)		80 V
Maximum Output Power		350 mW @ V_{in}= 3.3 V
Low Pass Filter	RC-LPF	R= 100 Ω, C= 0.1 μF
	LC-LPF	L= 2.2 μH, C= 0.1 μF
Voltage Ripple	@ I_o = 1 mA	2.12 mV
	@ I_o = 3 mA	7.2 mV

Fig. 22. APD-based communication system.

of APDs, the power requirement is extremely strict for a satisfactory level of avalanche gain in the optical communication. The temperature and voltage dependences of APDs make it difficult to maintain a constant avalanche gain through the open-loop power module, implying a decreased quality of communication system. The proposed power management emerges the AGC system and the LRHCR boost converter to provide an output voltage of 80 V and compensate the avalanche gain simultaneously. To eliminate the interference, the DZCC circuit suppresses the ripple voltage within 2.12 mV through the elimination of reverse recovery energy. A 97% accuracy of avalanche gain is obtained to guarantee the high quality of APDs. As a result, this design is well suited to be utilized on the biasing of APDs. In addition to advantages in terms of space, power, and reliability, this paper achieves tremendous cost savings at the same time.

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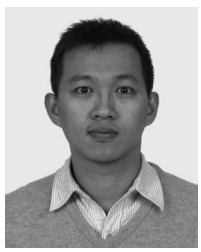

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