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# High-efficiency InGaN-based LEDs grown on patterned sapphire substrates using nanoimprinting technology

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ABSTRACT

This study employed roller imprint lithography and dry etching to fabricate patterned sapphire substrates (PSSs) of convex-shape with features of various heights. A soft polymer, polydimethylsiloxane (PDMS), was used as a mold to duplicate the pattern of a hard silicon template. The imprinted material was spin deposited onto a PDMS mold and transferred to the sapphire substrate using roller imprinting equipment. Inductive coupled plasma (ICP) etching was then used to fabricate the PSS. After epitaxial growth and chip processing, the current–voltage characteristics and light output of various LEDs were measured. The results demonstrate that the PSS process did not detract from the electrical properties of the LEDs; in fact, the output power of the proposed PSS LEDs was 25–30% greater than that of conventional LEDs. Simulation results show that PSS LEDs with structures of various heights would enhance optical efficiency in a manner similar to that demonstrated in these experiments.



## 1. Introduction

GaN-based light-emitting diodes (LEDs) have attracted considerable attention due to their small size, energy efficiency, longevity, and environmental friendliness [1–3]. However, the large difference in refractive index through the smooth interface between air ($n = 1$) and GaN ($n = 2.5$) can lead to considerable Fresnel loss and total internal reflection (TIR) [4], with a subsequent decrease in light extraction efficiency (LEE). The external quantum efficiency (EQE) of LEDs is determined by the internal quantum efficiency (IQE) and LEE. The IQE of GaN-based LEDs has been greatly improved because of advances in the crystal quality in recent years; however, increasing the LEE of LED chips remains a key factor in attaining higher EQE. In efforts to improve the LEE, various methods have been proposed to make it easier for emitted photons to escape into free space. These methods include altering the shape geometry of LEDs [5], surface roughening [6–7] and the use of a patterned sapphire substrate (PSS) [8–10]. Among these, the use of PSSs has been widely adopted in the industry because epitaxial quality and LEE can be improved simultaneously [11–13]. Previous research has indicated that LEE increases with a decrease in structural spacing [14]; however, decreasing structural spacing to the sub-micrometer scale is difficult to achieve using conventional photolithographic techniques. This study fabricated convex-shaped PSSs with sub-micron spacing and features of various heights using a rapid, low cost process, involving roller imprinting with dry etching. GaN-base LEDs were then prepared on the PSS using epitaxial growth and conventional chip fabrication processes. Finally, we investigated how the height of structures on the PSS influences light output.

## 2. Experiments

### 2.1. Fabrication of PDMS mold

Fig. 1(a) illustrates the process used in the preparation of the Si template. A $SiO_2$ layer (300 nm thickness) and photoresist (Shipley 1818) were spin deposited onto a two-inch Si substrate, respectively. The patterns were defined as an etching mask during inductively coupled plasma (ICP) etching via photolithography. The width of the cylinderical structures was 1.9 μm with spacing of 0.6 μm, as shown in Fig. 1(b). The heights of structures on the fabricated Si templates were 2 μm, 2.4 μm, and 3 μm, respectively.

A flexible mold was used for the non-planar imprinting process to ensure high imprint quality. Fig. 2 illustrates the procedure of fabricating the PDMS (Polydimethylsiloxane) mold and the results. The PDMS solvent and curing agent were mixed (10:1 weight ratio)

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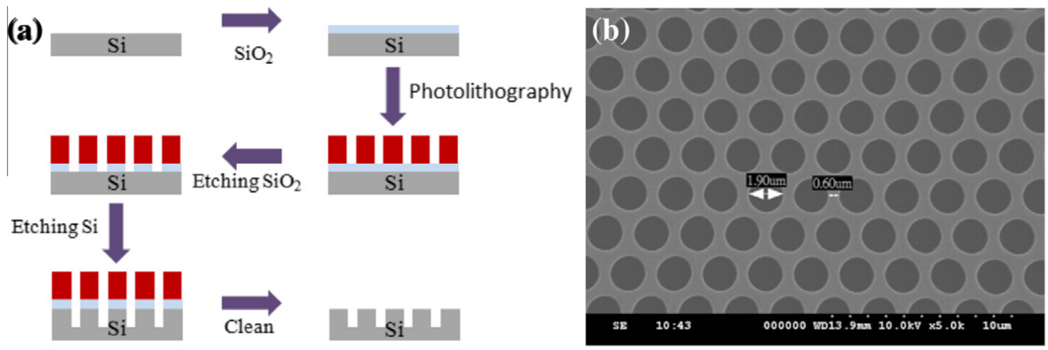


**Fig. 1.** (a) Schematic illustration of Si template; (b) SEM image of Si template.

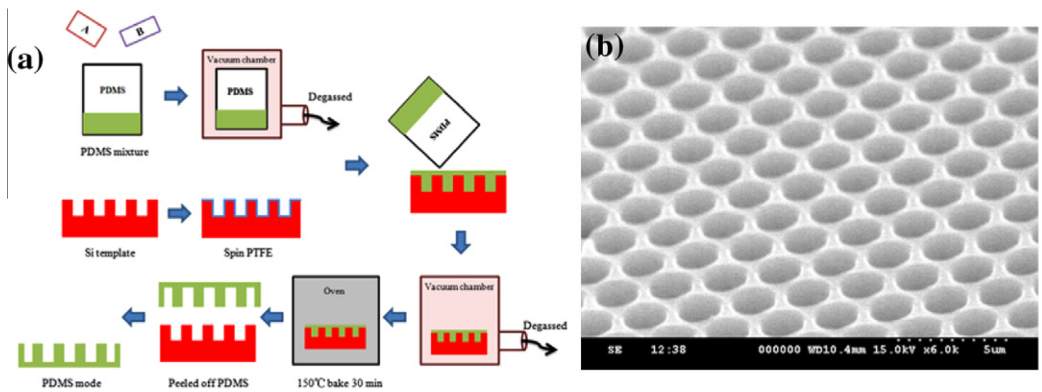


**Fig. 2.** (a) Schematic illustration of PDMS molding process; (b) SEM image of PDMS mold.

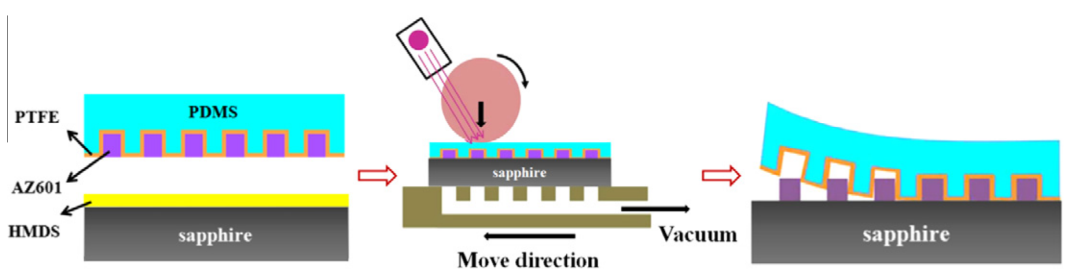


**Fig. 3.** Schematic illustration of roller imprinting process.

and degassed in a vacuum chamber to remove air bubbles from the mixture. After curing at 150 °C for 30 min, the solidified PDMS mold was peeled away from the Si template.

### 2.2. Roller imprinting process

Fig. 3 outlines the roller imprinting process. Rather than imprinting the entire surface at one time, the roller and substrate were imprinted progressively. This approach is applicable to the fabrication of structures with a large surface area [15–16]. Polytetrafluoroethylene (PTFE) was first sprayed onto the PDMS soft mold at 2000 rpm for 30 s and then cured at 200 °C for 10 min to obtain a lower surface energy. Hexamethyldisilazane (HMDS) was then sprayed onto the LED substrate at 6000 rpm for 30 s before being cured at 110 °C for 1 min to increase adhesion. Photoresist (AZ601) was sprayed onto the PDMS mold at room-temperature. The two-inch sapphire wafer was fixed to the translation stage using a vacuum holder in preparation for roller imprinting. During the imprinting process, a UV lamp was used as a curing source because the optical energy was sufficient to penetrate the quartz cylinder and PDMS mold and focus on the contact area.

### 2.3. Convex-shape PSS wafer preparation

In this study, convex-shaped PSSs were produced by dry etching. A mixture of $BCl_3$, $Cl_2$, and Ar gasses was introduced for ICP at flow rates of 40 sccm, 10 sccm, and 30 sccm, respectively. The ICP power and the RF power were set at 400 W and 166 W. Following the etching process, residual photoresist was removed using acetone, isopropyl alcohol, and DI water.

### 2.4. PSS LED epitaxy and chip process

The GaN-based PSS LED structure in this study was grown using metal organic chemical vapor deposition (MOCVD). The LED layer structure comprised a low-temperature GaN nucleation layer, a thick unintentionally doped GaN layer, a n-type GaN layer, an active region with 10 periods of InGaN/GaN multiple quantum wells (MQWs), and a p-type GaN layer. Indium tin oxide (ITO) was evap-

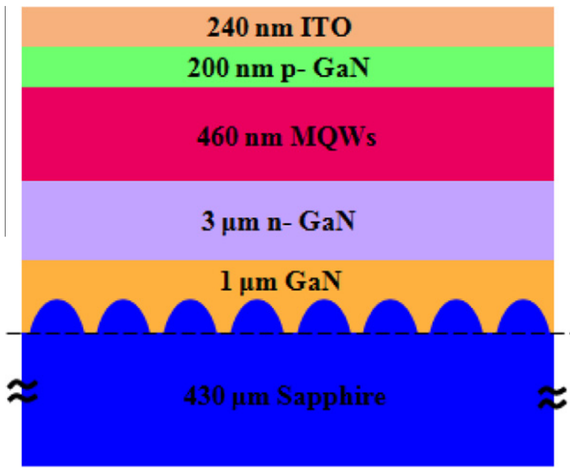


**Fig. 4.** Diagram of the PSS LED model for ray tracing simulation.

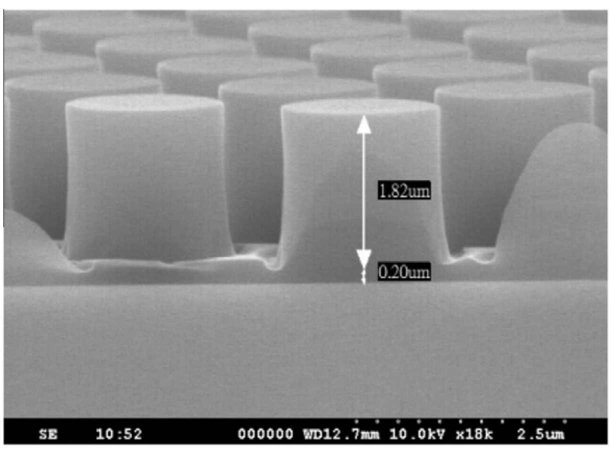


**Fig. 5.** SEM image of imprinted results.

orated onto the fabricated LED sample as a transparent conductive layer. Inductively coupled plasma (ICP) was used to partially etch the LED sample to expose the n-GaN. Optical lithography was used to define the ITO pattern, and wet etching was used to expose the p-GaN layer. The p- and n-electrodes were created by depositing Cr/Pt/Au on the p-GaN and n-GaN surfaces via thermal evaporation with rapid thermal annealing. The chip size of the fabricated LED sample was 615 μm × 1160 μm. The room temperature electroluminescence (EL) of the fabricated LED samples was then evaluated to identify the light intensity–current–voltage (*L–I–V*) characteristics by injecting the LEDs with various DC currents, with and without the PSS.

### 2.5. Light extraction analysis using the ray tracing method

To calculate extraction efficiency, we used Monte Carlo ray tracing to analyze the light propagation of LED chips with PSSs [17]. The simulation model of an LED chip with a sapphire of 430 μm, an n-GaN of 4 μm, an MQW of 460 nm, a p-GaN of 200 nm, and an ITO of 240 nm, is shown in Fig. 4. A two dimensional convex-shaped hexagonal close-packed array was arranged across the entire sapphire surface, as in the experiment. To reduce calculation time, the chip size was assumed to be 123 μm × 232 μm. The total emission power from MQW was set at 0.1 W. Mesa etching and electrodes on p- and n-GaN (as on the real chip) were disregarded. Light extraction was calculated according to the fraction of light collected by a spherical detector located 5 cm from the LED. The absorption coefficient of the MQWs was investigated; however, the effects of the other layers were considered inconsequential and therefore disregarded [18].

## 3. Results and discussion

Fig. 5 presents the imprinted results made using a PDMS mold with 2 μm deep structures. Our results revealed a residual layer (approximately 200 nm in depth) at the bottom of the structures, which decreased the height of the PSS structures following the ICP etching process.

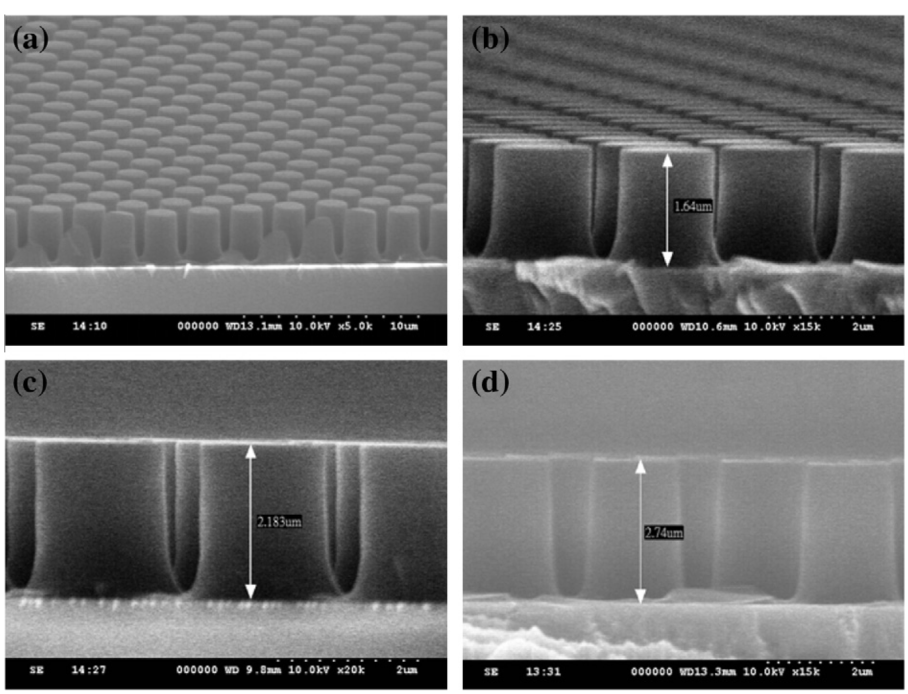


**Fig. 6.** SEM images of imprinted structures following $O_2$ plasma etching.

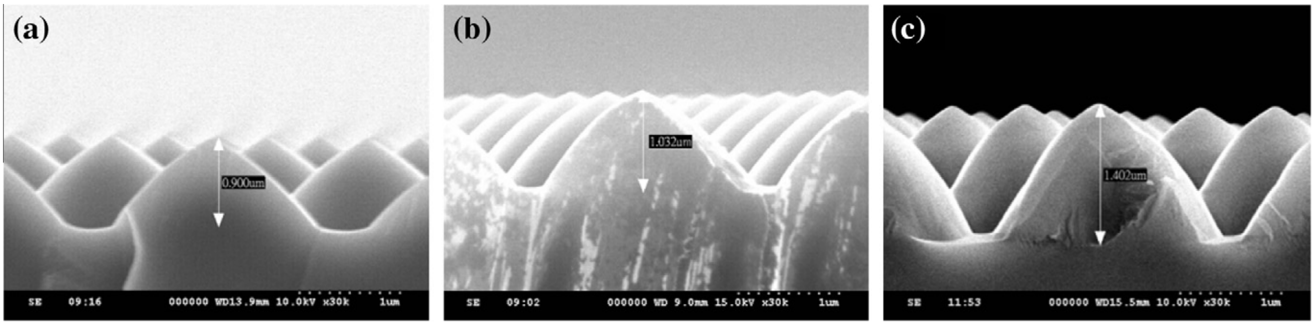


**Fig. 7.** SEM images of convex-shape PSSs with a structure height of (a) 0.9 μm, (b) 1 μm, (c) 1.4 μm.

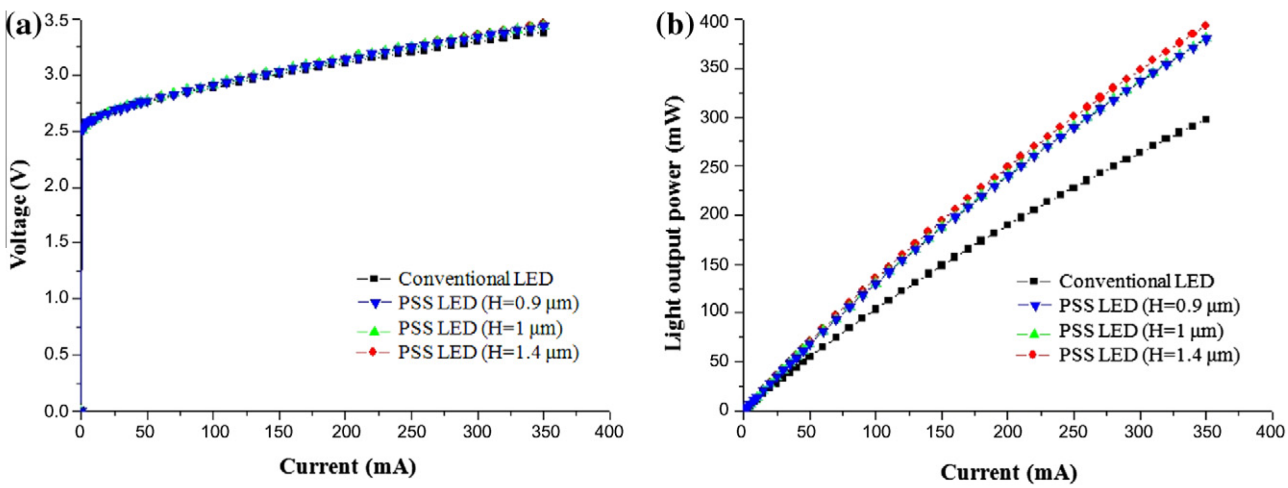


**Fig. 8.** (a) Current–voltage relationship of LEDs with and without the PSSs; (b) Output intensity of PSS LEDs and conventional LEDs as a function of driving current.

The residual layer was eliminated by applying $O_2$ plasma etching for 50 s, as shown in Fig. 6. Fig. 6(a) presents hexagonal close-packed structures with long-range order. The heights of the structures in Figs. 6(b)–(d) are approximately 1.6 μm, 2.2 μm, and 2.7 μm, respectively.

**Table 1**
Light output power and relative enhancement of various LEDs.

| LED types (structure height) | Output power | Enhancement (%) |
|---|---|---|
| Conventional LED | 122.03 | |
| PSS LED (0.9 μm) | 153.4 | 25.7 |
| PSS LED (1 μm) | 154.29 | 26.4 |
| PSS LED (1.4 μm) | 159.15 | 30.4 |

Fig. 7 presents SEM images of the convex-shaped PSS after ICP etching. The imprinted cylinders in Fig. 6(b)–(d) were used as an etching mask during the ICP etching process (22, 24, and 28 min, respectively). The structures in Fig. 7(a)–(c) are approximately 0.9 μm, 1 μm, and 1.4 μm in height.

Room temperature EL measurements of the InGaN LED with and without PSS as a function of forward current are presented in Fig. 8(a). Nearly all of the curves overlap, indicating that the electrical properties were not adversely affected by the PSS fabrication process. To investigate the influence of the PSS on the LEDs, the

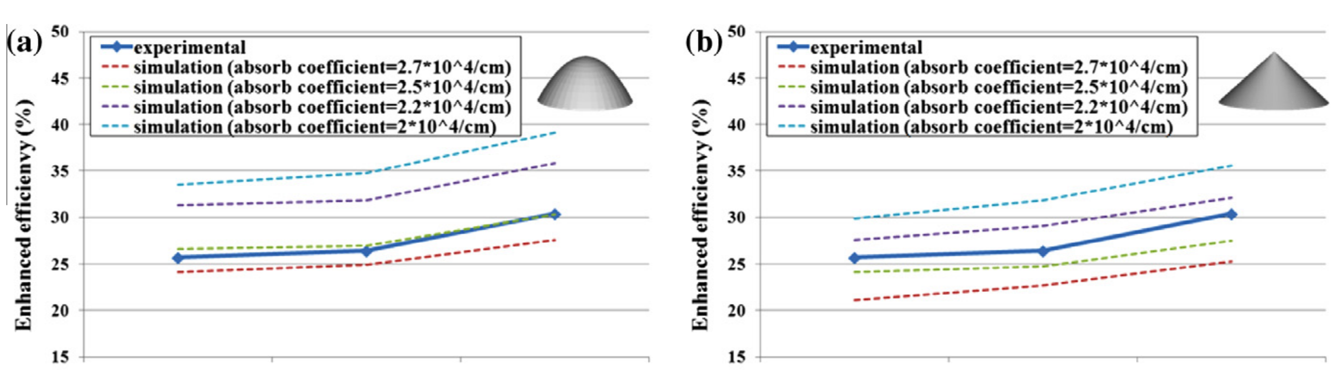


**Fig. 9.** Efficiency enhancement of the experimental and simulation results (compared to conventional LEDs) using structures of various heights: (a) PSS LEDs with paraboloidal structure; (b) PSS LEDs with conical structure.

optical performance of LED chips with and without the PSS was measured. The light output power versus injection current of the LED chips is shown in Fig 8(b). This figure demonstrates the effectiveness of the PSSs in enhancing optical efficiency, due to the redirection of photons emitted from the escape cone back into the escape cone. The output power of PSS LEDs with a current injection of 120 mA is shown in Table 1. The table also presents the difference in optical efficiency compared with conventional LEDs, indicating that the light extraction efficiency of PSS LEDs increased with an increase in the height of the structures.

To confirm the contribution of PSS to LEE, two PSS structures were constructed for ray tracing analysis: one with paraboloidal structures and the other with conical structures. Fig. 9 compares the simulation results with those from the experiment using structures of various heights. Because the absorption coefficient of the MQWs was unknown, we conducted several optical simulations using a range of absorption coefficients. Although the chip size was reduced to shorten simulation time and the structures were simplified representations of the actual PSSs, the trend of enhancement was very similar to that observed in the experiment. These results prove the reliability of optical simulations as analytical instruments prior to experimentation. Our experimental results indicate that the profiles of structure on the fabricated PSS tended toward paraboloidal and conical shapes. Results of simulated paraboloidal structures with an absorption coefficient of $2.5 \times 10^4$/cm were nearly identical to the devices used in the experiments. With structures of the same height and absorption coefficient; the simulated paraboloidal structure presented higher light extraction efficiency.

## 4. Conclusions

This study fabricated Si templates using photolithography and dry etching, followed by duplication of the patterns in a soft polymer PDMS mold. The imprinted material was transferred from the PDMS mold onto a sapphire substrate using roller imprinting equipment, whereupon an ICP etching mask was used to fabricate convex-shaped PSSs. Our results show that the PSS process did not have a detrimental effect on the LEDs. In both the experiments and simulations, increasing the height of structures was beneficial to the light extraction efficiency of PSS LEDs. Compared with conventional LED, optical efficiency was increased by 25.7%, 26.4%, and 30.4% when using structures with heights of 0.9 μm, 1 μm, and 1.4 μm, respectively.

## References


[1] M.R. Krames, O.B. Shchekin, R. Mueller-Mach, G.O. Mueller, L. Zhou, G. Harbers, M.G. Craford, J. Display Technol. 3 (2007) 160–175.
[2] T. Gessmann, E.F. Schubert, J. Appl. Phys. 95 (2004) 2203–2216.
[3] E.F. Schubert, J.K. Kim, Science 308 (2005) 1274–1278.
[4] A. David, T. Fuji, R. Sharma, K. McGroddy, S. Nakaruma, S. DenBarrss, E.L. Hu, C. Weisbuch, H. Benisty, Appl. Phys. Lett. 88 (2006) 133514-1–133514-3.
[5] M.R. Krames, M. Ochiai-Holcomb, G.E. Höfler, C. Carter-Coman, E.I. Chen, I.H. Tan, P. Grillot, H.C. Chui, J.W. Huang, S.A. Stockman, F.A. Kish, M.G. Craford, Appl. Phys. Lett. 75 (1999) 2365–2368.
[6] C. Huh, K.S. Lee, E.J. Kang, S.J. Park, Appl. Phys. Lett. 93 (2003) 9383–9385.
[7] T. Fujii, Y. Gao, R. Sharma, E.L. Hu, S.P. DenBaars, S. Nakamura, Appl. Phys. Lett. 84 (2004) 855–857.
[8] J.H. Lee, J.T. Oh, J.H. Lee, IEEE Photonics Technol. Lett. 20 (2008) 1563–1565.
[9] N. Okada, T. Murata, K. Tadatomo, H.G. Chang, K. Watanabe, Jpn. J. Appl. Phys. 48 (2009) 221031–1221034.
[10] J.B. Kim, S.M. Lim, Y.W. Kim, S.K. Kang, S.R. Jeon, Jpn. J. Appl. Phys. 49 (2010) 0421021–0421024.
[11] K. Tadatomo, H. Okagawa, Y. Ohuchi, Phys. Status Solidi A-Appl. Mat. 188 (2001) 121–125.
[12] D.S. Wuu, W.K. Wang, K.S. Wen, S.C. Huang, S.H. Lin, R.H. Horng, Y.S. Yu, M.H. Pan, J. Electrochem. Soc. 153 (2006) G765–G770.
[13] D.S. Wuu, W.K. Wang, K.S. Wen, S.C. Huang, S.H. Lin, S.Y. Huang, C.F. Lin, R.H. Horng, Appl. Phys. Lett. 89 (2006) 161–163.
[14] J.H. Lee, D.Y. Lee, B.W. Oh, J.H. Lee, IEEE Trans. Electron Devices 57 (2010) 157–163.
[15] J.J. Lee, S.Y. Park, K.B. Choi, G.H. Kim, Microelectron. Eng. 85 (2008) 861–865.
[16] H. Tan, A. Gilbertson, S.Y. Chou, J. Vac. Sci. Technol. B. 16 (1998) 3926–3928.
[17] T.X. Lee, K.F. Gao, W.T. Chien, C.C. Sun, Opt. Express 15 (2007) 6670–6676.
[18] J.F. Muth, J.D. Brown, M.A.L. Johnson, Z. Yu, R.M. Kolbas, J.W. Cook, J.F. Schetzina, MRS Internet J. Nitride Semicond. Res. 4S1 (1999) G52–G54.